

# Output Data Format for the ATLAS LAr Front End Board

John Parsons, Stefan Simion  
Nevis Labs, Columbia University

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## Abstract

This note describes the format of the output data stream of the the ATLAS LAr Front End Board.

## 1 Introduction

The Front End Board (FEB) [1] of the ATLAS LAr readout is responsible for the calorimeter signal amplification, shaping, and sampling at the LHC bunch crossing frequency of 40 MHz. A total of 128 calorimeter channels are processed by each FEB. For events corresponding to Level 1 Accepts, typically 5 samples per channel are digitized, serialized, and transmitted off-detector via 1.6 Gbps optical fiber.

### 1.1 FEB Channel Mapping and Data Flow

Each FEB handles 128 calorimeter channels. To achieve this density, components are mounted on both sides of the PCB. By convention, the “top” side of the FEB is the side on which all of the through-hole connectors are mounted. The top side can also be identified as the side on which are mounted the ADCs and most of the main digital ASICs, including the Gain Selectors, the SCA Controllers, the SMUX, and the GLink.

Figure 1 shows a photo of the top side of the FEB, with labels showing some of the main components. In the photo, the FEB is oriented with the

calorimeter signal input connectors at the bottom of the photo, and with the OTx of the output optical link emerging through the FEB front panel at the top of the photo.

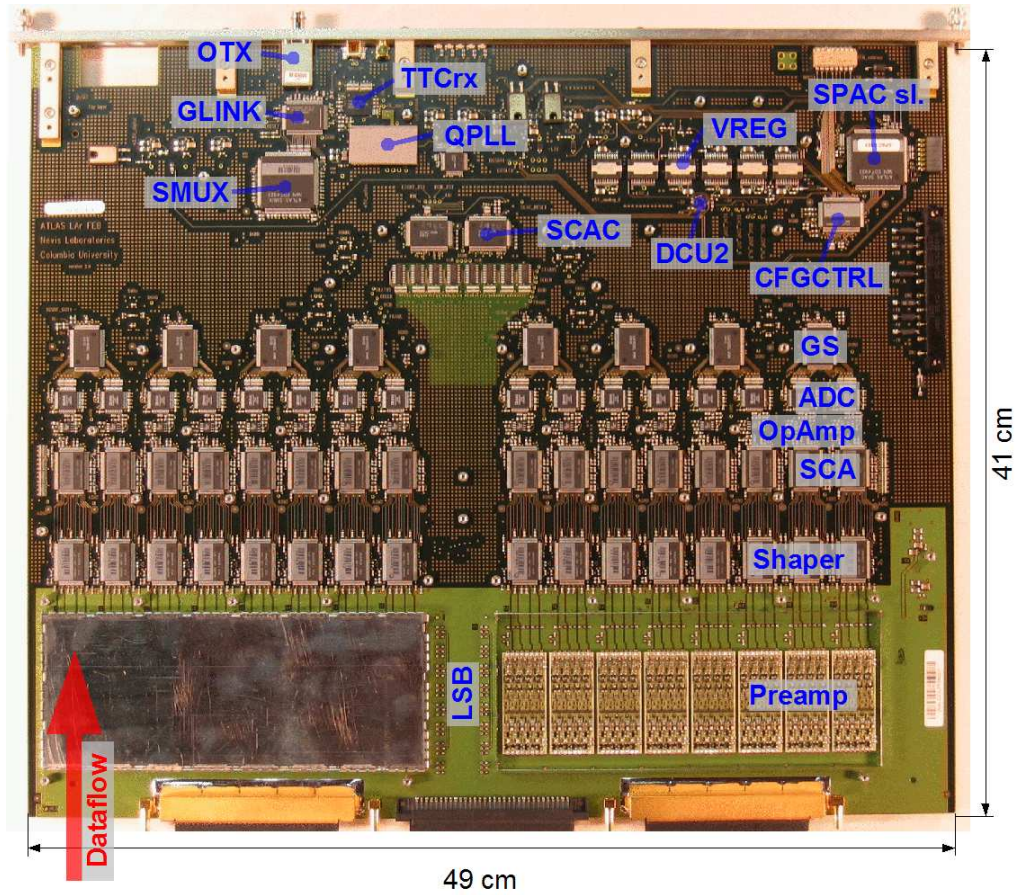


Figure 1: Photograph of the top side of the FEB.

The basic data flow on the FEB can be followed through the photo. Calorimeter signals enter at the bottom of the photo, and are routed through successive stages of analog processing, first preamplifiers, then shaper chips, and then SCA chips. Each combination of preamp+shaper+SCA manages 4 channels. Digitization is performed by 16 ADC chips, each handling 8 calorimeter channels, from the corresponding pair of SCAs mounted on the top and bottom surfaces of the FEB. The digital ADC outputs are trans-

mitted to Gain Selector (GSEL) ASICs. Each GSEL manages the data from two neighboring ADCs, corresponding to 16 channels.

As discussed in section 1.2, the GSEL formats data from a given ADC into 16-bit words. These are partially serialized, and then transmitted at 40 MHz via a pair of signal lines to the SMUX chip. The SMUX accepts the corresponding 32 data lines (2 lines for each of 16 ADCs), and performs a 2:1 multiplexing, providing 16 output lines at 80 MHz. These 16 lines are connected to the GLink chip, which performs the final serialization for optical transmission via the OTx.

The full schematics of the final FEB (FEB Version 2.0) are available at [http://www.nevis.columbia.edu/~atlas/electronics/ATLASFEB/FEB\\_v2.0\\_sch.pdf](http://www.nevis.columbia.edu/~atlas/electronics/ATLASFEB/FEB_v2.0_sch.pdf). In this orientation, the 16 ADCs are numbered in order from ADC\_1 on the left, through ADC\_16 on the right, where the notation is consistent with that used in the schematics. Similarly, the Gain Selectors are ordered from UG\_1 on the left through UG\_8 on the right.

Figure 2 tabulates the mapping of the 128 calorimeter channels through the various chips on the FEB. Within a group of 8 channels digitized by one ADC, the channels are multiplexed in order of increasing channel number.

SMUX Input	0, 1	2, 3	4, 5	6, 7	8, 9	10, 11	12, 13	14, 15	16, 17	18, 19	20, 21	22, 23	24, 25	26, 27	28, 29	30, 31
GSEL Number	1		2		3		4		5		6		7		8	
ADC Number	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Channel Numbers	0 -	8 -	16 -	24 -	32 -	40 -	48 -	56 -	64 -	72 -	80 -	88 -	96 -	104 -	112 -	120 -
	7	15	23	31	39	47	55	63	71	79	87	95	103	111	119	127

Figure 2: Mapping of the FEB channels through various chips on the FEB.

## 1.2 Gain Selector Output Data Format

The event data is formatted by the Gain Selector (GSEL) ASIC [2]. Each GSEL handles the data from two separate ADC chips, which digitize 8 calorimeter channels each. Therefore, 8 GSEL chips are required per 128-channel FEB.

For the 8 channels corresponding to a single ADC, the GSEL formats the data into an event fragment of 16-bit words according to the format shown in Fig. 3. Thus, each GSEL forms two such event fragments per event, which are prepared separately within the corresponding GSEL.

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Frame start	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Evt head 1	0	P	0	0	ADCID				PHASE			EVENTN				
Evt head 2	0	P	0	0	BCID											
Samp 1 head	0	P	0	0	F	L	B	A	CELLN							
Samples	0	P	Gain		ADC channel 0 sample 1											
	0	P	Gain		ADC channel 1 sample 1											
	0	P	Gain		ADC channel 2 sample 1											
	0	P	Gain		ADC channel 3 sample 1											
	0	P	Gain		ADC channel 4 sample 1											
	0	P	Gain		ADC channel 5 sample 1											
	0	P	Gain		ADC channel 6 sample 1											
	0	P	Gain		ADC channel 7 sample 1											
...	...															
...	...															
Last samp head	0	P	0	0	F	L	B	A	CELLN							
Samples	0	P	Gain		ADC channel 0 last sample											
	...															
	0	P	Gain		ADC channel 7 last sample											
Evt trailer	0	P	0	0	1	S	E	SCAC status								1
Frame end	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 3: FEB readout event format.

As described in more detail in the following sections, the event fragment format consists of the following 16-bit words:

1. a frame start word,
2. two event header words,
3. data words carrying the calorimeter signal data,
4. an event trailer word, and
5. at least one frame end word to separate from the next event.

### 1.3 Frame Start Word

The Frame Start Word is all ones, and signals to the ROD the start of a new event. Note that this word violates the odd parity requirement imposed on the remaining words.

### 1.4 Event Header Words

The first event header word carries the 4-bit ID number of the corresponding ADC, the 3-bit phase of the 5 MHz RCLK for this L1Accept, and a 5-bit event number.

The second event header word contains the 12-bit BCID number for this L1Accept.

For both header words, bits 15, 13 and 12 are zero, while bit 14 is used as a Parity bit to impose odd parity.

### 1.5 Calorimeter Data Words

The number of signal data words per event fragment depends on the number of samples and number of gains configured to be read out.

#### Sample Header Word

For each sample, there is first a sample header word, which contains the 8-bit SCA cell (capacitor) number, three “sample mode” bits, and one bit which has a value of 0 for normal data and 1 for data taken in a mode where configurable test data is transmitted instead of data from the ADC (for details, see the GSEL specification in reference [2]).

The sample mode bits indicate whether the sample in question is the first (F) or last (L) sample of the event, or whether the so-called Backporch (B) bit has been set for this event. If the Backporch bit is set in auto-gain mode, the gain selection algorithm was modified to prevent any channel from using a higher gain than in the previous event. This flag can be set by the SCA Controller [3] for events that occur less than some specified time (eg. the total LAr drift time of  $\approx 400$  ns) after the previous event, with the goal of preventing an incorrect gain selection for the second event in cases of large signals in the first event.

For the sample header word, as for the event header words described previously, bits 15, 13 and 12 are zero, while bit 14 is used to impose odd parity.

### ADC Data Words

The sample header word is followed by  $n \times 8$  words containing the ADC data for that sample, where  $n$  is the number of gains to be read out. The factor of 8 arises since each event fragment corresponds to a single ADC, or 8 calorimeter channels. Each ADC word includes the 12-bit ADC value in bits 0 through 11. Bits 12 and 13 encode the gain (01 = LOW gain, 10 = MEDIUM, 11 = HIGH). Bit 14 is used to impose odd parity, and bit 15 is zero.

The FEB is designed such that, for each sample and gain, the 8 ADC words come in order according to increasing channel number. When the FEB is configured to read multiple gains, the order in which the various gains are read is specified in the configuration data which is downloaded to the GSEL (see the Gain Selector documentation [2] for more details). The first 8 ADC words contain the data for all 8 channels for the first gain to be read, the next 8 ADC words contain the data for the second gain, and so on.

## 1.6 Event Trailer Word

The event trailer (status) word contains the 8-bit SCA Controller (SCAC) status word in bits 1 through 8. The SCAC status bits are not directly associated with the event, but indicate whether various errors or other conditions have been met. Whenever such a condition occurs, the SCAC sets the corresponding status bit, which will then be transmitted with the data in the next event which is read out.

The SCAC status bits are:

**Bit 1:** Init. A reinitialisation of the sequence occurred.

**Bit 2:** BCID Reset. The BCID counter was reset.

**Bit 3:** Double Bit Error. A cell address was found with two bits in error. This bit will reoccur repeatedly, since the error will not be corrected.

**Bit 4:** Single Bit Error: A cell address was found with a single bit error. This error was corrected.

**Bit 5:** Sequence Error: The sequence of cell addresses is corrupted. This error bit will be set without indicating harm if cell number sequencing is disabled in the configuration.

**Bit 6:** Free FIFO Underrun. The SCA run out of free cells. Invalid cell numbers were inserted into the sequence.

**Bit 7:** Done FIFO overflow.

**Bit 8:** Chip ID (Serial address bit 6).

More details of the SCAC status bits can be found in the SCAC documentation [3].

Bits 9 and 10 of the event trailer word are used as flags to indicate that single or double bit errors, respectively, have been detected in the Error-Detection-and-Correction (EDC) logic of the GSEL. When such errors are detected, the corresponding bits are set to one. An appropriate SPAC command is required to reset the flag bits to zero. In case of a double bit error, the GSEL parameters have been corrupted and must be reloaded via SPAC. As for the SCAC described above, single bit errors in the GSEL parameters are corrected automatically, but the flag in Bit 8 can be used to monitor the rate of such errors.

In the event trailer word, bits 0 and 11 are set to one, while bits 12, 13 and 15 are zero. As usual, bit 14 serves to impose odd parity.

For events with no errors, the Event Trailer half-word should be 0x4801 (or 0x0805 for an event which is the first trigger following a BCID Reset).

## 1.7 Frame End Word

When the readout is idle, words of all zeros are sent. The all-zeros word also serves as the Frame End Word, indicating to the ROD that an event has been completed. The FEB is designed to ensure that there is at least one such word transmitted between events. Note that, like the Frame Start Word, this word violates the odd parity rule imposed on all other data words.

## 2 FEB Data Serialization

The formatted event fragments of 16-bit words from each GSEL are serialized in a sequence of steps that results in a single 1.6 Gbps bit-serial output stream

being transmitted via optical link from each FEB.

The first step in the serialization is performed by the GSELS. For each of its two event fragments of 16-bit words, the GSEL outputs two bits parallel at 40 MHz, taking eight 40 MHz clock cycles to output each partially serialized 16-bit word.

With 8 GSELS per FEB, and with each GSEL outputting 4 data lines (2 event fragments, each with two data lines), the SMUX chip [4] receives a total of 32 data bits at 40 MHz. The SMUX then performs a 2:1 multiplexing in order to generate an output stream of 16 bits at 80 MHz. In addition, the MUX generates a FLAG, which is set to one for the MUX cycle when data from channels 0 - 63 are sent to the GLink and set to zero for the MUX cycle when data from channels 64 - 127 are sent.

The 16 SMUX data output signals and FLAG are then transmitted at 80 MHz to the GLink serializer chip, which adds protocol and control bits and produces a single serial output stream of 1.6 Gbps. In the final step, this serial stream is converted to an optical signal and transmitted off of the FEB via the OTx.

At the ROD end of the fiber, the 1.6 Gbps optical signal is converted back to an electrical signal via the ORx. It is then de-serialized by the GLink receiver back into an image of the 16 bits at 80 MHz data stream output from the SMUX. Details of the GLink protocol and serialization/de-serialization are managed transparently by the GLink chipset.

### 3 Data Valid Signal

In addition to the event fragment data, the GSEL outputs a DataValid (DAV) signal. DAV is active (LO true) during the transfer of all words belonging to the event data block, except for the mandatory Frame End (all zeros) word that is inserted between events.

The DAV signal from one GSEL per half-FEB was routed on the FEB and could be connected or not to the SMUX chip depending on some solderable jumpers on the FEB. In response to a request from the ROD design team, the FEBs were produced with the jumpers set such that the DAV signal is in fact connected. This choice must be taken into account on the ROD for proper functioning of the FEB-ROD optical link.

## References

- [1] J. Ban, S. Negroni, J. Parsons, S. Simion, and B. Sippach, “Design and Implementation of the ATLAS LAr Front End Board”; available at <http://www.nevis.columbia.edu/~atlas/electronics/ATLASFEB/FEBnote.pdf>.
- [2] S. Boettcher, J. Parsons and W. Sippach, “The Gain Selector ASIC for the ATLAS LAr Calorimeter”; available at <http://www.nevis.columbia.edu/~atlas/electronics/asics/ggains/gainsel.ps>.
- [3] S. Boettcher, J. Parsons, W. Sippach, and D. Gingrich, “The SCA Controller for the ATLAS LAr Calorimeter”; available at <http://www.nevis.columbia.edu/~atlas/electronics/asics/scac/scac-dsm.ps>.
- [4] D. Dzahini, et al., “The SMUX Chip Production Readiness Review”; available at <http://agenda.cern.ch/fullAgenda.php?ida=a0316>.