QPLL proton irradiation

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1. QPLL test board

The printed circuit board designed for radiation carries the QPLL circuit and the quartz crystal; a bank of switches connecting to the QPLL `FSEL[5..0]` and `ExtCntl` inputs; a power supply connector; and LEMO connectors for the input clock signals and for the 40 MHz output clock signal. The `inLVDS±` and `lvds40MHz±` are converted to single-ended 50 Ω signals using transformers.

2. Measurement setup and results

For the test we use a HP53131A frequency counter. The 10 MHz reference from the HP53131A is used to feed an Analog Devices AD9852 direct digital synthesizer, which generates a precise programmable frequency for the QPLL input. The AD9852 is programmable via the parallel port of the data acquisition PC. The QPLL output clock is connected to the HP53131A input. The counter measures the QPLL output clock frequency continuously, with a gate set to 1 s for good precision. If the QPLL is locked we expect that the measured frequency is exactly (within less than 0.1 Hz) equal to the frequency programmed into the synthesizer board.

The frequency counter is configured to “print” each measurement to the RS232 output, which is connected to the serial port of the PC.

When monitoring the QPLL output, the data acquisition program ignores the first frequency measurement immediately following a frequency change (reprogramming of the AD9852) to allow the QPLL the time to lock to the new frequency. The actual time spent to re-lock is not measured.

The radiation run took place on February 28th at the Northeast Proton Therapy Center at the Massachusetts General Hospital.

Seven boards (QPLL+XTAL) were irradiated to 2.5 10^{13} p/cm^2 (160 MeV) each. Two boards (Q0 and Q7) were set in fixed frequency range mode (`ExtCntl=1`), and were tested in a 20-second cycle where the input was a fixed frequency within the lock range for 16 seconds (to look for SEU-induced unlock) and the input was turned off the remaining 4 seconds, to measure the free-running frequency as a function of proton fluence.

The remaining five boards were set to auto range mode (`ExtCntl=0`), and were tested in a 1-minute cycle where the input is one of three fixed frequencies, cycled through every 20 seconds (to look for SEU-induced unlock). For these five boards, the lock range was measured at the beginning and at the end of the irradiation.

One, possibly two events which could be SEUs were observed. One event was for board Q4, namely a single incorrect frequency reading while the input clock was stable. However this board had a PCB contamination problem (circuit would not oscillate) before it was irradiated; was fixed; and then again stopped working long after the beam was turned off. It is therefore probable that the SEU-like event for this board was not beam-related.

The second event was with board Q5, which at one point took more than 1 s to lock after switching to the new frequency. The frequency measured by the counter was correct only one extra cycle after the frequency changed. We understand that the frequency calibration (range selection) logic inside the QPLL is not protected against SEUs, since the circuit would anyway restart the frequency calibration cycle in case of an error. We do not expect frequency calibration cycles to occur very often during normal LHC operation.

The power supply current and the free-running frequency versus fluence are shown in Figure 1 for board Q7 and Figure 2 for board Q0[1]. The power supply current versus fluence is shown in Figure 3 for boards Q2, Q3, Q5, and Q6. For board Q4, the current measurement is not useable, possibly related to the PCB contamination problem mentioned above. Figure 4 shows the frequency lock range for boards Q2 through Q6, before and after irradiation.

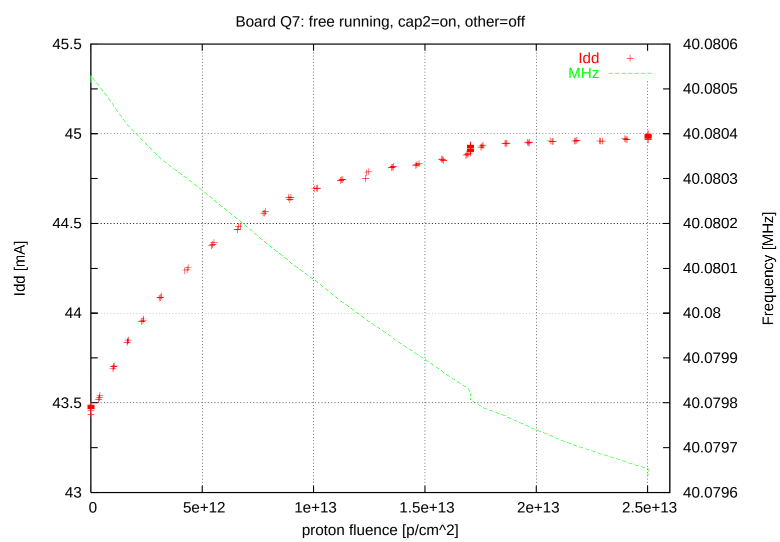

Figure 1: Power supply current and free-running frequency versus proton fluence for board Q7.

1. For board Q0, the inLVDS± inputs were pulled low or high with 2 kΩ resistors do disable this input and use the CMOS clock input; however the 100 Ω termination across inLVDS± was also present due to a PCB cabling error. As a result, the voltage at LVDS± may not have been sufficient to disable this input. This may explain why sometimes when in free-running mode, the Q0 board oscillates at the higher limit, instead of the lower limit, of the fixed-frequency range; and why it would not lock on the CMOS clock input.

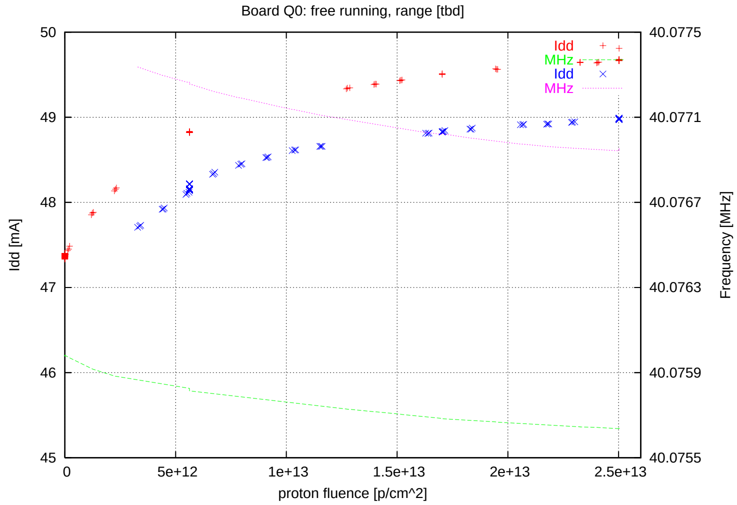

Figure 2: Power supply current and free-running frequency versus proton fluence for board Q0. The higher power supply current (red markers) corresponds to the lower free-running frequency (green curve).

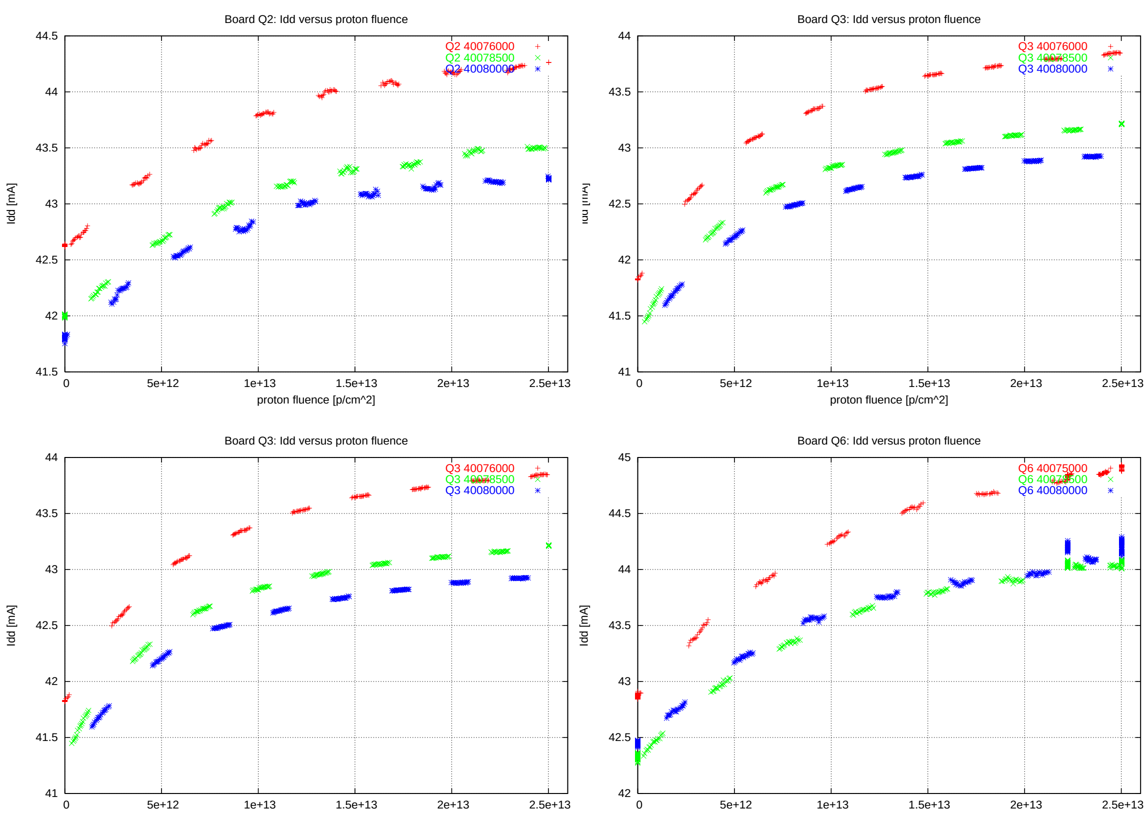

Figure 3: Power supply current versus proton fluence for boards Q2, Q3, Q5, and Q6. The input clock frequency was changed at 20 s intervals.

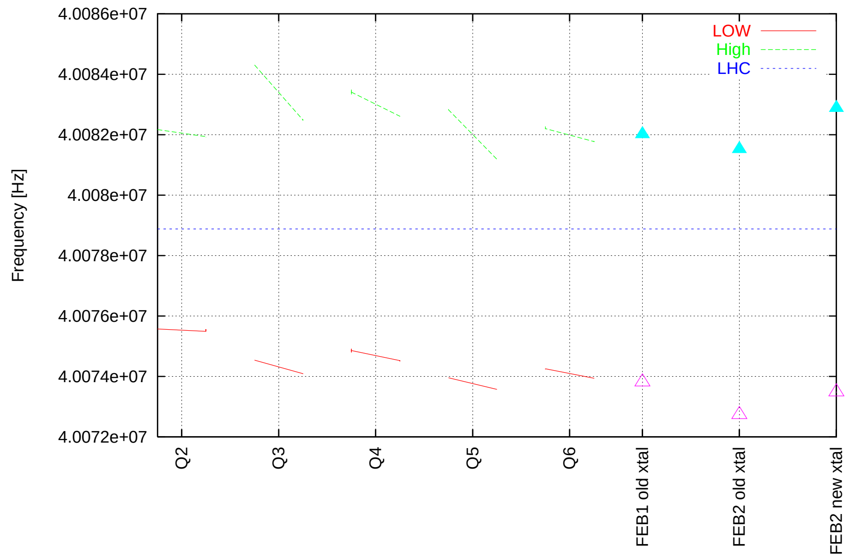

Figure 4: Frequency lock range for boards Q2 through Q6 before and after irradiation. Also shown are the lock ranges measured on two front-end boards.

3. Conclusion

Seven QPLL and crystals were irradiated with 160 MeV protons up to 2.5 10^{13} p/ cm^2 . No latch-up was observed. One, possibly two SEUs were observed, from which the QPLL recovered without external intervention. The upper and lower limits of the frequency lock range decreased after irradiation[1]; however, the circuit was always able to lock on the nominal LHC frequency. The measurement was not sensitive to upsets in the QPLL output frequency divider/counter.

4. Acknowledgements

We thank Ethan W. Cascio for his support and for the excellent operation of the Mass. General Hospital cyclotron.

1. This effect is confirmed by irradiation tests performed by CERN and understood to be caused by ionizing radiation.