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08/01/02

## ***Proposed pipeline depth increase for muon PDT and SC electronics***

We have considered possible implementation of the pipeline depth increase in two muon detector sub-systems: Scintillation Counter (SC) Electronics and Proportional Drift Tube (PDT) Electronics. Currently both sub-systems have about 4.8  $\mu$ S depth of the event data pipeline, which is not sufficient to work with increased L1 trigger decision time that may be required for Run IIb. Listed below are our recommendations on proposed changes.

### *1) PDT Electronics.*

We propose that main clock frequency of the TMC-TEG3 chip is changed from  $RF/2$  to  $3RF/7$ . This will result in an increase of the pipeline depth from 4.82  $\mu$ S to 5.62  $\mu$ S. The increase is about six 132 ns “ticks”. The bin width of the TMC will change from 1.18 nS to 1.37 nS. This is a 16% degradation of the time resolution and may be considered negligible. The following steps are required to implement this change:

- Modification of the firmware on all 110 Control Boards (two chips per board)
- Installation of the additional wires (4) on all Control Boards
- Modification of the main DSP software for the Control Board (remove even/odd crossing correction and change bin width constant)
- Modification of the hardware database and control and monitoring software due to the changes in the CB registers (L1 TxEn delay)

Listed above steps require removal of the Control Boards from the collision hall. Estimated time for the hardware upgrade is about 3 weeks. At least one skilled technician is needed for this project to perform CB modifications. Fully implemented upgrade has to be tested with the detector installation prior to modifications. This modification requires access to the D0 collision hall.

### *2) SC Electronics*

We propose that additional six 132 nS “ticks” are added to the SFE pipeline by modifying internal ALTERA FPGA logic. The modification will change clock frequency of the auxiliary pipeline from  $4RF/7$  to  $RF/7$ . This will result in an increase of the pipeline depth from 4.745  $\mu$ S to 5.537  $\mu$ S. The following steps are required to implement this change:

- Modification of the firmware on all 145 SFE modules

- Modification of the hardware database

Listed above steps do not require removal of the SFEs and can be done remotely. Estimated time for upgrade is about 2 weeks. Fully implemented upgrade has to be tested with the detector installation prior to modifications. This modification does not require access to the D0 collision hall.