

Buffer Controller – Logic Daughterboard Communications

5 July, 2002

1) Introduction

Communication between the Buffer Controller (BC) and the Logic Daughterboard (DB) is accomplished using PCI-3 and six special purpose lines (*SPARE0-SPARE5* on the J4/P4 connectors on the motherboard¹). All of these lines are defined as active hi. Note – in the current implementation, L1/2_ERROR and L1/2_BUSY signals from the DBs to the BC are ignored. The signals described in the table below are generated internally by the BC. It may prove useful to get error/busy input from the DBs in the future (and is a straightforward change to the BC logic) so these lines should be maintained in the DB designs.

Name	J4/P4 Pin	Direction	Use
<i>DB_L3_DATA</i>	26	DB→BC	DB has L3 data to transfer ²
<i>BC_BUSY</i>	30	BC→DB	BC has received L3 data
<i>L1_ERROR</i>	34	DB→BC	BX mismatch between BM and DB L3 data DB requests SCL Init
<i>L1_BUSY</i>	38	DB→BC	not defined
<i>L2_ERROR</i>	42	DB→BC	BX mismatch in data sent to output FIFO
<i>L2_BUSY</i>	46	DB→BC	L3 output FIFO on BC is full

Table 2: Direct communication lines between BC and DB.

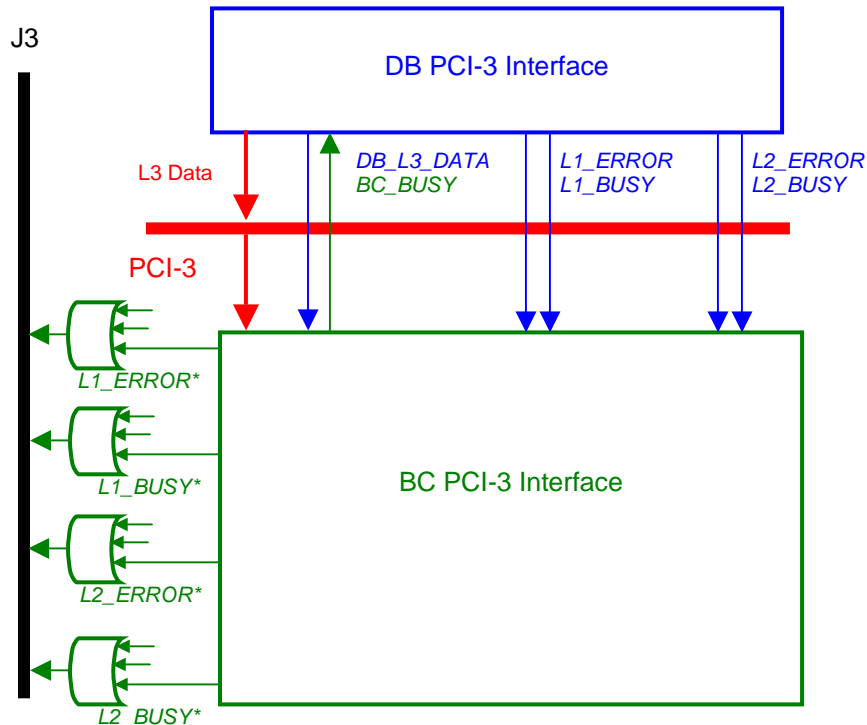


Table 1: BC to DB communication.

References

¹ E. Hazen and S. Wu, *Motherboard Electrical Specification Update* (7 July, 2000), http://ohm.bu.edu/~hazen/my_d0/mb9u/mb_update.html

² *L3 Data Buffer on the Daughterboards*, http://www.nevis.columbia.edu/~evans/stt/docs/L3_Buffer.pdf