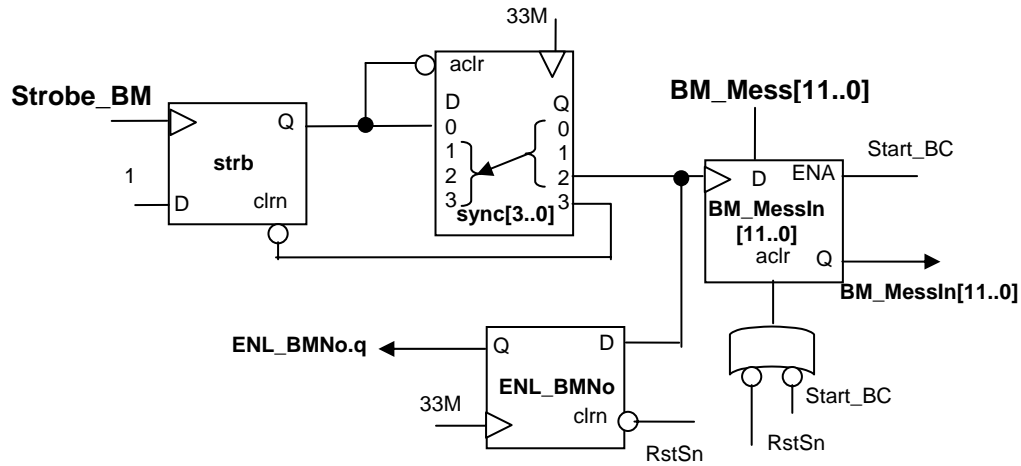


Buffer Controller: Messages from BM

code version: 20-May-03
 created in: *pci3_lm.tdf, b_ctrl.tdf*



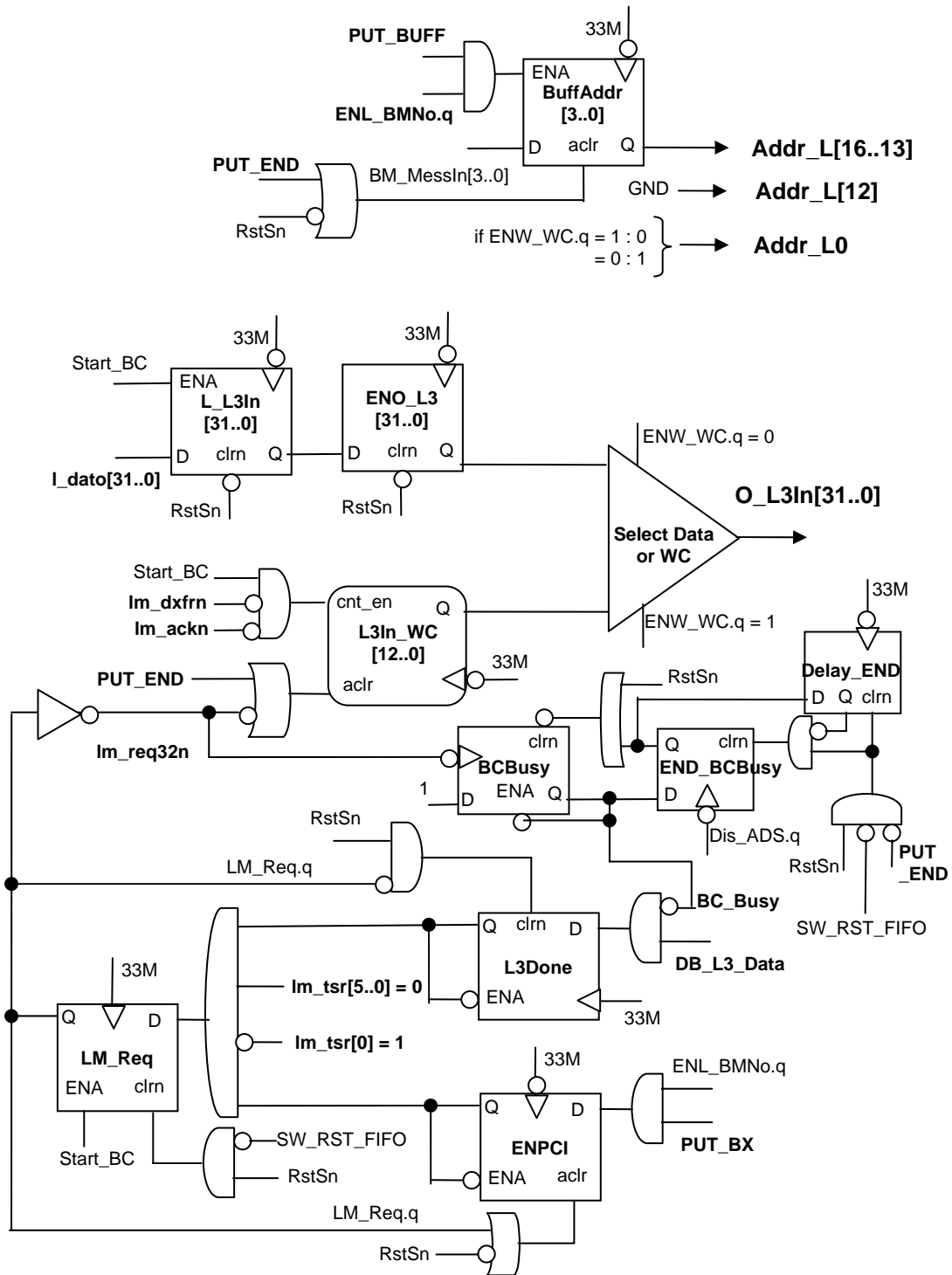
Same structure used:

- *PCI3/pci3_lm.tdf* PUT messages
- *buf_Ctrl/b_ctrl.tdf* GET messages

BM_MessIn[11..8]	PUT Flag Set	BM_MessIn[11..8]	GET Flag Set
[11..8] == 1	PUT_BUFF	[11..4] == 0x40	GET_BUFF
[11..8] == 2	PUT_BX	[11..8] == 5	GET_BX
[11..8] == 3	PUT_END	[11..0] == 0x600	GET_END

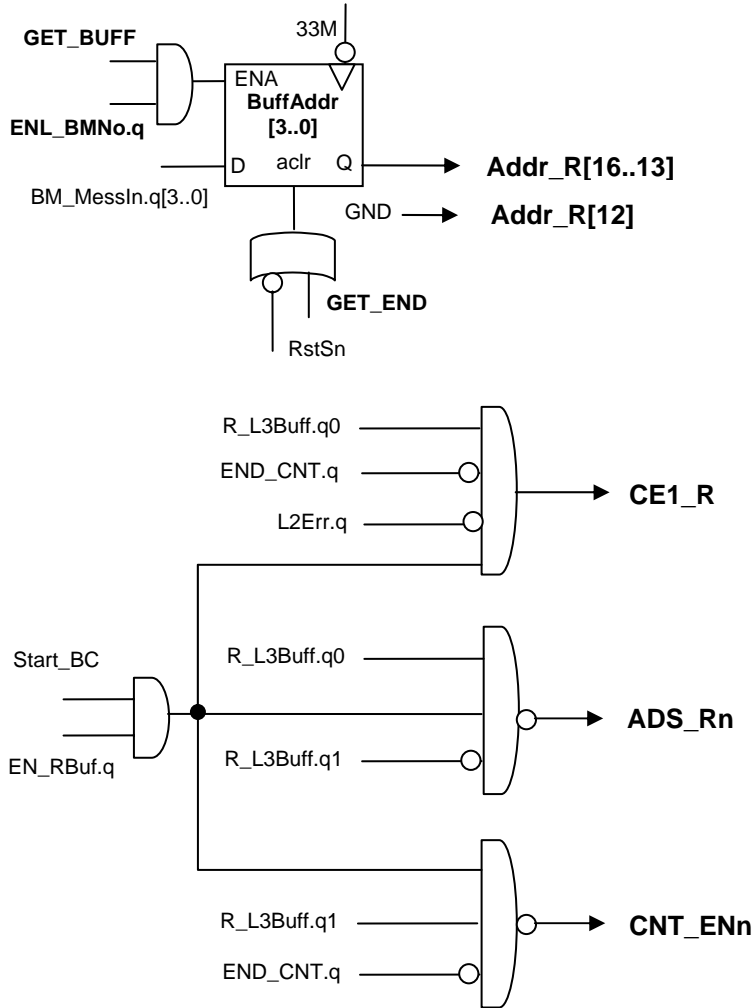
Buffer Controller: Writing to the DPRAM – Addr & Data

code version: 20-May-03
 created in: pci3_lm.tdf



Buffer Controller: Reading from the DPRAM

code version: 20-May-03
 created in: *b_ctrl.tdf*



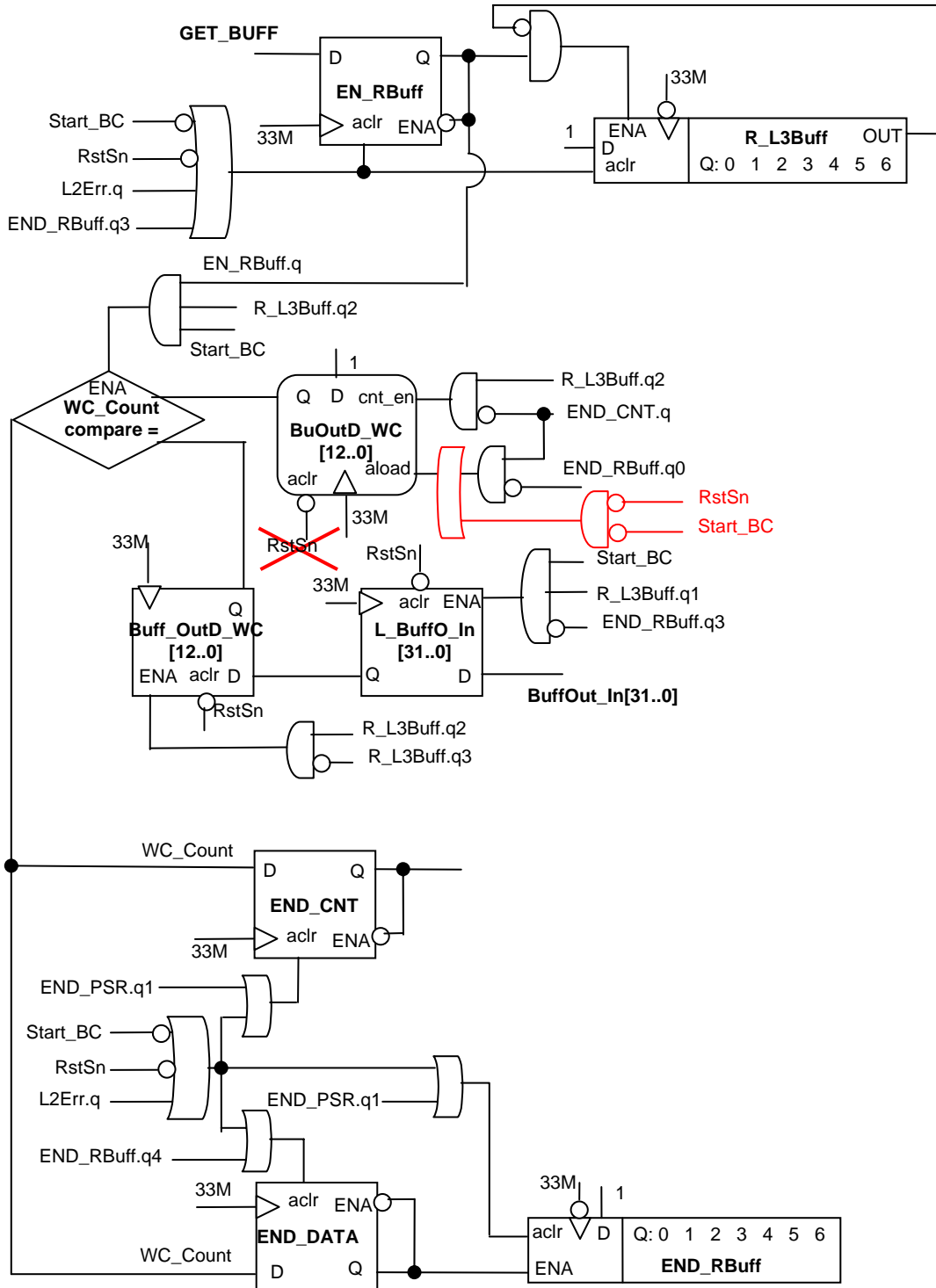
Signals for reading the DPRAM

- **Addr_R[16..0]** Address in DPRAM – upper 4 bits mark buffer boundaries
- **CE1_R** Chip enable – extends 1 clock due to DPRAM internal write delay
- **ADS_Rn** Address strobe – load first address
- **CNT_ENn** Counter enable – internal address counter

Buffer Controller: Buffer Reads – Internal Logic

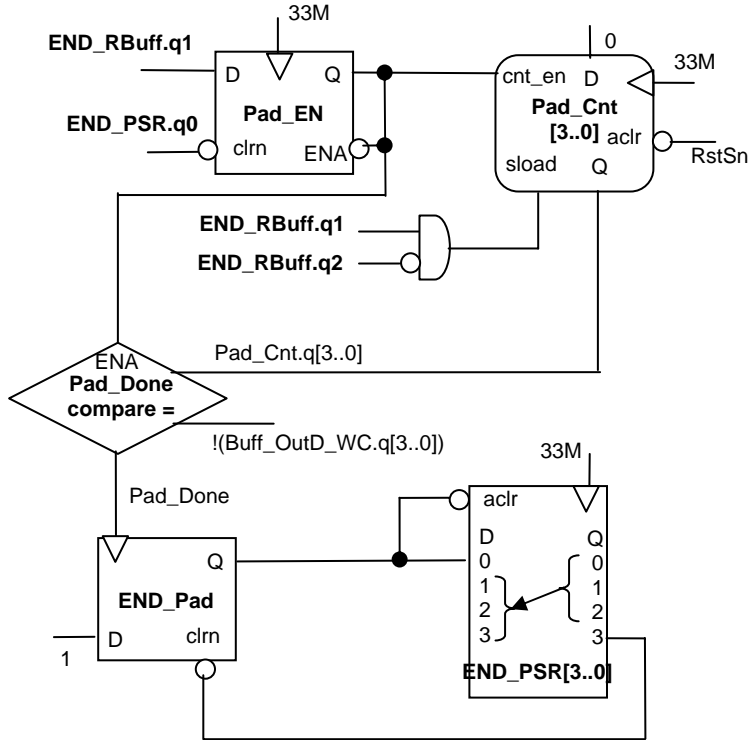
code version: 13-Jun-03 (in preparation)

created in: *b_ctrl.tdf*



Buffer Controller: Buffer Reads – Pad Generation

code version: 20-May-03
 created in: *b_ctrl.tdf*



For Block Size = 16 (pabs_bit = 4):

- $N+1 = \text{No.}(\text{data words}) + \text{Checksum} + \text{ChkSumError} = \text{No. words in Out FIFO}$
 (count from 1)
- $\text{Buff_OutD_WC} = N = \text{WC from Addr0 in Buffer}$
- $\text{L3_WC} = N+1$ round to next 16 = WC read by SBC
- $\text{L3_WC}[5..4] = \text{Buff_OutD_WC}[5..4] + 1$
 $\text{L3_WC}[3..0] = 0$
- $\text{Pad_Cnt} = \text{no. need to add to } N \text{ to get } N+1 = \text{multiple of 16}$

Buff_OutD_WC (from Buffer)				Pad_Cnt	L3_WC (to WC FIFO)		
all	[5..4]	[3..0]	! [3..0]	[3..0]	all	[5..4]	[3..0]
0	00	0000	1111	15	16	01	0000
1	00	0001	1110	14	16	01	0000
14	00	1110	0001	1	16	01	0000
15	00	1111	0000	0	16	01	0000
16	01	0000	1111	15	32	10	0000
20	01	0100	1011	11	32	10	0000

Buffer Controller: Writing to FIFO

code version: 20-May-03

created in: *b_ctrl.tdf*

