

FRC Status

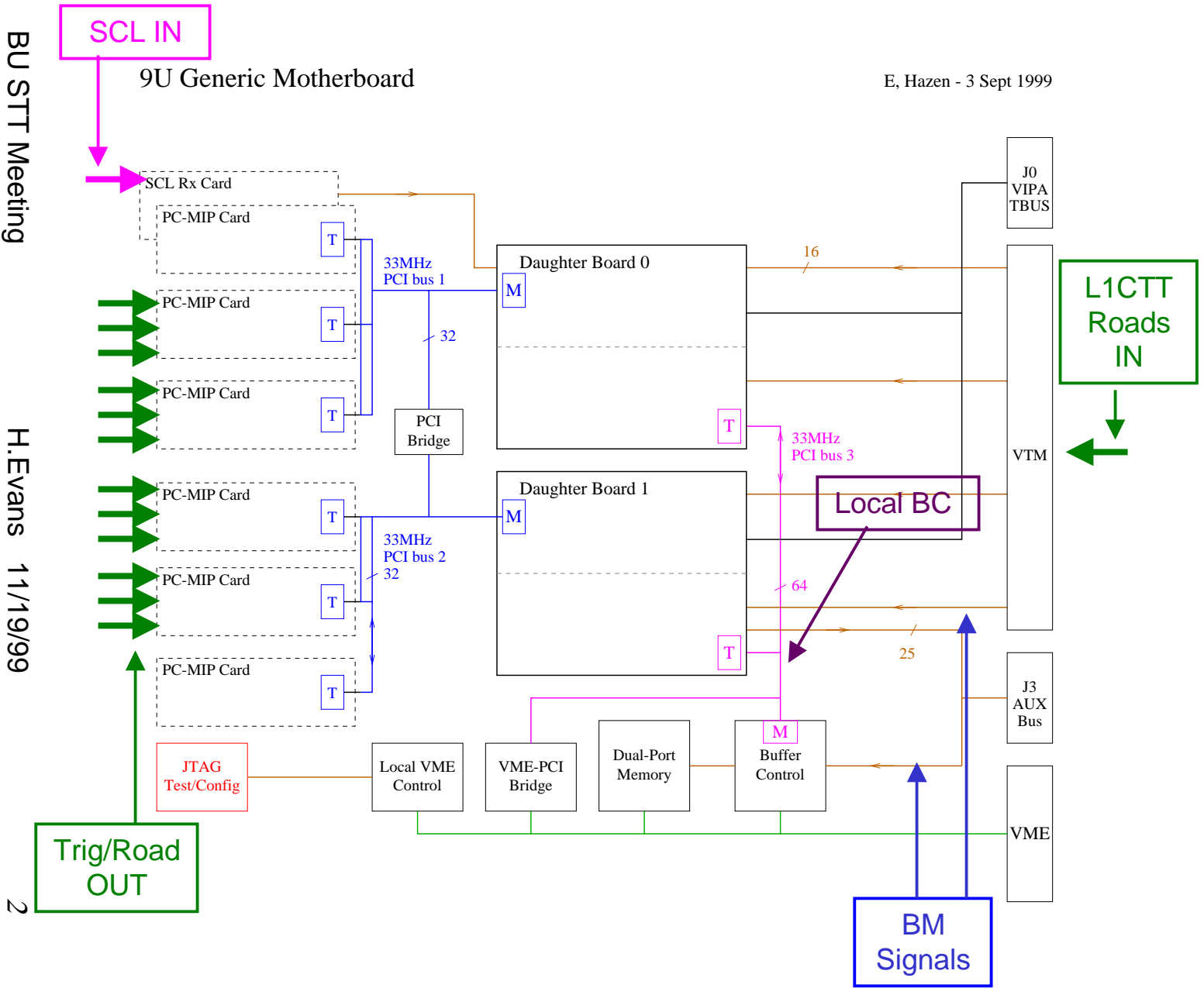
H.Evans

Columbia U.

- **Two Stages to FRC Design**
 - 1) Exact Spec's of Control Functions & I/O
 - 2) Layout Board to Accomplish These
- **Where Do We Stand**
 - Still on Stage 1) Phys.
 - Start Stage 2) before End of Year Eng.
- **Why Should You Care**
 - Comm from/to FRC impacts Design of other Boards
 - * Mainly a Stage 1) Issue
 - * Changes Possible from Injection of Reality in Stage 2)
- **Outline** (concentrate on external issues)
 - 1) What to Expect from FRC
 - 2) When to Expect It
 - 3) What to Send Back

Standard STT Board (FRC)

E, Hazen - 3 Sept 1999



BU STT Meeting

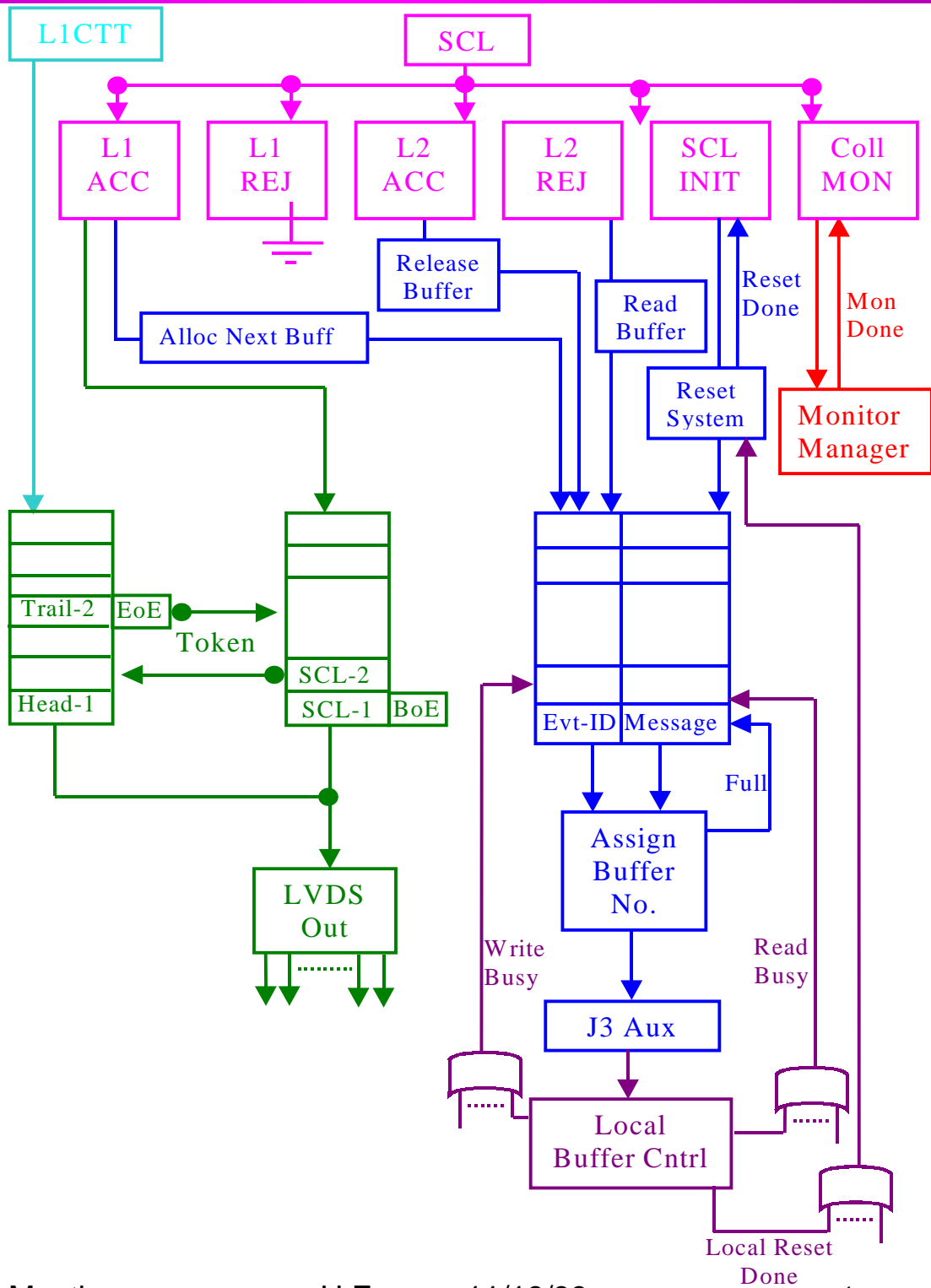
H. Evans 11/19/99

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What to Expect from FRC

- **Trigger/Road Data** **LVDS**
 - Signals Start of Event
- **Buffer Management** **Aux J3**
 - FRC BM ↔ Local BCs
 - BM: Start Transfer → VBD
 - BC: Wrd Cnt → VME-mem → VBD **VME**
DPM → fifo → VBD
 - * under control of VBD
 - Note: this might also be a good place to implement Reset/Error Signals
- **Monitoring** **VME**
 - Coordinate Transfer of Monitor Info from Boards to Bit3 MPM
 - Should it be the FRC that does this?
 - * Note: FRC receives *Collect Status* Signal from SCL

Communications Flow



When to Expect It

	Δt -min	Δt -ave	Action
L1 Decision Yes	132ns 8.4 μ s	132ns 100 μ s	SCL→FRC Data→STCs,TFCs BM→BCs (allocate)
L2 Decision Yes	? ?	100 μ s 1ms	SCL→BM BM→BCs (output)
Monitoring Collect	132ns ?	132ns ~5s	SCL→FRC FRC→Mon. Master

Trigger/Road Data Structure

- **T/R Data has 4 Components**

- 1) Trigger Info $2 \times 32\text{-bits}$
- 2) L1CTT Header $4 \times 32\text{-bits}$
- 3) Road Data $N \times 32\text{-bits}$
- 4) L1CTT Trailer $1 \times 32\text{-bits}$

- **Control Characters for T/R Data (FRC→STC,TFC)**

Bit Use	Meaning
00 Invalid	Outside of Event
01 BoE	First Word of Event
11 Data	Valid Data Word
10 EoE	Last Word of Event

⇒ Trig/Road Information needs 34 bits

- **No T/R Handshaking (STC,TFC→FRC)**

- Buffer Trig/Road Inputs
- Event ID on ALL outputs
 - * preserve synch between different sources

Trig/Road Data Format

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
(*) L1 Qualifiers								L1 Qualifiers								Trigger Info
free								free								
Turn No.								Turn No.								
BX No.								Total No. Trks (?)								
Header Length								No. of Objects								L1CTT Header
H-Form		Object Format						Object Length								
Bunch No.								Data Type								
Rotation No.								Rotation No.								
(Algorithm min ver)								(Algorithm max ver)								
Status Bits								Proc. Bits (firmware ver)								
P	N	No. Trks Pt2 (<47)						P	N	No. Trks Pt1 (<47)						
P	N	No. Trks Pt4 (<47)						P	N	No. Trks Pt3 (<47)						
S	PtBin	Ext Pt	0	0	Err Code			0	0							
Relative Φ (0-43)				0	0	D	Trk Sector Address									
...								...								
Data Type								Bunch No.								L1CTT Trailer
Longitudinal Parity								Longitudinal Parity (**)								

See M.Martin: <http://d0server1.fnal.gov/users/Protocols/protocols.htm> (ver 6.1)

(*)BoE Cntrl Bits

(**)EoE Cntl Bits

L1CTT Glossary (Abridged)

- **Trigger Info**

- L1 Qual Processing Info for Event

- **Header**

- P/N Some Trks w/ Pos/Neg Pt
- No. Ptx No. of Trks in Pt Bin x

- **Data**

- S Sign of Trk
- Pt Bin Pt Bin Number (0-3)
- Ext. Pt Bin-1 (1.5-3 GeV) A-Offset
Bin-2 (3-5 GeV) A-Offset
Bin-3 (5-10 GeV) Pt-Info
Bin-4 (10- GeV) Pt-Info
- Error Transmission Errors
- Rel Φ H-Layer Fiber Number
- D Track also sent to Adjacent Segm
- Trk Adr Address of 4.5° wedge of Trk

L1 Trigger Qualifiers

- Current understanding from Jim Linnemann (10/26/99)
 - probably can only use 16 bits

Bits	Name	Comments
00	L1NoZeroSuppress	
01	L2UnbiasedSample	
02	L2CollectStatus	Monitoring
03	L2ForcedWrite	
04	L2GlobalNeeded	<i>Don't Use</i>
05-06	L2Mu	
07-12	L2Cal	
13-15	L2PS	
16	L2STTNeeded	
17	L2TrackNeeded	
18	L2TrackShortOutput	
19	L2ImpactNeeded	
20	L2ImpactShortOutput	
xx	L1HeartBeat	

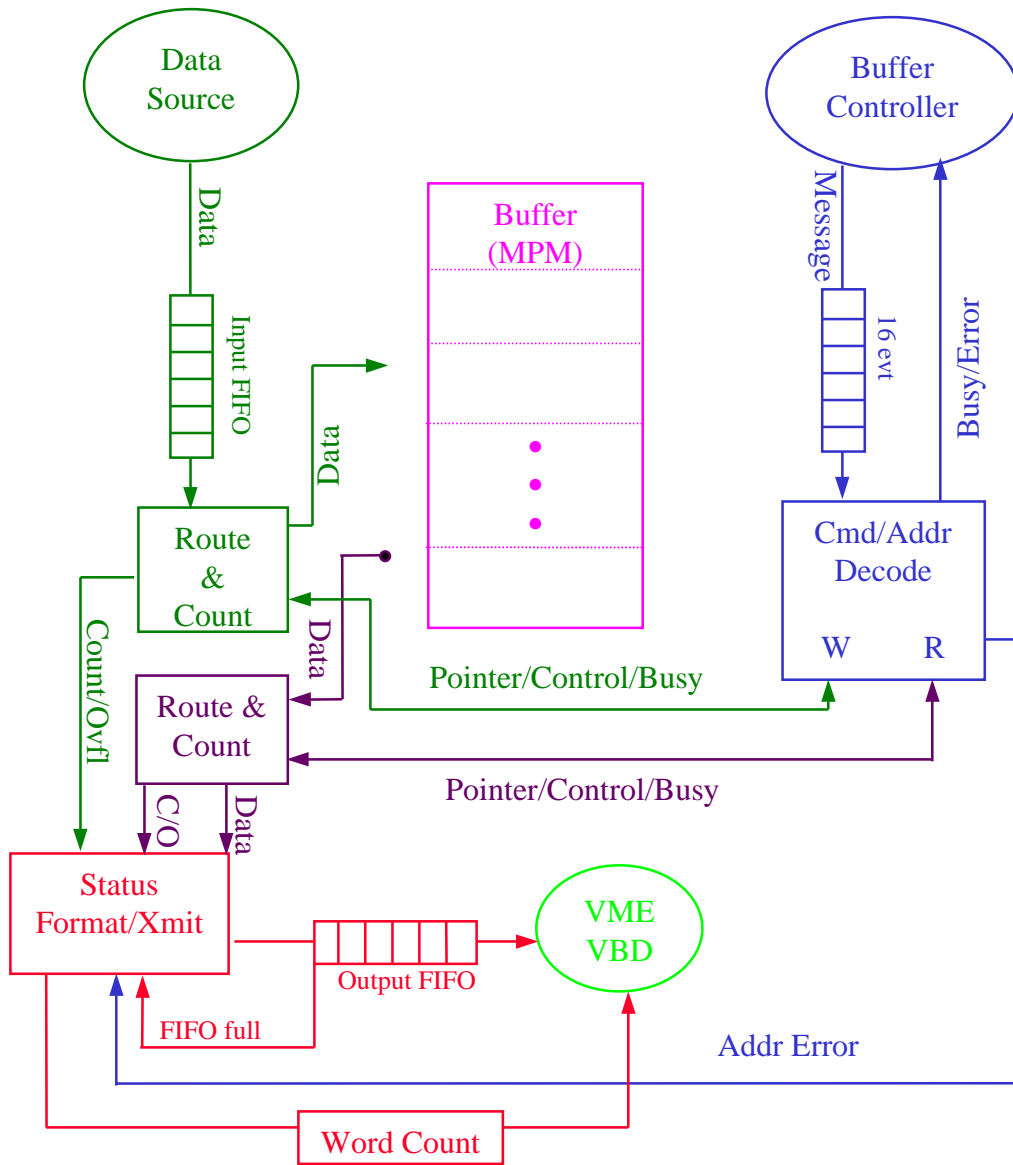
Buffer Protocol (VRB)

- **Buffer Manager (VRBC) Protocol Implemented on J3 row C**
- **12 pins Messages** (BM→Dest's):
 - Bits 11-8 Message Type
 - 7-0 Value
- **1 pin Msg Strobe**
- **10 pins Status** (Dest's →BM)
 - Open Collector TTL
 - OR of all Dest's
 - Dest's must set these Status Lines in response to Messages from FRC
- **15 pins Free**
 - Use for Error Comm (?) (Dest's→FRC)

VRB Messages & Status

No.	Name	Purpose
MESSAGES		
1	Readout Buffer No.	L1: next in buff no.
3	Bunch Crossing No.	L1: consistency
4	Scan Buffer No.	L2: VRB out buffer no.
5	Event No.	L2: event label
13	Clear Errors	clear errors - no reset
14	Reset/Restart	SCL Init (?)
STATUS		
0	Readout Busy	L1: in buffer busy
1	Scan Busy	L2: out buffer busy
2	Sync Error	Data Link Sync Error
3	Frame Error	Non-Valid Data Word
4	Identifier Error	Invalid Event ID
5	Format Error	Data Format Error
6	Controller Error	Invalid Message
7	VRB Error	Buffer Overflow

L3 Buffer Unit



SCL Init

- **SCL Init Sequence**

Command	Implementation
1) FRC Rec Init from Hub	mezzanine
2) FRC Send Init to all Card	BM→J3
3) FRC INIT_ACK to Hub	mezzanine
4) FRC Clear L1/L2_ERROR	mezzanine
5) All Receive Init from FRC	J3→BC
6) All Raise Local Busy	BC→J3
7) All Perform Init Sequence wait for all Inputs clear send Init Done signal	BC→J3
8) FRC Wait for ALL Init Dones	BM→J3
9) FRC Clear INIT_ACK	mezzanine

Monitoring

- **The \$30,000 Question - Who is the Monitor Manager ?**
 - The FRC ?
 - A Commercial VME CPU?
- **FRC**
 - + L2CollectStatus arrives on SCL as part of L1 Qualifiers
 - Entirely New Module for FRC
 - * need to make it Bus Master
- **VME CPU**
 - + Programming Simplified
 - + Could use CPU for other tasks
 - * downloading, testing, storage,....
 - Cost (depends on choice)
- **Decision Needs Understanding:**
 - Monitoring Goals
 - Difficulties of Manager Task
 - Other uses for CPU