

# FRC & L3 Buffering



**H.Evans**

**Columbia U.**

- **FRC Tasks:**

- 1) Receive/Transmit Road Data from L1CTT
- 2) Interface to SCL (trigger)
- 3) Manage L3 Buffers for STT System

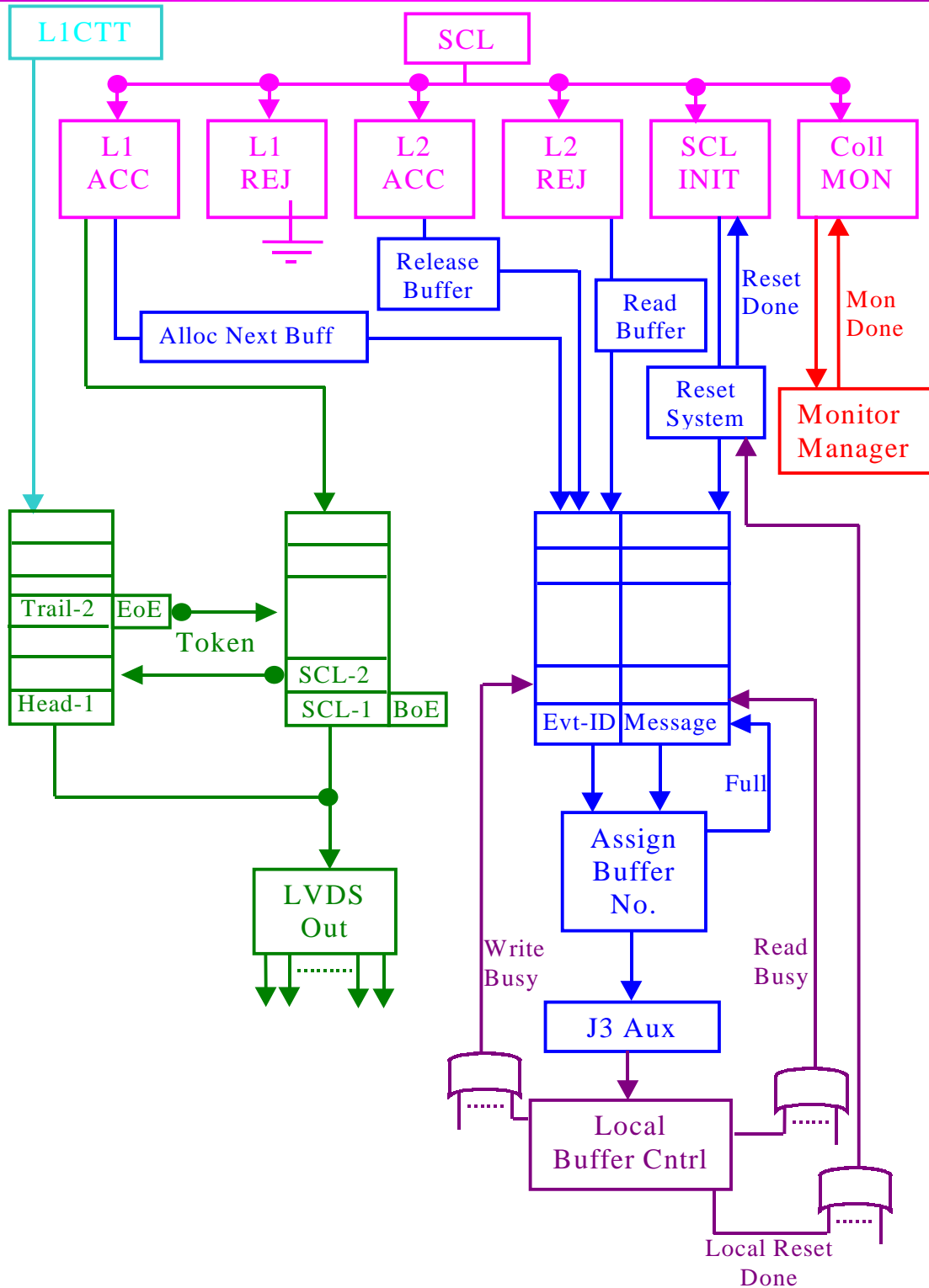
- **Two Stages to FRC Design**

- 1) Exact Spec's of Control Functions & I/O
- 2) Layout Board to Accomplish These

- **Where Do We Stand**

- Stage 1)                      **finish 3/3/00**                      **Phys.**
- Stage 2)                                                                **Eng.**

# The FRC Functionally



# FRC Communications Paths

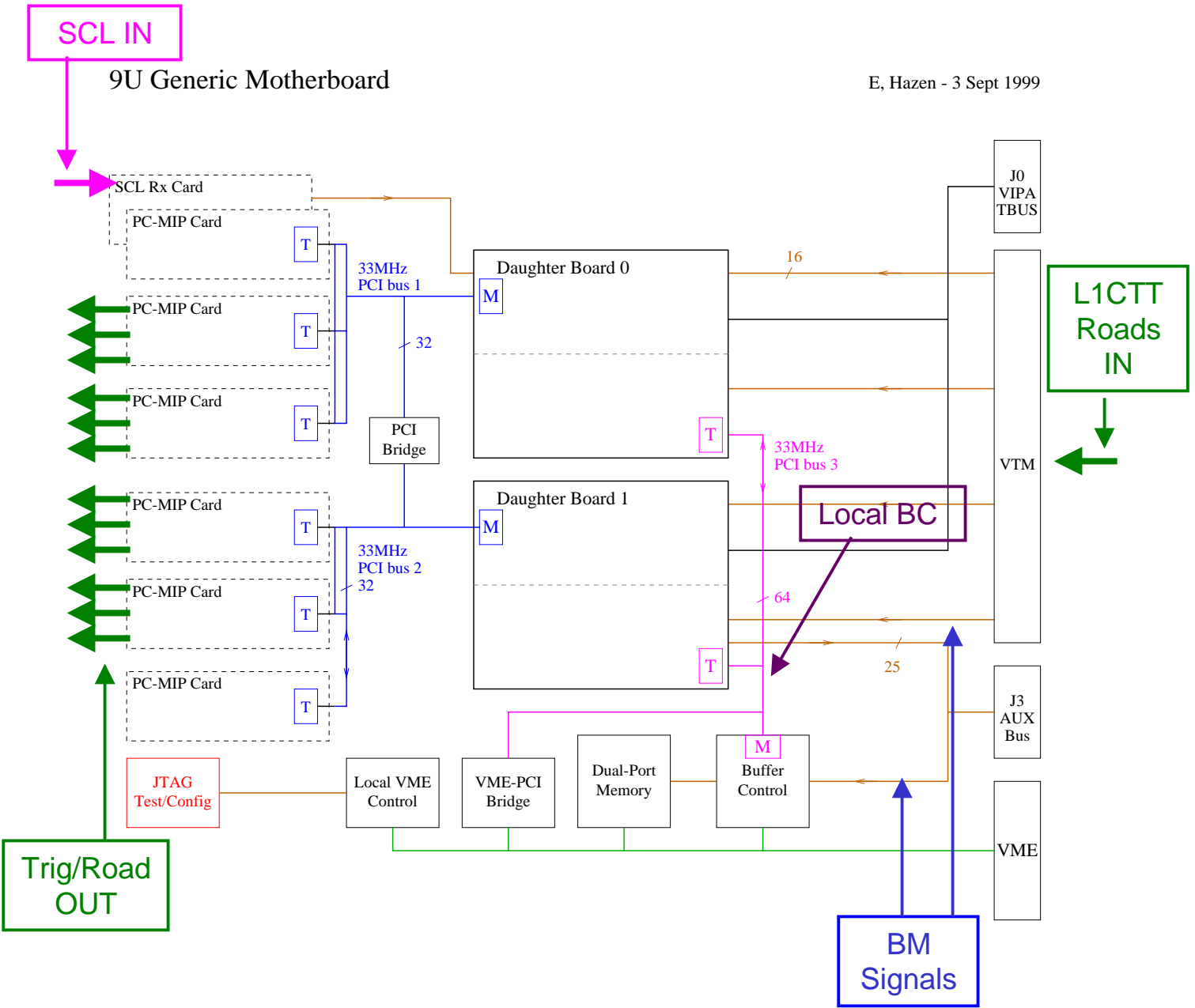
- External Communications

I/O	Data	Information	Path
I	L1CTT	Roads	Fiber→VTM
I	SCL	Trigger	SCL Mezz.
O	Trig/Road	Event Synch (trig) Roads	Pt-to-Pt LVDS → STCs, TFCs
O	Buffer Man.	Buffer No.'s	J3 (c.f. VRBC) ↔ ALL
O	System Ctrl	Init/Busy/Error	J3 (?) ↔ ALL
O	Monitoring	CollectStatus	VME→CPU
O	L3 Data	Buffers of Individ. Boards	VME→VBD

- Internal Communications

- Standard Mother/Daughter-board PCI-Bus Paths for Input/Output
- Road ↔ SCL ↔ Buffer Man ↔ FRC L3 Buff.

# Standard STT Board (FRC)



E, Hazen - 3 Sept 1999

Dec. 10, 1999

H.Evans / STT Status

# When to Expect It

- **FRC Controls STT Event Timing**
  - It is the only card in the STT that talks directly with the SCL

	$\Delta t$ -min	$\Delta t$ -ave	Action
<b>L1 Decision</b>	<b>132ns</b>	<b>132ns</b>	<b>SCL→FRC</b>
<b>Yes</b>	<b>8.4<math>\mu</math>s</b>	<b>100<math>\mu</math>s</b>	<b>Data→STCs,TFCs BM→BCs (allocate)</b>
<b>L2 Decision</b>	<b>?</b>	<b>100<math>\mu</math>s</b>	<b>SCL→BM</b>
<b>Yes</b>	<b>?</b>	<b>1ms</b>	<b>BM→BCs (output)</b>
<b>Monitoring</b>	<b>132ns</b>	<b>132ns</b>	<b>SCL→FRC</b>
<b>Collect</b>	<b>?</b>	<b>~5s</b>	<b>FRC→Mon. Master</b>

# Trigger/Road Data Structure

---

- **T/R Path has 2 Functions:**
  - 1) Pass L1CTT Info from STT → L2CTT
    - \* STT replaces L1CTT → L2CTT Path
  - 2) Distrib abridged Trigger Info → Rest of STT
    - \* All boards must have T/R Input
- **T/R Data has 4 Components**
  - 1) Trigger Info      2 × 32-bits
  - 2) L1CTT Header    4 × 32-bits
  - 3) Road Data        N × 32-bits
  - 4) L1CTT Trailer    1 × 32-bits
- **Control Characters for T/R Data (FRC→STC,TFC)**
  - Use LVDS Control Characters for Begin/End of Event
- **No T/R Handshaking (STC,TFC→FRC)**
  - Buffer Trig/Road Inputs
  - Event ID on ALL outputs

# Trig/Road Data Format

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
(*) L1 Qualifiers								L1 Qualifiers								Trigger Info
free								free								
Turn No.								Turn No.								
BX No.								Total No. Trks (?)								
Header Length								No. of Objects								L1CTT Header
H-Form		Object Format						Object Length								
Bunch No.								Data Type								
Rotation No.								Rotation No.								
(Algorithm min ver)								(Algorithm max ver)								
Status Bits								Proc. Bits (firmware ver)								
P	N	No. Trks Pt2 (<47)						P	N	No. Trks Pt1 (<47)						
P	N	No. Trks Pt4 (<47)						P	N	No. Trks Pt3 (<47)						
S	PtBin	Ext Pt	0	0	Err Code			0	0							
Relative $\Phi$ (0-43)						0	0	D	Trk Sector Address							
...								...								
Data Type								Bunch No.								L1CTT Trailer
Longitudinal Parity								Longitudinal Parity (**)								

See M.Martin: <http://d0server1.fnal.gov/users/Protocols/protocols.htm> (ver 6.1)

(\*)BoE Cntrl Bits

(\*\*)EoE Cntl Bits

# Buffer Manager

---

---

- **Buffer Manager Tasks**
  - Listen to SCL
  - Keep List of Write/Read Buffer No.'s for Entire System
  - Broadcast next Write/Read Buffer No. based on SCL Info
  - Receive Status Info from All Boards
  - Signal VBD to begin Reading Buffers
  - *Deal w/ Init/Error/Busy Conditions ?*
  - *Send CollectStatus to Monitor CPU ?*
- **Steal most of this from the VRBC**
  - Implemented on row C of J3
  - **12 pins Messages** **BM→Dest's**
    - \* (buffer no. for write/read)
  - **1 pin Msg Strobe**
  - **10 pins Status** **Dest's→BM**
    - \* (OR of all Dest's)
  - **A few free pins for other uses**

# VRB Messages & Status

No.	Name	Purpose
<b>MESSAGES</b>		
1	Readout Buffer No.	L1: next in buff no.
3	Bunch Crossing No.	L1: consistency
4	Scan Buffer No.	L2: VRB out buffer no.
5	Event No.	L2: event label
13	Clear Errors	clear errors - no reset
14	Reset/Restart	SCL Init (?)
<b>STATUS</b>		
0	Readout Busy	L1: in buffer busy
1	Scan Busy	L2: out buffer busy
2	Sync Error	Data Link Sync Error
3	Frame Error	Non-Valid Data Word
4	Identifier Error	Invalid Event ID
5	Format Error	Data Format Error
6	Controller Error	Invalid Message
7	VRB Error	Buffer Overflow

# L3 Buffer Unit

