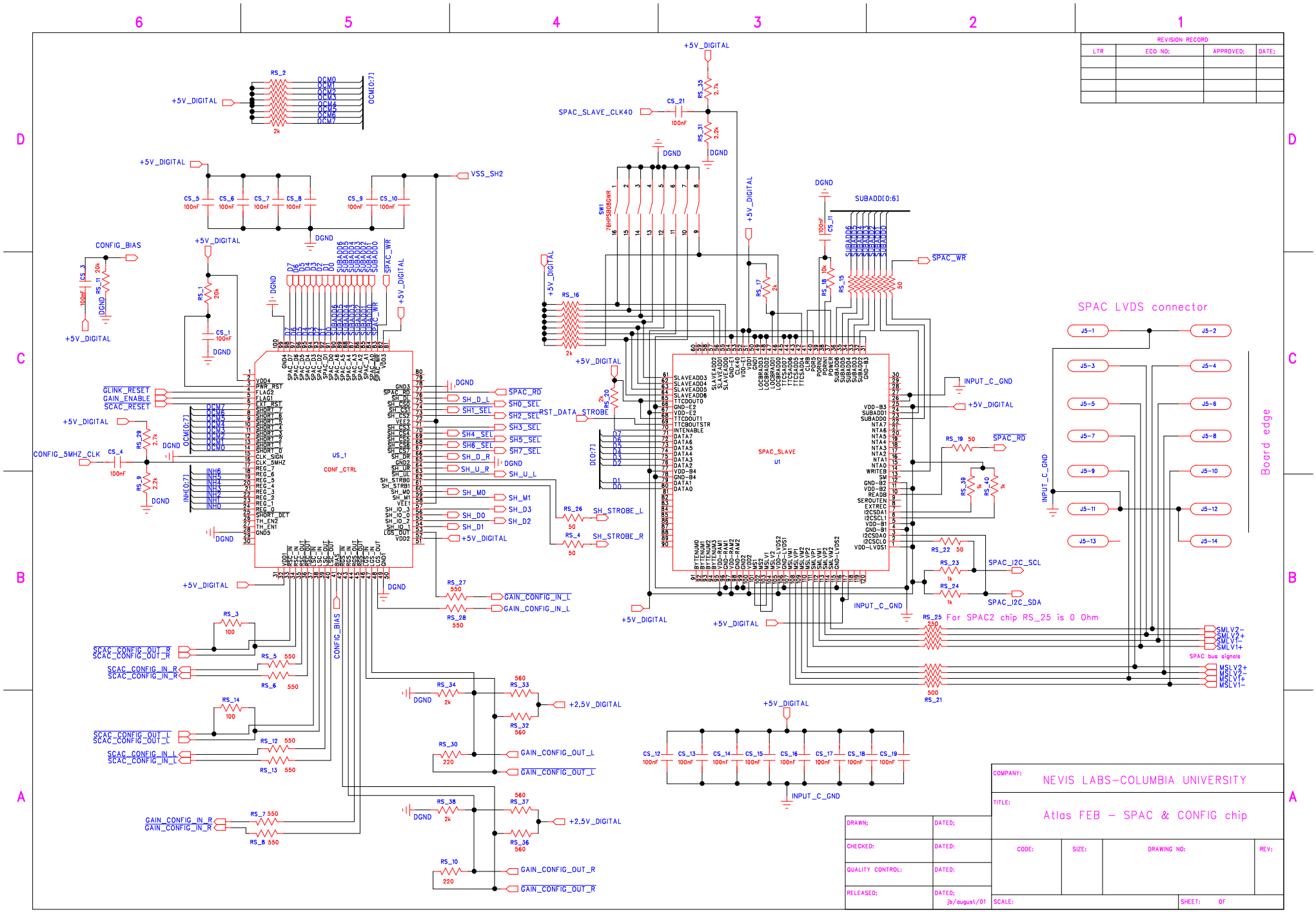

REVISION RECORD
LTR
ECO NO:
APPROVED:
DATE:
SPAC LVDS connector
Board edge
SPAC_SLAVE
U1
US_1
CONF_CTRL
SPAC_SLAVE_CLK40
SUBADD[0:6]
SPAC_WR
SPAC_RD
SPAC_I2C_SCL
SPAC_I2C_SDA
INPUT_C_GND
+5V_DIGITAL
DGND
VSS_SH2
CONFIG_BIAS
GLINK_RESET
GAIN_ENABLE
SCAC_RESET
CONFIG_5MHZ_CLK
RST_DATA_STROBE
SH_STROBE_L
SH_STROBE_R
GAIN_CONFIG_IN_L
GAIN_CONFIG_IN_R
GAIN_CONFIG_OUT_L
GAIN_CONFIG_OUT_R
SCAC_CONFIG_OUT_R
SCAC_CONFIG_IN_R
SCAC_CONFIG_OUT_L
SCAC_CONFIG_IN_L
+2.5V_DIGITAL
For SPAC2 chip RS_25 is 0 Ohm
SPAC bus signals
SMLV2-
SMLV2+
SMLV1-
SMLV1+
MSLV2+
MSLV2-
MSLV1+
MSLV1-
COMPANY:
NEVIS LABS-COLUMBIA UNIVERSITY
TITLE:
Atlas FEB - SPAC & CONFIG chip
DRAWN:
DATED:
CHECKED:
DATED:
QUALITY CONTROL:
DATED:
RELEASED:
DATED:
jb/august/01
CODE:
SIZE:
DRAWING NO:
REV:
SCALE:
SHEET: OF