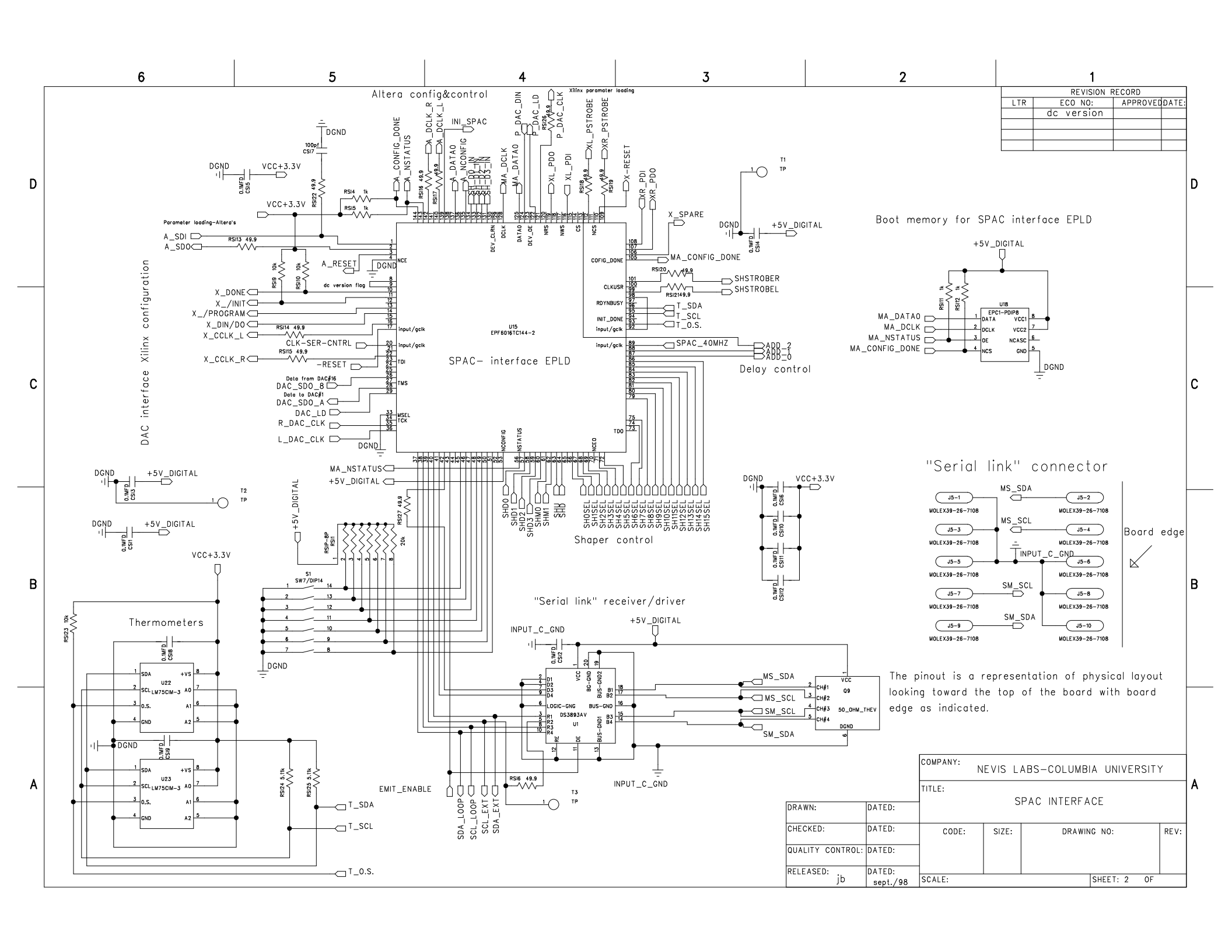
Altera config&control
Xilinx parameter loading
DAC interface Xilinx configuration
SPAC- interface EPLD
U15
EPF6016TC144-2
Boot memory for SPAC interface EPLD
U18
EPC1-PDIP8
Delay control
Shaper control
"Serial link" receiver/driver
"Serial link" connector
Thermometers
U22
LM75CIM-3
U23
LM75CIM-3
S1
SW7/DIP14
U1
DS3893AV
Q9
50_OHM_THEV
Board edge
The pinout is a representation of physical layout looking toward the top of the board with board edge as indicated.
REVISION RECORD
LTR
ECO NO:
APPROVED
DATE:
dc version
COMPANY:
NEVIS LABS-COLUMBIA UNIVERSITY
TITLE:
SPAC INTERFACE
DRAWN:
DATED:
CHECKED:
QUALITY CONTROL:
RELEASED:
jb
sept./98
CODE:
SIZE:
DRAWING NO:
REV:
SCALE:
SHEET: 2 OF