ATL-AL-EN-0009

Design of the ATLAS LAr Front End Board

1 Front end board requirements and specifications

As described in the TDR of the liquid argon (LAr) calorimeter[1], the front end boards (FEBs) contain the electronics for amplifying, shaping, sampling, pipelining, and digitizing the liquid argon (LAr) calorimeter signals. The FEB electronics must handle the signal dynamic range of about 16 bits without contributing more than 0.2% to the constant term of the energy resolution. The coherent noise per channel must be kept below 3 MeV. The FEB must store the calorimeter signals during the Level 1 trigger latency of up to 2.5 μs, read out typically five samples per channel for each Level 1 trigger, and provide virtually dead-timeless operation at the maximum Level 1 trigger rate of 75 kHz. In addition, the FEBs must perform the first step of summing in the formation of the Level 1 analog trigger tower signals.

In addition to these performance requirements, the FEB design must provide high channel density and low power and reasonable cost. The design provides 128 channels per FEB, with an estimated power consumption of approximately 0.7 W per channel. The FEB placement in crates on the detector requires tolerance to 100 kRad of ionizing radiation and to 5×10^{13} n/cm^2, over 10 years of LHC operation. Finally, the limited access to the FEBs places stringent demands on reliability and fault tolerance.

2 FEB design considerations

On the FEB, the calorimeter signals are received, amplified, split into three gain scales, and shaped with a bipolar shaping function. The shaped signals are then sampled at the bunch crossing frequency of 40 MHz, with the samples stored in analog form in switched-capacitor array (SCA) analog pipelines during the Level 1 trigger latency. Upon receipt of a Level 1 trigger accept, the train of samples are read from the SCA and digitized by a 12-bit ADC. A gain selection algorithm is applied that guarantees that all samples for a given channel and given event are digitized using the same gain scale, in order to reduce possible systematic effects. The digitized samples are formatted and then transmitted off-detector to the Read Out Driver (ROD) modules for processing.

A simulation, incorporating performances measured in the test beam with several prototype read-out systems, was performed [2] to determine the influence of the read-out electronics, including quantization error, on the calorimeter energy measurement. Based on these studies, it was decided to deal with the dynamic range with three overlapping, linear gain scales, with gains of approximately 1, 10, and 100. Figure 1 shows the results for such a

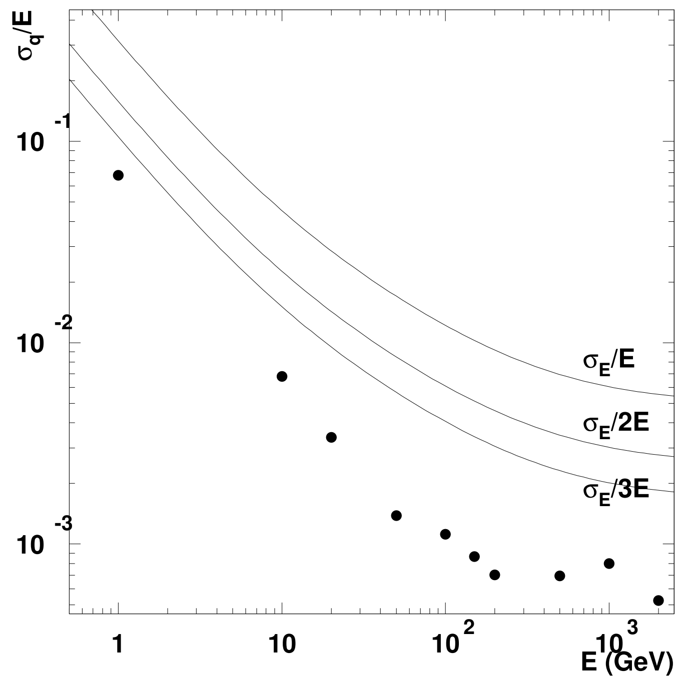

Figure 1: Comparison of the quantization noise of a three-gain system with gains of 1, 10, 100 to the calorimeter resolution in presence of 200 μV coherent noise, for a luminosity of 1.0×10^{34} cm^{-2}s^{-1}.

simulation. The upper curve shows the intrinsic calorimeter energy resolution versus energy, including the sampling and constant terms as well as thermal noise, while the lower curves show this same curve divided by factors of two and three respectively. The points show the error introduced by the read-out electronics, assuming 200 μV of coherent noise and using a 12-bit ADC with a resolution of 0.5 LSB. They are well below the intrinsic calorimeter resolution over the entire energy range. A three-gain system thus provides some immunity against coherent noise which would enter the system downstream of the shaper output.

The deposited energy and time of deposition will normally be calculated by applying an optimal filter algorithm to five samples placed around the peak. However, it should be possible to guarantee that one of the samples lies within $\pm$ 2 ns of the peak of the pulse (at least for cells containing most of the energy). This is possible, even with a single "phase" of the 40 MHz clock per FEB, since the mapping of calorimeter cells onto FEBs is done such that any given FEB contains channels from a single depth segment of the calorimeter. This, along with the cabling scheme, implies that all signals within one FEB will have a relative timing which is quite closely matched.

The FEB should be designed to be used for all parts of the LAr calorimeter system, including EM barrel and endcaps, hadronic endcaps (HEC), and the forward calorimeters. Those parts of the readout which are specific to a particular calorimeter subsystem, namely the preamps and Level 1 layer sums, are designed as plug-in modules so that the same FEB board can be used for the entire LAr readout.

3 Module 0 FEB Implementation

The Module 0 FEB is designed to resemble, as much as possible within the time constraints set by the Module 0 testbeam schedule, the final FEB design. The Module 0 FEB has the final physical dimensions and channel density, with 128 channels per board of dimensions 490 mm $\times$ 409.5 mm. The full analog signal processing chain is implemented using prototypes of the final preamps, shapers and analog pipelines. The digitization and readout rates match the ATLAS specifications, and fully support readout with a 75 kHz Level 1 rate with minimal deadtime.

3.1 General layout of the Module 0 FEB

Figure 2 shows a functional block diagram of the Module 0 FEB. The block diagram for the HEC, which uses cryogenic GaAs preamplifiers in the liquid argon, looks similar, but with the warm preamplifiers replaced by hybrids which provide signal inversion, pole-zero compensation and additional shaping in order to match the rest of the readout chain.

The calorimeter signals are received and amplified by four-channel plug-in preamplifier hybrids. The preamplifier outputs are connected to a four-channel, three-gain shaper chip which amplifies and splits each signal into three gain scales, and applies the bipolar shaping function to each scale. In addition, the shaper also sums the four channels as the first level of summing in the formation of the analog Level 1 trigger sums. Each shaper chip is followed by a four-channel SCA chip which samples the shaped signals at 40 MHz and stores the samples in analog form during the Level 1 trigger latency. Upon receipt of a Level 1 trigger, typically 5 samples are extracted from the SCA and digitized with a 12-bit commercial ADC, with one ADC servicing 8 calorimeter channels (i.e. 2 SCA chips). The "Output Control" FPGAs choose the optimal gain to be digitized for each channel, and format the data for transmission to the ROD. The SCA controller performs the address bookkeeping for the analog memories, as well as providing the TTC interface. A "SPAC" link performs the serial downloading and readback of control data for configuring the FEB.

The Module 0 FEB is realized as a 10-layer printed circuit board (PCB). Active components are mounted on both sides of the PCB in order to achieve the desired density of 128 channels per FEB. As suggested in the block diagram, the general topology of the FEB layout moves progressively from the sensitive analog electronics to the digital portion of the board, in order to minimize coupling. Each set of components is mounted in a single row across the FEB (along the z direction in ATLAS), and the rows of different components do not overlap. As one moves in the radial direction in ATLAS across the FEB, one encounters the row of preamplifiers, then shapers, then SCAs, then ADCs, then digital logic, and finally the digital links. This spatial separation reduces noise coupling into the analog electronics, and also allows the use of segmented ground and power planes.

Great care must be taken, in such a high-density environment, to carefully minimize noise injected into the analog measurement by the surrounding digital logic. The preamplifiers are enclosed in a dedicated Faraday shield. In addition, in order to provide common-mode noise rejection, the preamplifiers are AC-coupled to the shaper inputs, and differential connections are made between the shapers and analog pipelines, and between the pipelines and ADCs. As will be discussed later, these efforts have succeeded in achieving a noise level on the FEB which is dominated by the preamplifier noise.

A brief discussion of the various functionalities is presented below. More details of the

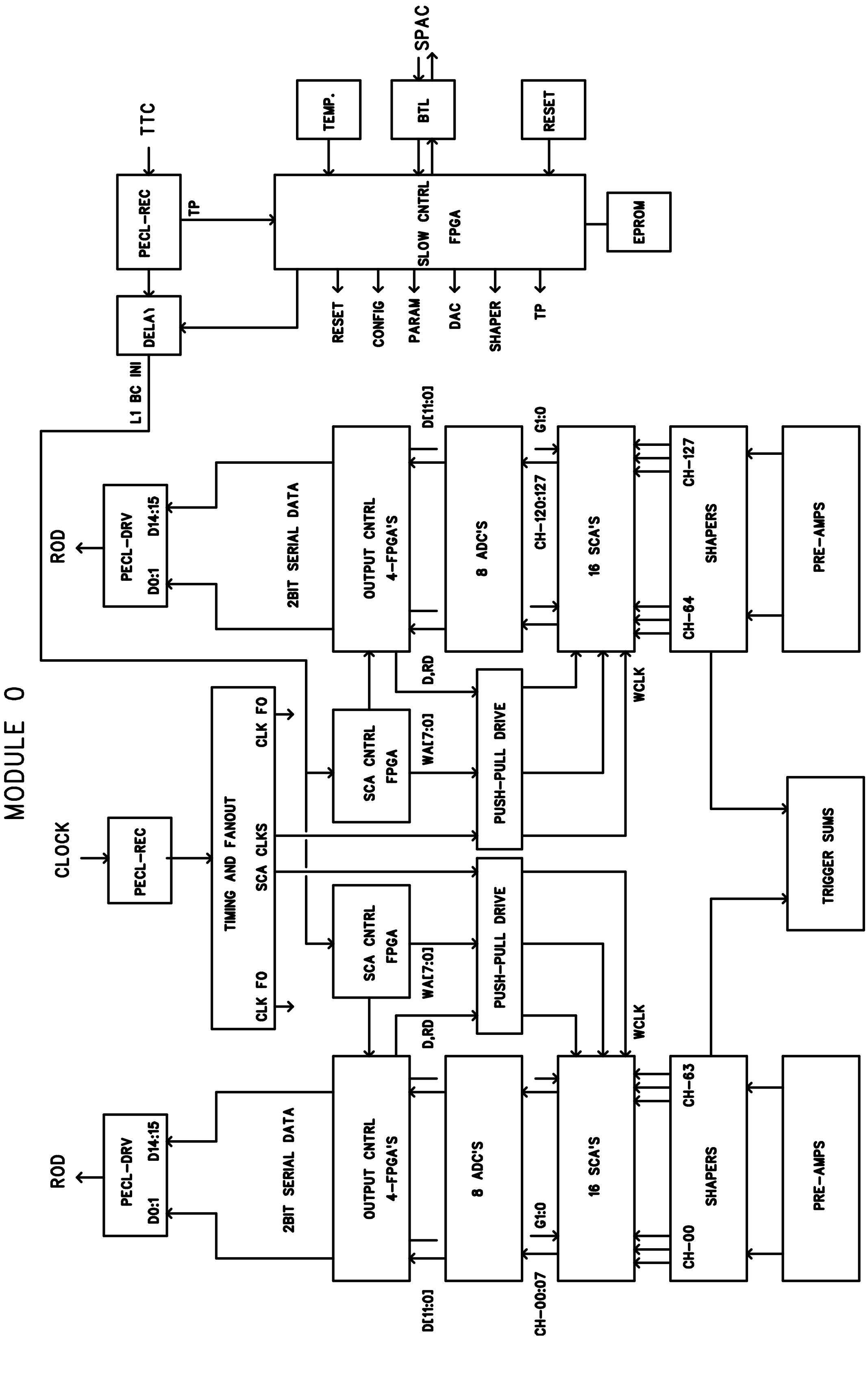

Figure 2: Block diagram showing the functionality of the Module 0 FEB.

circuitry of each block can be found in the schematics, which are available electronically via WWW at

`http://nevis1.nevis.columbia.edu/~atlas/electronics/schematics.html.`

3.2 Signal inputs

The raw calorimeter signals arrive through the front end crate baseplane on two of the three 96-pin DIN connectors on the signal input side of the FEB. The connectors used were chosen to mate through the baseplane with the warm cables coming from the feedthroughs, and to satisfy the 2 cm pitch required between boards in the Front End Crate. The outer two rows of 32 pins each are used for the 64 signals on each connector, with the inner row of pins used for ground connections.

The quality of the ground connection is very important for the avoidance of ground motion between the FEB and baseplane, which could be seen at the preamp inputs and amplified, contributing to coherent noise in the readout. The connectors do not provide a sufficiently high quality ground connection, due in part to the rather large inductance of the connector pins and to the assignment of one ground pin for every two signal pins. In addition, the plastic connector does not provide a shield connection which would allow a separation between signal return and ground. To improve this, a custom shielding and grounding arrangement has been designed and produced by Instrument Specialties, Incorporated. Measurements with prototypes have demonstrated that the specification of coherent noise per channel of less than 5% of the white noise can be met with these shields. The Module 0 FEBs and front end crates are being equipped with the shields for use in the 1999 testbeam runs.

3.3 Analog signal processing chain

The fundamental FEB building block corresponds to a four-channel "slice" of the analog signal processing chain, including preamp, shaper and analog pipeline (for more details, see the "Slice 0" schematic). The four-channel format of these custom components have been matched to allow a tight, hierarchical design to be used for the FEB, in order to achieve the required density and maintain good noise performance. The Slice 0 components are mounted on the bottom of the PCB, while the "Slice 1" components are mounted above them on the top side. Together, they share the same ADC. The sides are distinguished by the state of the "Parity" bit which informs the SCA chip whether it is the first or second to be digitized.

From the input connectors, the signals are routed to the inputs of the four-channel preamplifier hybrids (for more details, see the note on the preamps), which are mounted on both sides of the FEB. The signals are routed on two inner layers, each surrounded by ground planes, to avoid pick-up. In addition, the use of two layers allows the routing without signal crossings to avoid cross-talk. The preamplifiers are enclosed in their own RF-gasketed Faraday shields to provide additional noise immunity.

The preamp outputs are AC-coupled and routed directly to the inputs of the four-channel shaper ASICs, which split the signal into three gains and provide fast bipolar shaping (see the note on the shapers for more details). In addition, the shapers provide analog sums of the four channels on a single chip as the first stage of formation of the Level 1 trigger sums.

The 12 shaper signal outputs (4 channels times 3 gains) are DC-coupled directly to the inputs of the SCA analog pipeline chip. The shaper reference output is coupled to the SCA reference pipelines (see the next section) in order to provide a pseudo-differential connection for the cancellation of common mode noise. DC-coupling between the shapers and SCAs is important to remove the need to apply an event-by-event baseline correction, which would be necessary in the high-rate environment of the LHC since zero-area balance in the shaper outputs is lost in the case of saturated signals. While a baseline correction can be implemented using the digital filtering of the multiple samples, it would result in an effective increase in noise. The DC-coupling, however, complicates the operation of the SCAs by imposing a signal reference level of 0 V. The SCA chips must therefore be operated with offset power supplies of +3.3V and -1.7V. With such a set-up, the signal voltage range is restricted to +2.5 V for the positive lobe and -0.9 V for the negative lobe. A measurement of the negative lobe is important in order to be able to deal with signals present on pile-up signals from previous bunch crossings, and also in order to be able to measure the entire bipolar pulse shape for monitoring purposes.

Control buses for setting the shaper trigger switches, and for delivering the Write and Read addresses and clocks to the SCA chip, are also shown on the Slice 0 schematic. The SCA is produced in two versions, one the mirror image of the other, so that chips mounted on opposite sides of the PCB are able to share vias for the large number of control connections. This is necessary to achieve the routing density required on the FEB.

3.4 Analog memory

One SCA analog memory chip handles the signals for all three gains of four different calorimeter channels, and also provides a differential reference pipeline for each channel. It therefore contains a total of 16 pipeline channels. The reference channels are connected to the reference output of the shaper chip. The use of a single SCA for four channels provides an ideal match to the four-channel three-gain shaper chip (which in turn matches the four-channel preamplifier hybrid). This allows a compact layout with short signal traces, and avoids potential problems in cross-talk and signal trace loads which could result if a more complex routing of signal traces over several signal layers were necessary.

One pipeline channel, depicted in figure 3, comprises an input signal buffer as well as a source follower on the signal return, an array of 144 analog storage cells, and a read-out operational amplifier. The input buffer serves several functions, including limiting the input signal voltage, reducing the drive requirement of the shaper output stage, and decreasing the level of cross-talk by buffering the flow of signal currents on and off the chip. Similarly, the source follower on the signal return line, which is common to all channels, reduces the cross-talk by limiting the current, and therefore voltage drop, in the return line by redirecting these currents to the power rails.

Each storage cell contains an approximately 1 pF capacitor and two sets of switches; the write switches connect the signal voltage across the capacitor during a write operation, while the read switches connect the capacitor across the read operational amplifier during a read operation. The dynamic range of SCA analog memories is limited mainly by systematic noise introduced by clock feedthrough during the opening and closing of the various switches. The basic cell architecture depicted in 3, with two CMOS and two NMOS switches, has been carefully optimized to minimize clock feedthrough. The reference pipeline plays a key role in providing the symmetry necessary to allow cancellation of most common mode and address-induced noise. Attention has been paid to reduce the noise injected into the analog measurement due to the digital address and control lines. All control lines are received differentially with low-voltage swings and level-shifted on the SCA chip. In addition, the

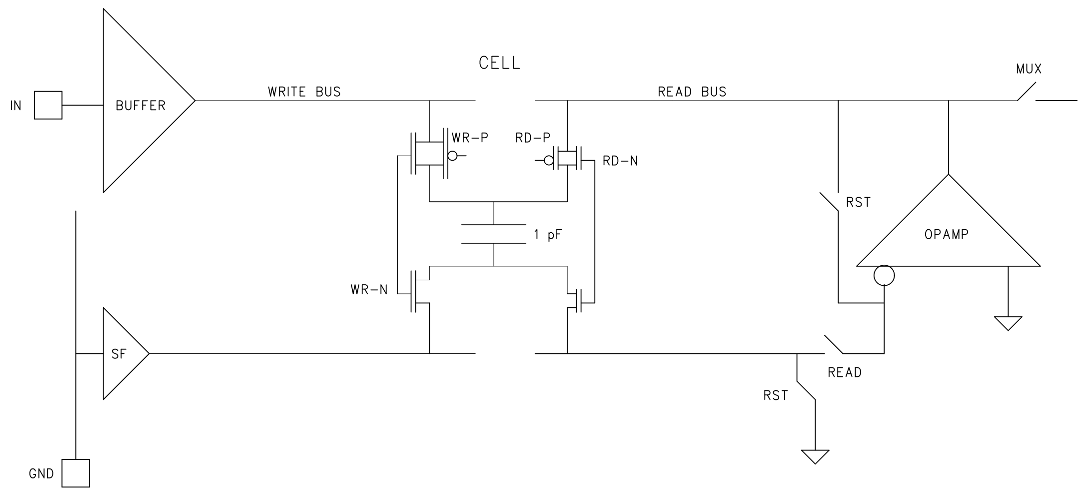

Figure 3: Schematic diagram for one SCA pipeline channel. Only one of 144 storage cells is shown.

control logic itself has been optimized to reduce the number of logic level transitions. Details of the SCA performance, in both the HP and DMILL versions, are provided in a separate note.

The SCA is designed for random access to any cell, with the read and write addresses generated by a separate SCA Controller chip and subsequently decoded on the SCA chip. Buffering of the data from Level 1 accepts is accomplished by the SCA Controller transferring the addresses of the relevant samples to a FIFO of samples awaiting digitization, thereby preventing them from being overwritten. The read and write switches are controlled independently by separate buses. Thus, while one sample is being read out, it is possible to continue to sample the input voltage and write to other cells in the pipeline. This simultaneous read and write operation allows operation at 75 kHz Level 1 trigger rates with minimal deadtime.

3.5 Digitization and gain selection

A pair of SCA chips (ie. a total of 8 channels), mounted on opposite sides of the PCB, share a single 12 bit ADC. The pseudo-differential SCA outputs are added with an op-amp, which also allows the overall DC offset to be set by a programmable dual-DAC chip before input to the 12-bit ADC (for more details, see the "ADC & Control" schematic). The ADCs are operated with a continuous 5 MHz clock which is derived from the 40 MHz input clock.

The data bits from two ADCs are connected through series resistors (to reduce noise) to an ALTERA FPGA. To reduce the required rate of digitization and the amount of data to be read out, only one gain scale will usually be digitized per channel and event. Reconstructing the pulse height for a given channel from samples digitized on different gain scales would be susceptible to systematic effects such as those due to different shaping times on different scales. To avoid this, a gain selection algorithm is applied which guarantees that all samples

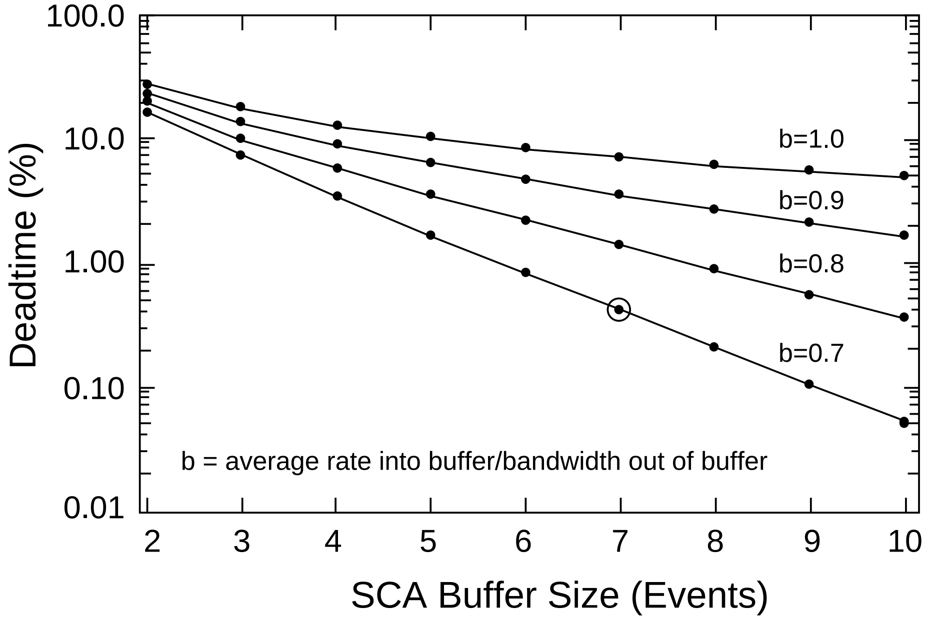

Figure 4: Deadtime versus SCA buffer size in events. For a mean Level 1 trigger rate of 75 kHz, the read-out and trigger rates correspond a value of b of about 0.7 (see the text for more details). Therefore a 144-cell deep pipeline, with a 7-event buffer, will yield a dead time below 0.5rate of 100 kHz, this rises to a few per cent.

for a given channel and event are digitized using the same scale. The ALTERA FPGA is responsible for performing the channel-by-channel gain selection by controlling the gain selection lines driven via differential LVDS connections back to the 4 SCA chips to which it is connected. Using an FPGA allows a variety of gain selection algorithms to be investigated. In ATLAS-style running, one would first digitize the sample near the peak on the Medium gain. The ALTERA then compares this value with two 12-bit thresholds which are downloaded individually for each channel, in order to choose the optimal gain for that event. All samples are then digitized for this channel using the selected gain scale. This algorithm implies the digitization of six samples per channel if five are finally required, since the original peak testing sample is not used in the final processing. With one ADC per 8 channels, the time required to digitize a single event is be 9.45 μs, yielding a maximum event digitization rate of 105.8 kHz. The average Level 1 trigger rate, on the other hand, will be limited to 75 kHz initially (later upgradeable to 100 kHz). The ratio of the average rate into the SCA event buffer divided by the maximum output rate will thus be b = 75/105.8. With this value of b and a 144-cell SCA which allows a seven event buffer, the dead time introduced by the finite SCA buffer size will be below 0.5% (see figure 4).

For inter-calibration or testing, it is possible (by downloading parameters to the ALTERA chips through the SPAC serial bus) to digitize multiple gain scales for all channels (albeit at a slower trigger rate), or to "force" the selection to any particular gain scale for any channel.

It is also possible to digitize up to 32 samples per channel, in order to digitize and read out the entire waveform. This allows a measurement of the drift-time, which can be used to monitor temperature and other variations which would contribute to the constant term in the energy resolution.

The ALTERA also formats the data for transmission to the miniROD using differential PECL levels, according to the format described in [3]. The ALTERA inserts into the ADC data stream the header, control words, and trailer. Some of the control information, such as the Bunch Crossing Number and the SCA addresses, is transmitted serially to the ALTERA's from the Xilinx SCA Controller which interfaces with the TTC and performs the address bookkeeping (see the next section). The ALTERA's also calculate and insert parity bits into each 16-bit data word they produce, to allow single-bit data transmission errors to be detected at the miniROD.

3.6 TTC interface and SCA control

The SCA analog pipelines are controlled by the on-board SCA Controller, implemented as a Xilinx FPGA. The SCA Controller is responsible for generating the Write and Read addresses and other control signals for the SCA chips, handshaking with the gain selection ALTERA FPGA chips, interfacing with the Level 1 trigger, providing the local Bunch Crossing Counter, etc. More details of the Controller functionality and programmability can be found in a separate note, while details of the implementation of the two SCA Controllers in the Module 0 FEB can be found in the "TTC& Xilinx" schematic.

Each Xilinx FPGA controls 64 of the channels on the FEB. Having two controllers per Module 0 FEB maps naturally onto the board topology which includes, for example, two separate connectors for the data output. In this way, the two sets of 64 channels can operate essentially independently of each other. In addition to increasing the system reliability, this allows the possibility to operate the two halves of the board with different pipeline addresses. This flexibility gives an additional handle on determining, and minimizing, the noise induced by the address transitions being transmitted over the FEB.

The density of the FEB requires that the SCAs for each set of 64 channels receive their control signals via a bus (see the SCA Control schematic for more details). The control bus has been carefully simulated to provide low signal distortion and good timing. To minimize noise, all SCA control signals are transmitted differentially with low voltage swings, and the control bus has been routed on an inner layer of the FEB surrounded by ground planes. In addition, an algorithm is applied which keeps, as much as possible, the cell addresses in numerical order. Thus, once a cell has been digitized and is available again, it is inserted back into the FIFO of available addresses only when its place in the ordered sequence is encountered. The Write address, which changes every 25 ns, is then Gray encoded in order to limit the system to single bit transitions except in the case where the ordered sequence of cells is interrupted by encountering cells which are reserved while awaiting digitization. The Read address, which changes only on a longer time scale, is transmitted bit serially and stored in a shift register on the SCA chip. This serves to reduce both the number of simultaneous bit transitions and the number of pins required on the SCA.

3.7 Clock fanout

The FEB receives a single 40 MHz clock from the TTC system. The Module 0 implementation of the LAr readout does not use the full TTC system, including TTCRx chips, which will be used in ATLAS. Therefore, no programmable delay of the 40 MHz is provided on the Module 0 FEB. Instead, the external Module 0 TTC system was designed to provide each FEB with an individually delayed 40 MHz CLK signal.

Details of the clock distribution can be found in the "Clock Fanout" schematic. A variety of clocks of different phases are required on the FEB. As shown, these are all derived from the single input clock using ECL logic.

The "Write" logic of the FEB operates at 40 MHz. The Xilinx SCA Controllers receive the 40 MHz clock, and use it to run their internal address bookkeeping logic. The "Write" clock for the SCA analog pipelines is clipped to a narrow width before being bused to the SCA chips. The SCA "Read" clock of 5 MHz is counted down from the 40 MHz clock. The SCA Write and Read clocks both have their phases adjusted for optimal noise performance by passing them through a series of gates.

The 5 MHz ADC clocks are counted down from the 40 MHz clock, and are phase-adjusted so that the digitization occurs at the appropriate time relative to the SCA Read operation (ie. once the SCA output data has settled). Similarly, the 5 MHz ALTERA clocks are phased to latch the ADC data at the appropriate time. The ALTERA chips also require 40 MHz clocks, in order to be able to synchronize and hand-shake with the Xilinx Controllers, and to be able to format and output the data at 40 MHz.

3.8 Communication and control

In addition to the 40 MHz CLK, there are two general types of control signals received by the FEB. Control data is sent via a "SPAC" serial control link, while time-critical signals, such as the Level 1 Accept, are transmitted from the TTC system. Both are described in more detail below.

3.8.1 Serial control

Each FEB is connected via a bi-directional SPAC serial control link [4] to a "SPAC Master" module which is located in an external VME crate. The serial links of the various FEB are bused within a front-end crate. Control data required to configure the FEB for data taking are transmitted to the FEB through this link. It is also possible to read back and verify these parameters using the same link.

Details of the implementation of the SPAC link on the Module 0 FEB can be found in the "SPAC Interface" schematic. An ALTERA FPGA, booted upon power-up from an EPROM, serves as the SPAC slave. It communicates with the SPAC link, and also with the different components on the FEB which need to be addressed. The local SPAC address of a particular FEB is set via a 7-bit switch mounted on the FEB.

The various types of data to be loaded to (and/or read back from) the FEBs, and the protocols used, are summarized in reference [5]. The operations which can be performed via the SPAC link on the FEB include:

- set the switches on the Shaper chips which enable/disable the contributions from the individual channels to the Level 1 analog sum,

- program the DACs used to set the offset voltage at the ADC inputs,
- download the program to be operated by the Xilinx SCA Controller FPGAs,
- download the parameters to configure the Xilinx SCA Controller FPGAs, such as the number of samples to digitize, the order of digitization, etc.
- download the program to be operated by the ALTERA gain selection FPGAs,
- download the parameters to configure the ALTERA gain selection FPGAs, such as the number of gains to digitize, the order of digitization, thresholds to be used in the gain selection, etc.
- read back the temperature from the two digital thermometers, one on each side of the FEB.

3.8.2 TTC control

In addition to these “slow” control signals sent via the SPAC serial link, there exist several “fast” signals for which the phase with respect to the 40 MHz machine clock is important. These are the clock itself (CLK), Level 1 trigger (L1), bunch-crossing counter reset (BCR), reset (RST), initialize (INIT), and test pulse (TP). The first three signals are responsible for the operation of the FEB and synchronization of the system with the Level 1 trigger. A RST would imply a complete board reset, including rebooting the SCA Controllers, while INIT would clear all buffers and align all pipelines on a well-defined cell (such as cell 0). A TP signal would cause the preamplifiers to be pulsed (assuming the pulser had been enabled via the SPAC link), one of the test features of the FEB.

These signals are generated by the TTC system. For Module 0, these signals are transmitted to each FEB differentially via point-to-point connections, though a bused solution for all signals except CLK is under investigation. The implementation of the TTC link on the Module 0 FEB was illustrated in the “Xilink & TTC” schematic. Since the TTC signal could be bused, while the CLK connections are point-to-point, it is necessary to ensure that one avoids the possibility of a metastable state occurring if edges overlap when the signals are latched by the SCA Controllers using the CLK signal. Therefore, all signals except CLK are sent through an ALTERA FPGA functioning as a programmable delay, before transmission to the Xilinx SCA Controllers. No delay is applied to the CLK, in order to avoid degrading the energy and particularly the timing resolution by increasing the CLK jitter.

3.9 Data transmission

The system is completely data-driven, with all necessary control information (such as event headers, bunch-crossing numbers, etc.) accompanying the data, having been inserted into the data stream by the ALTERA gain selection chips. Parity is also included in the data to allow the detection of transmission errors.

Data is synchronously output from the FEB in 32-bit words at 40 MHz, corresponding to 1.28 Gbit/s. The data is sent via differential PECL via two output connectors (one connector per set of 64 channels), along with a 40 MHz clock which can be used by the miniROD to strobe the data. The data format which has been implemented is described in reference [3]. Data from a given ADC is packed into 16-bit words by its ALTERA gain selection chip (12 bits of ADC data, 2 bits gain, 1 bit fixed to 0 to identify the word as an ADC data word instead of a control word, and the last bit a parity bit to ensure odd parity). To avoid a multiplexer and wide data bus at the output, each 32-bit wide data word contains 2 bits of data from each of the 16 ADCs. Thus, the ALTERA transmits two bits of a 16-bit word, every 25 ns for 8 CLK cycles. Since the ADCs are operated with a 200 ns clock (ie. 5 MHz), the time required to transmit one 16-bit word in this way exactly matches the time until the next word is produced. Therefore, an additional advantage of this method is that it removes the need for large digital buffers on the FEB.

To allow a later "upgrade" to an optical data link, the output connectors can include a 5 V regulated voltage (on some of the pins normally reserved for ground) in order to provide power to a plug-in module with the serializer and optical transmitter. This selection between +5 V or ground on these pins is enabled via jumpers on the FEB.

3.10 Level 1 trigger sums

The first level of Level 1 analog sums is performed by the shaper chip, which sums its four channels (assuming they have each been enabled by the shaper trigger switches). The sum outputs of the shaper chips are routed on an inner layer to two plug-in "Layer Sum Boards" which perform the next level of analog summing with a granularity which depends on which section of the calorimeter is being read out by the FEB. The Layer Sum Board outputs are routed to the central connector on the input signal side of the FEB, for transmission via the baseplane to the Trigger Tower Builder. Care was taken to keep well separated the trigger outputs and input signals, to avoid inducing oscillations.

3.11 Test functions

The most stringent test of the FEBs, and indeed of the entire read-out chain, is derived from the calibration system. However, given the limited access to the FEB crates, it is very important that the FEBs be fully tested before installation and connection to the calorimeter and calibration system. In addition, the size and density of the FEBs implies that re-working the boards will be a difficult task, and so it will be important to be able to not only discover a failure, but to identify as closely as possible the source of the failure. This ability will also allow remote "debugging" of faulty components during normal ATLAS running, with the possibility (at least for some possible failure modes) to reconfigure the read-out to minimize the number of bad channels. For these reasons, several different, and redundant, test features are incorporated into the FEB design itself, including:

- As mentioned previously, the warm preamplifiers can be pulsed via their -3 V power supply line. This feature allows a thorough test of the FEB electronics chain, including the Level 1 sums, independent of the calibration system. For noise reasons, the pulse must be heavily filtered and does not resemble the LAr signal pulses. However, the final pulse is sufficiently large that it is possible to check whether all channels, and all gain scales, are functional.
- The offset between SCA and ADC is set via a DAC which can be programmed via the SPAC link. Tests of the DC linearity and noise of the ADCs can be performed this way. For such tests, the SCA outputs can be held in a high impedance state such that the noise will be dominated by that of the ADC itself.

- The SCA Controller design contains sufficient flexibility to allow operation of the SCAs in different modes for testing purposes. For example, one can program the number of samples and the order in which the samples are digitized, one can switch on or off operation with simultaneous Read and Write operations, etc.
- While the gain selection logic would normally be configured to choose the gain for each channel, it is possible to reconfigure it to force selection of any particular gain for any channel, or to read out all three gains for all channels.
- All digital parameters which are down-loaded via the serial control network (such as the number of samples, etc.) can be read back through the same network.
- Via the serial network, it is possible to load test data into the ALTERA gain selection and data formatting FPGAs. Upon receipt of a trigger, they will then use the downloaded data in place of real ADC data, formatting the rest of the event with the appropriate header, control words, and parity bits so that the fake "event" can be unpacked by the miniROD. Reading the data through the standard data link and comparing with the down-loaded patterns allows identification of failures in the data transmission hardware, etc.

3.12 Power and grounding

Power is brought to the FEB on the 10-conductor power bus in the Front End Crate. Each voltage is locally regulated on the FEB. The voltages used, and the currents drawn for a single FEB, are summarized in table 1. The total power dissipation for a single FEB (with Cu readout) is approximately 85 W, or 0.66 W per channel. Of this, approximately 20% is dissipated in regulator voltage drops. However, the regulators are essential for a variety of reasons, including protection of the board against faulty power supply voltages, over-current protection, and noise immunity.

Input Voltage (V)	Current (A)	Power (W)
+6VD	4.15	24.9
+6VA	3.20	19.2
+4V	3.80	15.2
-4V	5.30	21.2
-6V	0.20	1.2
+11V	0.23	2.5
Total		84.2

Table 1: Power dissipation of the Module 0 FEB.

The distribution of regulators for the preamps and shapers, and for the SCAs and the digital part of the FEB, are shown in separate schematics. A total of 20 voltage regulators are required per FEB. Several of the voltages are split to two regulators, both to separate the power for the two sets of 64 channels, and to stay safely within the current ratings of the regulators (particularly for the negative regulators). The regulators are physically mounted toward the back of the FEB.

The grounds are split in several places on the FEB to minimize the noise couplings and ground currents. One ground split occurs between the shapers and SCAs, and another underneath the ADCs. All grounds are tied together at a single point on the FEB.

The FEB PCB is designed with a large number of additional holes for mounting the cooling plates. To remove the heat from the FEB, a water-cooled plate will be mounted to each side of each FEB (see the separate note on the Front End Crate for more details).

3.13 Module 0 FEB noise performance

Table 2 summarizes the noise measured on the Module 0 FEB. The noise of 6.6 counts $\approx$ 6.6 mV for the HI gain with preamp loads agrees well with the noise of 6.5 mV measured for the combination of preamp plus shaper measured on a separate test jig[6], demonstrating that the HI gain noise as measured on the FEB is, as required, dominated by the preamp noise. Measurements of an early FEB prototype, before the shapers were mounted, found a total noise of 0.5 ADC counts for the combination of SCA, op-amps and ADCs.

FEB Configuration	Noise (ADC Counts)		
	HI gain	MED gain	LO gain
No preamps	0.68	0.66	0.59
50 Ω preamps, no input loads	5.8	0.9	0.6
50 Ω preamps, 330 pF loads	6.6	1.0	0.6

Table 2: Noise per channel (in ADC counts) as measured on the Module 0 FEB. One ADC count corresponds to approximately 1 mV, referenced to the ADC input.

It was seen with unshielded input connectors that the coherent noise was unacceptably high, typically 10 - 20% of the total noise, whereas the specification of less than 3 MeV per channel is of order 5%. Tests with the new connector shields and grounds indicate that the 5% specification can be met. Additional improvement, down to the 2 - 3% level, is obtained once the FEB is optically decoupled. Figure 5 shows some typical coherent noise results, expressed as a percentage of the total noise per channel.

The dynamical performance of the Module 0 FEB, including pulse linearity, crosstalk, etc., also meets the specifications. These results are reported in a separate note.

4 Evolution toward the ATLAS FEB design

As mentioned previously, the Module 0 testbeam schedule did not allow sufficient time for the Module 0 FEB design to address all of the final ATLAS requirements. The status of some issues remaining to be resolved, and plans for resolving them, are discussed briefly below.

4.1 Radiation tolerance

Including safety factors, the final FEBs must tolerate, over 10 years of LHC operation, ionizing radiation of 100 kRad and neutron fluences of 5×10^{13} n/cm^2.

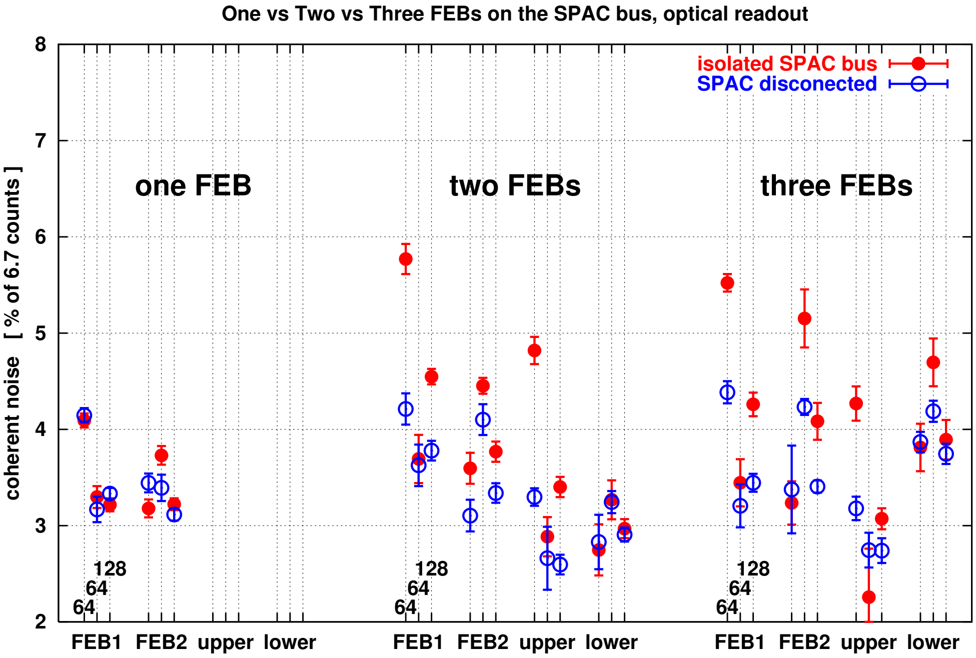

Figure 5: Coherent noise per channel, expressed as a percentage of the total noise per channel. The data show a variety of FEB configurations, including operation with a single FEB, and with 2 and 3 FEBs in the crate.

The analog signal chain involves custom preamplifiers, shapers and analog pipelines. The discrete preamplifier hybrids and custom ASIC shapers both utilize bipolar technologies and have been demonstrated through testing to be sufficiently radiation tolerant. The Module 0 SCA chips were produced using the Hewlett Packard (HP) 1.2 μm CMOS process. Before the Module 0 production, it was known that this process was being discontinued by HP in favor of smaller feature size processes, and the design would have to be migrated to a different process. The design has since been migrated to the DMILL process; first DMILL prototypes are being tested and show excellent results (see the separate note on the DMILL SCA). It is assumed that the final SCA chips will be produced with DMILL, and will resolve the radiation tolerance issue for the SCA.

The Module 0 FEB uses a commercial 12-bit 10 MHz CMOS ADC (the AD9220 from Analog Devices). Radiation tests of this device (a note is in preparation) showed that, at total doses of less than 10 kRad, the analog current started to rise. Therefore, this device is not suitable for ATLAS. A possible replacement is the Analog Devices AD9042, a bipolar 40 MHz 12-bit ADC. This device has been extensively radiation-tested by CMS, and withstands up to several MRad and several $\times 10^{13}$ n/cm^2 without degradation[7]. We have tested several samples, before irradiation, and verified that the devices perform well at 5 MHz on a test board designed to mimic the setup we would use on the ATLAS FEB. We have acquired several irradiated parts from CMS in order to repeat these measurements after irradiation; these tests will soon begin.

Concerning the digital logic, the current Xilinx FPGA's (which use a 0.35 μm process) were irradiated, and showed no damage until about 40 kRad. Recent results of a newer version of the chip, fabricated in 0.25 μ CMOS, however, showed damage below 10 kRad.

Additional tests of ALTERA FPGA chips are planned. However, even assuming an FPGA which survived the total dose could be found, a worry remains about the possibility that the FPGA configuration is lost by a neutron or charged particle induced single event upset, requiring that the program be reloaded. For these reasons, the working hypothesis is that the FPGA's used on the Module 0 FEB will have to be migrated to Gate Arrays using DMILL or some other radiation tolerant process. As a learning exercise, we have started the process of migrating the current Xilinx SCA Controller to DMILL, in consultation with the service offered by CEA for such conversions.

The final ATLAS FEB will require many voltage regulators. We plan to use the positive voltage regulators being developed at CERN, and have specified that we will also need negative voltage regulators. The discussions concerning development of negative regulators continue, and this is a critical issue for development of the final FEB.

The tantalum capacitors used on the Module 0 FEB will be replaced with ceramic capacitors. If radiation-tolerant DACs are not available, the offset to the ADC could be set with passive components, though this would remove the (non-critical) possibility to separately test the ADCs in situ.

4.2 Optical coupling

The final configuration of the front end crate should rely on optical coupling to the outside world, apart from power connections and the cables transmitting the Level 1 analog sums. The Module 0 FEB was designed to receive its control signals on copper cables, and to transmit the output data with differential PECL lines over copper. However, it was foreseen to "upgrade" the data readout to optics once optical links were more fully developed. Prototype G-Link optical FEB-ROD links have been developed and successfully tested. Incorporation of the links into the FEB design awaits finalization of the optical link architecture.

Simple optical decouplers for the TTC and CLK connections have also been developed and successfully tested. Development of an optically decoupled SPAC connection is in progress.

4.3 Control architecture

Some development is required of the final control architecture. The baseline calls for a Controller board installed in the front end crate. The Controller would be optically coupled to the SPAC Master, located in the associated ROD crate outside the detector, and to the TTC system, and would fanout the serial and fast control information to the boards in the front end crate. A prototype Controller board is currently under development, as is the implementation of the control fanout using buses for the SPAC and TTC information.

The final FEB design will incorporate a TTCRx chip for receiving the CLK and TTC information. We have acquired the existing TTCRx test board, and associated TTCVi module, to begin the process of implementation of the TTCRx in the FEB design. Having a TTCRx chip on each FEB also gives rise to the possibility to use the TTC "Channel B" feature as a redundant path for sending the control data required to configure the FEB.

The final choices await demonstration of the Controller prototype, and further study of the bus and other possible architectures, including issues of reliability and fault tolerance. Investigations are also being made of the noise implications of signal buses in the crate. For example, in figure 5, the coherent noise per channel was plotted for 1, 2 and 3 FEBs in the crate. These measurements need to be extended to more boards in order to fully evaluate any possible degradation introduced by signal buses interconnecting the boards.

5 Summary and conclusions

The Module 0 FEB has been successfully designed with the final ATLAS channel density. Lab tests and initial testbeam measurements with a few FEBs (described in a separate note) indicate that they satisfy the ATLAS performance specifications, though careful attention must be paid to the quality of the ground connection and shielding of the input connectors. A total of 50 FEBs have been produced and will soon be available at CERN for the 1999 testbeam runs, completing a major milestone in the FEB development.

Efforts are already underway to migrate from the Module 0 FEB to the final ATLAS FEB design. The schedule calls for production of a full crate of final ATLAS FEB prototypes in 2001 in order to fully assess their performance in the testbeam before proceeding to production.

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