ATLAS Liquid Argon Calorimeter Front End Electronics

Names and institutions

ABSTRACT: The ATLAS detector has been designed for operation at CERN's Large Hadron Collider. ATLAS includes a complex system of liquid argon calorimeters. This paper describes the architecture and implementation of the system of front end electronics developed for readout of the ATLAS liquid argon calorimeters.

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Version history

- - Dec. 18/2007 - JP - another major pass at editing, reorganizing
- - Dec. 12/2007 - JP - more work; shifting SPAC and other things around
- - Dec. 8/2007 - JP - lots of writing/editing
- - Dec. 1/2007 - JP - lots of writing/editing, insert HV+280V, CMB
- - Nov. 11/2007 - JP - lots of writing/editing, insert HEC LV
- - Nov. 4/2007 - JP - integrate Receiver, Baseplane sections
- - Oct. 10-19/2007 - JP - pick up again, integrate TBB figures, start writing/editing process again, add in HV section title, start to fill in figs and info on TDB
- - Mar. 24/2007 - JP - start to integrate part on TBB from Xavier
- - Mar. 8/2007 - JP - split off perf part to separate note. start putting in info from Helio's old crate note, move to JINST .tex template
- - Feb. /2007 - JP - put contributions from Luis, Bertrand
- - Jan. 10/2007 - JP - template created

1. Introduction

ATLAS [1] is a large general-purpose detector designed for operation at the Large Hadron Collider (LHC) at CERN. The LHC is a proton-proton collider which will operate with a center-of-mass energy of 14 TeV. A system of liquid argon (LAr) calorimeters forms one of the major ATLAS detector systems. The LAr calorimeters include the electromagnetic barrel (EMB) calorimeter, which is housed in the central cryostat and provides coverage for pseudorapidities $|\eta| < 1.5$. The ranges of larger pseudorapidity are covered by endcap calorimeter (EC) systems, housed in separate endcap cryostats. Each EC cryostat includes an electromagnetic endcap (EMEC) calorimeter, a hadronic endcap (HEC) calorimeter, and a forward calorimeter (FCAL) providing coverage up to $|\eta| = 4.9$. More details about the design, construction, and performance of the calorimeters themselves can be found in Reference [2].

As depicted schematically in Figure 1, the electronic readout of the ATLAS LAr calorimeters is divided into a Front End (FE) system of boards mounted in custom crates directly on the cryostat feedthroughs, and a Back End (BE) system of VME-based boards located in an off-detector underground counting house (dubbed USA15) where there is no radiation. The design and implementation of the BE system, which includes DSP-based electronics for digital filtering of the readout signals in order to reconstruct the deposited energy and other quantities, is described in Reference [3]. The purpose of this note is to describe the overall architecture and implementation of the ATLAS LAr FE system. A subsequent publication will describe the measured system performance of the overall ATLAS LAr readout.

2. Overview of ATLAS LAr Front End Electronics

Given the fine segmentation of the ATLAS LAr calorimeters, a total of 182468 active channels must be read out. The FE electronics faces demanding requirements, which include the following:

- the calorimeter signals must be sampled at the LHC bunch crossing frequency of 40 MHz. The signals must be stored during the latency of the Level 1 (L1) trigger of up to 2.5 μs (100 bunch crossing). For triggered events, the readout must be accomplished without significant deadtime for a maximum mean L1 trigger rate of 75 kHz.

- the energy deposit in each calorimeter cell must be measured with a precision of better than 0.25% at high energy. A dynamic range of ≈ 17 bits is needed to cover the energy range of interest, from a lower limit of ≈ 10 MeV set by the noise levels up to a maximum of 3 TeV. The coherent noise over many cells must be maintained below 5% of the total noise per channel.

- the time of the energy deposition in each calorimeter cell must be measured with a precision of ≈ 100 ps for high energy pulses.

- analog sums corresponding to L1 trigger towers of size $\Delta\eta \times \Delta\phi = 0.1 \times 0.1$ must be delivered for use by the L1 trigger system.

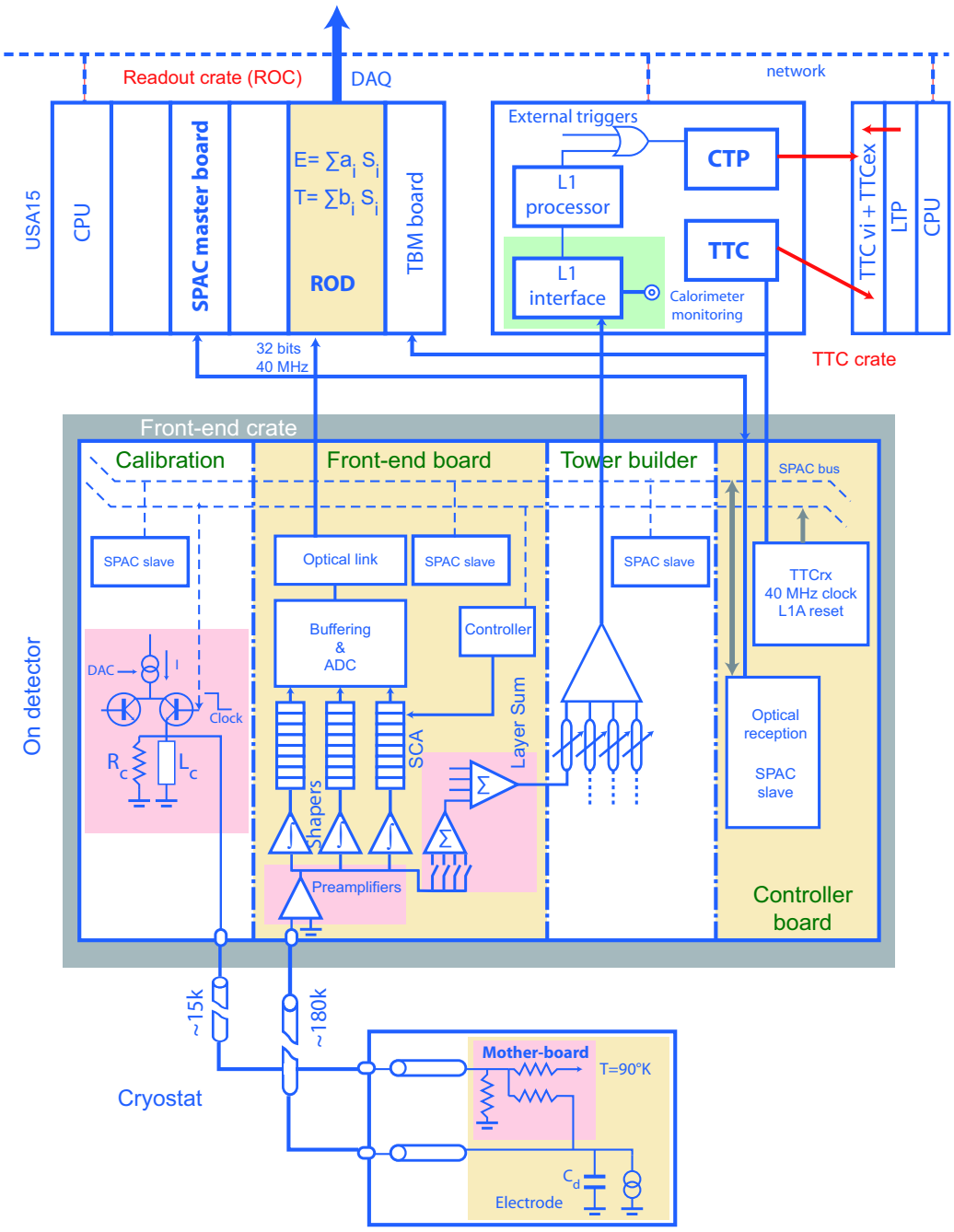

Figure 1. Block diagram depicting the architecture of the overall ATLAS LAr readout electronics. The lower box depicts the calorimeters installed in their respective cryostat. The central box illustrates the functionality of the FE boards located in FE crates mounted on the cryostat feedthroughs. The upper layer shows the off-detector BE electronics mounted in Readout Crates, as well as trigger and TTC (control) crates.

Given the stringent noise requirements, the LAr FE electronics boards are placed in crates mounted directly on the calorimeter cryostat feedthroughs. This on-detector location provides many additional requirements, including tolerance of significant levels of radiation. Achieving a high channel density and low power is important. The FE boards must be water-cooled to remove

any heat dissipated. Access is very limited, so reliability is a key concern.

2.1 FE System Architecture

As was shown in Figure 1, the FE system includes Front End Boards (FEB), which perform the readout and digitization of the calorimeter signals, Calibration (CALIB) boards which inject precision calibration signals, Tower Builder Boards (TBB) and Tower Driver Boards (TDB) for producing analog sums for the L1 trigger, and Controller (CONT) boards for distributing clocks and other control information. **expand this para a bit?

The conceptual design of the FE crate (FEC) is shown in Figure 2. Crates are mounted on top of mechanical structures called pedestals, which serve as transition pieces between the cylindrical walls of the cryostats and the flat crate bottom. Inside the pedestal, the calorimeter signals are routed from the feedthrough to the baseplane of the crate via stripline cables. The FEC baseplane plays the role of a traditional backplane, except in this application only analog signals are routed on the lines. Power distribution within the FEC is done along one side of the FEC via a dedicated power bus. Another bus mounted on the same side of the FEC is used to distribute the "SPAC" serial control signals to the various boards in the crate.

Each FEC is divided mechanically into two halves. The bus distributing power to the boards traverses the entire crate, but for most other purposes the basic element of the FE electronics is one Half FEC (HFEC). The configuration of each HFEC depends on the calorimeter to which it is connected. The EMB is equipped with 32 FE crates, configured as 64 identical EMB HFECs. The readout of the EMEC includes 16 dedicated EMEC crates, configured to provide 32 "EMEC Standard" HFECs. In addition, a set of eight crates are shared between the EMEC and the HEC, providing eight "EMEC Special" HFECs and eight HEC HFECs. The FCAL has two dedicated crates, which are only half-equipped in order to provide the necesary two FCAL HFECs. Table 1 summarizes the number of the various types of FE boards in each type of HFEC. Note that a total of 1524 FEBs is required to read out the entire calorimeter system.

HFEC Type	HFEC	FEB	CALIB	CONT	TBB	TDB
EMB	64	896	64	64	64	-
EMEC Std	32	416	32	32	32	-
EMEC Special	8	136	16	16	24	-
HEC	8	48	8	8	-	16
FCAL	2	28	2	2	-	4
Total	114	1524	122	122	120	20

Table 1. Summary of the numbers of the various main FE boards per HFEC type for the different calorimeters.

Electronics boards are inserted into the FEC from the top (as seen in Figure 2). Active boards are equipped with two cooling plates, which serve as heat exchangers so that the chilled water circulating within them removes the heat from the electronic components. To prevent leaks, the water is circulated below atmospheric pressure.

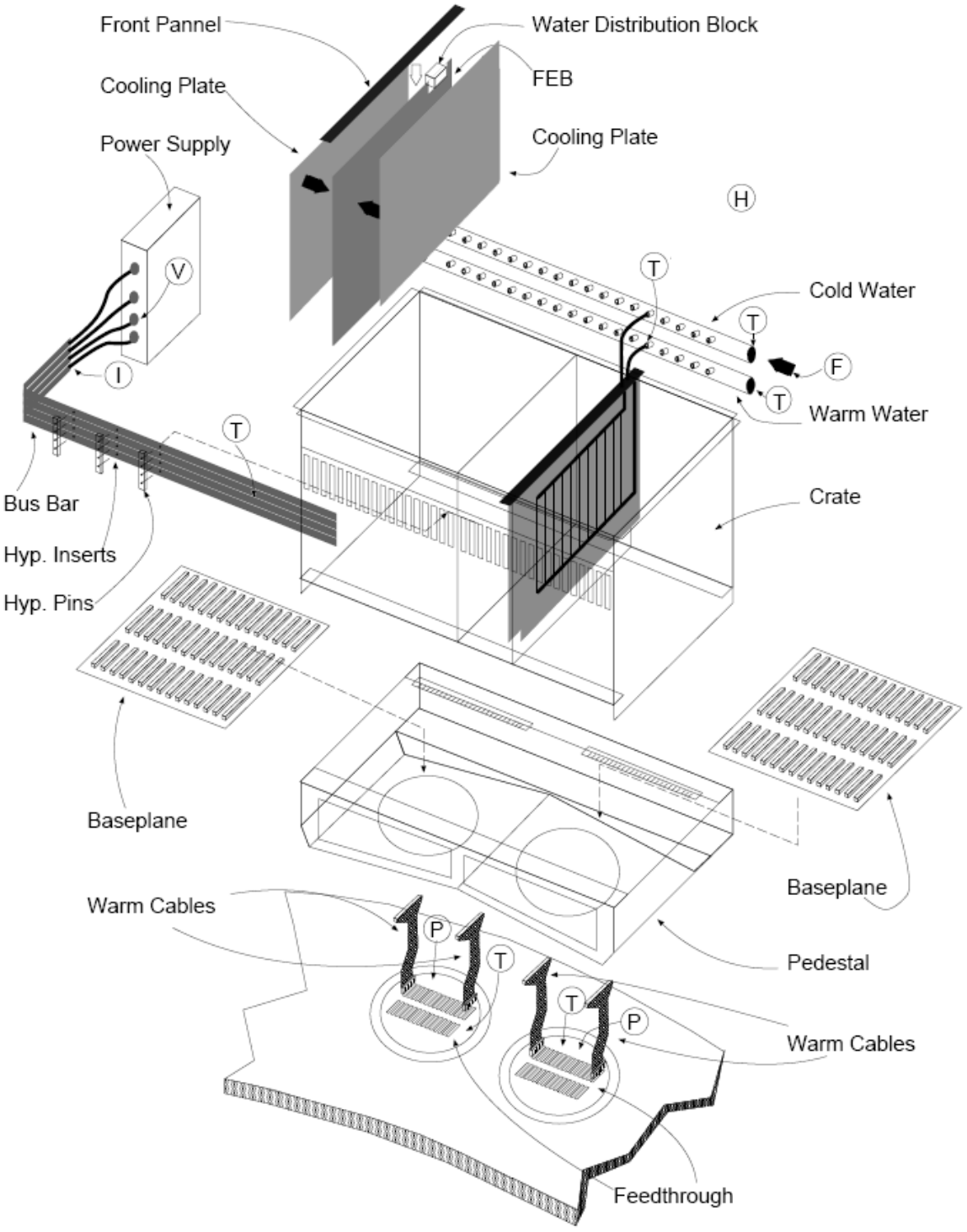

Figure 2. Conceptual drawing showing the various components of the FEC system.

Crates are mounted around the circumference as the calorimeter. Figure 3 shows the arrangement of major components on the system in the vicinity of one FEC. Figure 4 shows a photograph of one end of the EMB cryostat, in which a number of the FECs are visible. The mechanical in-

tegrity of the FEC and pedestal structure need to be properly dimensioned to hold the electronics weight at different angles. The spaces between FECs are heavily used for the routing of cables and other services to the ATLAS inner tracking detectors, so strict attention must be paid to staying with the envelope of space assigned for the LAr electronics.

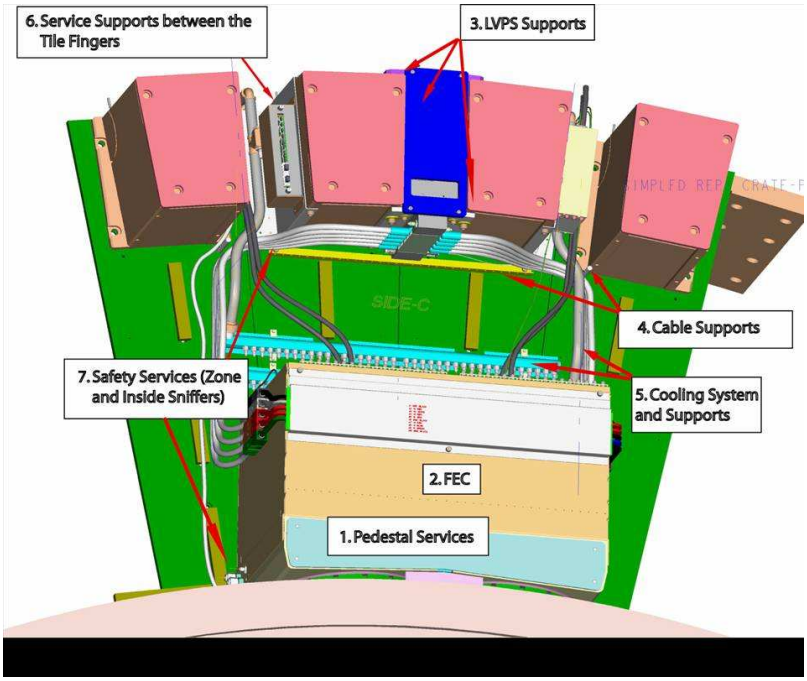

Figure 3. Diagram depicting the arrangement of LAr frontend electronics components in the vicinity of one Front End Crate. ***photo better?

The various boards in the FECs require control signals for proper operation. These signals include the 40 MHz LHC clock, the L1 Accept signal, and other fast synchronous signals provided as part of the ATLAS Trigger, Timing and Control (TTC) system [9]. In addition, most of the boards need to be configured and monitored by writing or reading back the values of various on-board registers and other resources. A custom serial link known as SPAC (Serial Protocol for the ATLAS Calorimeters) [10] is used for this purpose. These control architectures are described in more detail below.

The FE readout is implemented via custom electronics boards housed in the FECs. The external dimensions of the boards must be 490 mm $\times$ 409.5 mm, and the board thickness is limited to a maximum value of 2.54 mm. Figure 5 illustrates the required board dimensions, and all the connectors and their locations. Connectors are mounted along three edges of the boards. Connectors along the front panel side bring in the TTC control signal and provide outputs to the BE electronics. On the opposite edge, connections to the FEC baseplane are made. Finally, the power and SPAC serial control connections are made along one side edge of the boards. Boards are located in the FEC with a pitch of 800 mils (20.3 mm). However, unlike the case for VME-style boards, the boards are mounted on the center relative to their front panel (see the side view on the right of Figure 5).

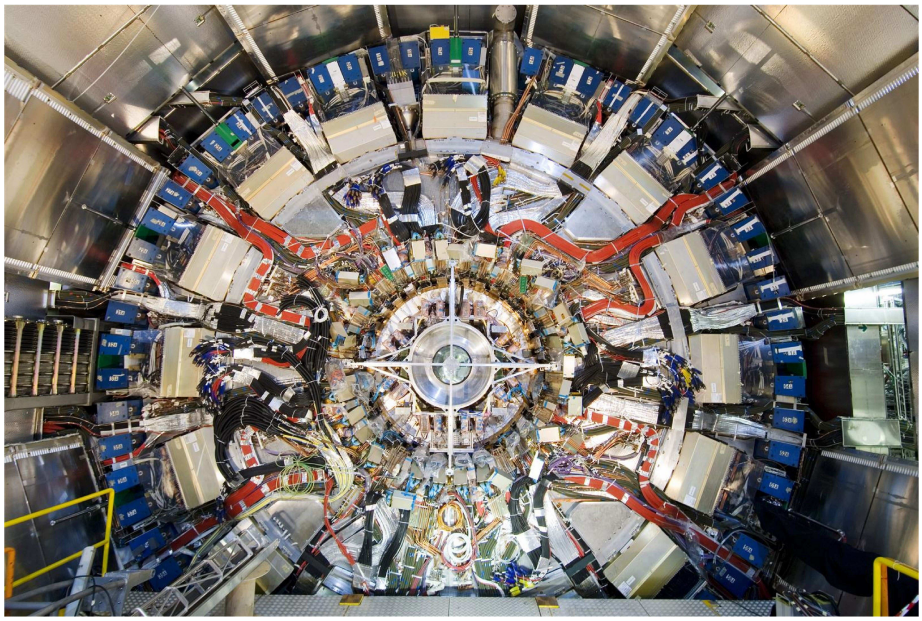

Figure 4. Photograph of one end of the EMB cryostat, taken during June 2007 during installation and integration of the inner tracker endcap. The LAr FECs are visible around the circumference of the cryostat.

Figure 5. Drawings showing the mechanical dimensions of electronic boards to be inserted into the FEC, along with the locations of the various connectors. ***need new fig 4 from Helio's note; current .eps crashes file and can't be used; perhaps don't need??

2.2 Trigger, Timing and Control

The ATLAS TTC system [9] distributes the 40 MHz LHC clock, the L1 Accept signal, and other signals (such as Resets) which are necessary to properly synchronize the various parts of the ATLAS detector. These signals are driven optically from the TTC crate located in USA15 to each Controller through individual optical fibers. The signals are then electrically distributed to each FE board through point-to-point connections.

***doubling for reliability

2.3 SPAC Serial Control

The general layout of the SPAC serial communication system is shown in Figure 6. This link is used to load, to update, or to read back the various registers and memories of the FE boards through VME commands sent to the SPAC Master boards [12], located in the ROD crates in USA15. Each serial network consists of one master and multiple slaves. Connections betwen SPAC Masters in USA15 and Controllers in FECs on the detector are made via unidirectional optical links. Separate fibres are required for Master-to-Slave (MS) and Slave-to-Master (SM) communications.

The protocol requires, at least, two unidirectional lines: one Master to Slaves line (MS), and one Slaves to Master line (SM). For each direction, both data and clock are combined to form a single signal in the same way as in the Manchester coding system: a logical one (respectively zero) is coded by a low to high (respectively high to low) transition. For reliability purposes, the down-

stream and upstream serial lines MS are duplicated (upstream lines : SM1, SM2 ; downstream lines : MS1, MS2). At any time, only one of the two downstream lines carries the useful information, the other line remaining idle (the decision is done at the SPAC master level). Each serial slave receives both lines and automatically detect which one is idle and which one is active. On the opposite, the upstream serial lines SM1 and SM2 carry both the same information at the same time. This scheme limits the decision logic on the remote slave side and therefore improves the reliability of the system.

The optical signals are converted into electrical differential signals on the Controller and transferred on a copper bus to the various FE electronics boards, housing the serial slaves. To improve the reliability and the noise immunity of the system, the serial bus is implemented in a differential technology.While the master boards, sitting in a radiation-free environment, consist of programmable logical devices housed on VME boards, the serial slaves, located in the FE crates, have to be radhard ASICs.

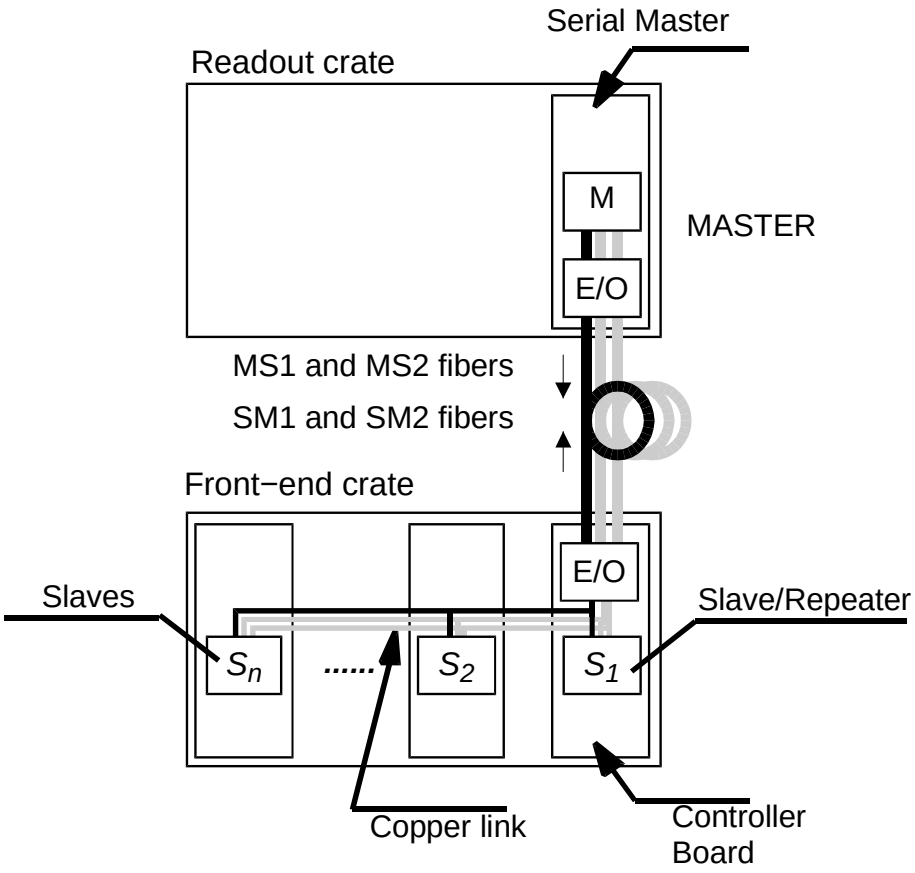

Figure 6. Architecture of the SPAC serial control system.

The protocol enables point-to-point read or write data accesses or broadcast write data accesses to all or a part of the slaves of a network, at a raw data bit rate of 10 Megabits per second. Each serial slave in the network is identified by a unique 7-bit address. One of these addresses is reserved for *global broadcast* accesses, and 15 others are reserved for *local broadcast* accesses. Each

serial slave is also assigned a 4-bit local broadcast address that determines which local broadcast command it should consider.

SPAC Frame definition

Any SPAC frame (figure 7) circulating on the network is a sequence made of 9-bits data words, as sketched in figure 7. At a rate of 10 Mbits/s, one word is 900 ns long.

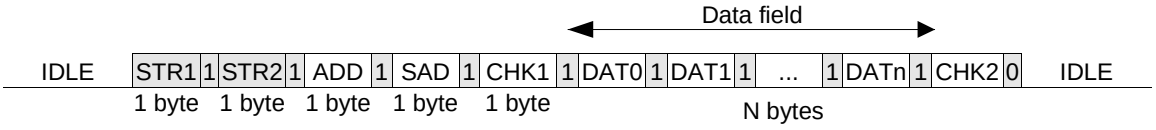

Figure 7. Sketch of a typical SPAC3 frame, made of 9-bits data words.

- All data bits are Manchester-encoded, such that a logical one is coded by a low-to-high transition (i.e. 50 ns low, 50 ns high at 10 Mbits/s) while a logical zero is coded by a high-to-low transition.
- The 9-bit data word consists of a byte of useful data, sent in *big endian* order (least significant bit first), and a Continue/Last bit (logical zero for the last word).
- The *idle state* of the serial lines is indicated either by a static low level or a sequence of indefinite length of logical `{0,1}` doublets that form a *carrier*.
- The start (STR) of a frame is indicated by a *preamble*, made of a 2 bytes pre-defined sequence of logical zeros and ones (`$55`, a continue bit, `$3A` and a continue bit, forming the pattern shown in figure 8).
- The fifth word is a *"partial" checksum* (CHK1), calculated on the slave address and the sub-address fields of the frame. If a slave detects a checksum error at this level, it ignores the subsequent data bytes of the frame. ***explain why
- The last word is the *data checksum* (CHK2), calculated only on the data field if it exists (bytes after the partial checksum).
- At the end of the frame transmission, the lines goes back to its idle state (static low or carrier).
- Particular case: when a slave detects an error in an incoming frame, it can generate an *interrupt frame*, under the form of a static high level during approximately one microsecond.

The frames produced by the master (resp. a slave) are such that the direction bit of their second word is 1 (resp. 0). The words between the fifth (partial checksum word) and the last one (data checksum word) are the data field. Its function varies according to the context:

- In a write frame produced by a master, it contains the data bytes to write into the slave boards.

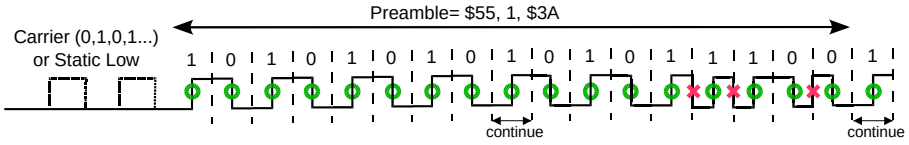

Figure 8. Predefined preamble indicating the start of a frame (denoted STR in the other figures). ***combine with previous fig using (a),(b)

- In a read request frame produced by the master, it indicates the number of data bytes to read from the target slave board (or *byte count*). In this configuration, the data field cannot contain more than two bytes, and if it is empty, the byte count is assumed to be 1.
- In an answer frame produced by a slave, in consequence of a read request produced by the master, the data field contains the data read from the board.

SPAC Slave ASIC

Each FE electronics board house a SPAC slave ASIC to communicate with the SPAC master through the serial network. A functional diagram of the ASIC is shown in figure 9 and a detailed description of the chip is given in Reference [10]. The slave receives the incoming frames from the serial master on the MS serial inputs, decodes the different fields of the frames and, if required, communicates with the host board either by its parallel interface module or by its I^2C master interface. Finally, it encodes its reply frame and sends it to the master via the SM serial outputs.

The SPAC slave provides to the board it is mounted on a parallel interface to read and write, under request of the serial master, the on-board resources. These resources can be 8-, 16- or 32-bit registers, or a block of memory bytes of arbitrary length, and are identified with a 7-bit *subaddress*. Several subaddresses are reserved to access some internal resources of the SPAC slave. The SPAC slave also provides to the board a I^2C [**?**] master interface. I^2C interfaced components on the board can therefore be controlled through read or write accesses to some dedicated internal registers of the SPAC slave.

Typically, the SPAC slave ASIC communicate through I^2C interface with the calibration logic chip on the CALIB, through the parallel interface with the Configuration Controller on the FEB, and with the Bimux chips on the TBB. On each board, the slave ASIC receives its clock from its on-board TTCrx chip.

3. Front End Board

The frontend readout of the LAr calorimeters is implemented on the 128-channel Frontend Board (FEB). A detailed description of the design and implementation of the FEB can be found in Reference [4]. Here we describe only a few of the most salient details.

A block diagram indicating the main features of one four-channel element of the FEB architecture is shown in Figure 10. The raw signals from the calorimeter are mapped onto the FEB inputs as they emerge from the cryostat feedthroughs. On the FEB, the signals are first subject to

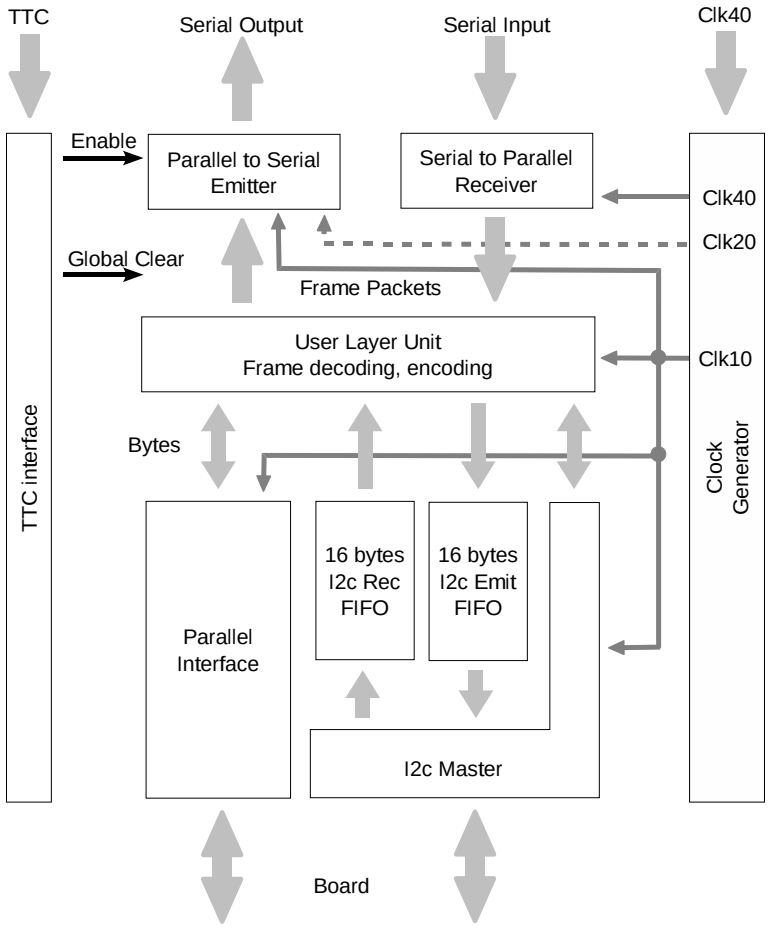

Figure 9. Functional diagram of the SPAC slave ASIC.

several stages of analog processing. Preamplifier hybrids amplify the raw signals, which are then split and further amplified by shaper chips to produce three overlapping linear gain scales which are each subject to fast analog shaping. The shaped signals are then sampled at the LHC bunch crossing frequency of 40 MHz by switched-capacitor array (SCA) analog pipeline chips, which store the signals in analog form during the L1 trigger latency. ***expand a bit (shaping fcn, gain ratios, ncells in SCA for derandomizing buffer plus deadtime, up to 32 samples, ...)

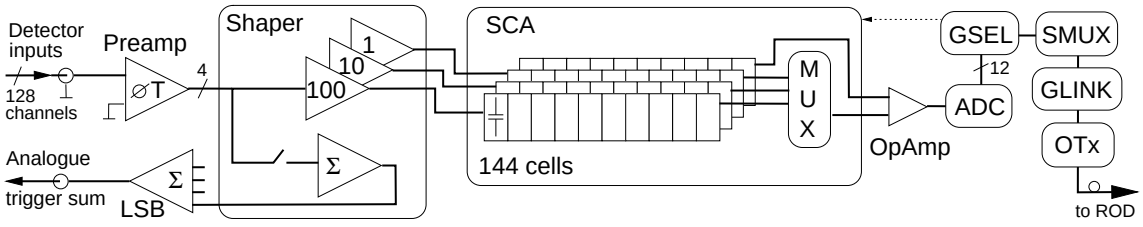

Figure 10. Block diagram of the FEB architecture, depicting the data flow for four of the 128 channels.

For events accepted by the L1 trigger, typically five samples per channel are read out from the SCA using the optimal gain scale, and digitized using a 12-bit ADC. The digitized data are formatted, multiplexed, serialized, and then transmitted optically out of the detector to the ROD via a single 1.6 Gbps optical output link per FEB.

In addition to reading out the individual calorimeter channels, the FEB performs the first two stages of summing in preparation of analog sums used by the L1 trigger system. Each shaper chip outputs a sum of its four input channels. These partial sums are routed to two Layer Sum Boards (LSBs) on each FEB that perform further summing, depending on the region of the calorimeter to which the board is connected, and then drive the sums through the FEC baseplane to the correspoding TBB or TDB in that HFEC.

***enough about FEB , or need a bit more?? perhaps some perf. numbers. (17 bits, coh noise < 3%, sigmaE < 0.1%, sigmat < 20 ps, power, ...)

4. Calibration Board

***one intro sentence

A detailed description of the design and implementation of the CALIB can be found in Reference [5]. Here we briefly describe only a few of the main features.

***few paras about CALIB functionality; Figure 11

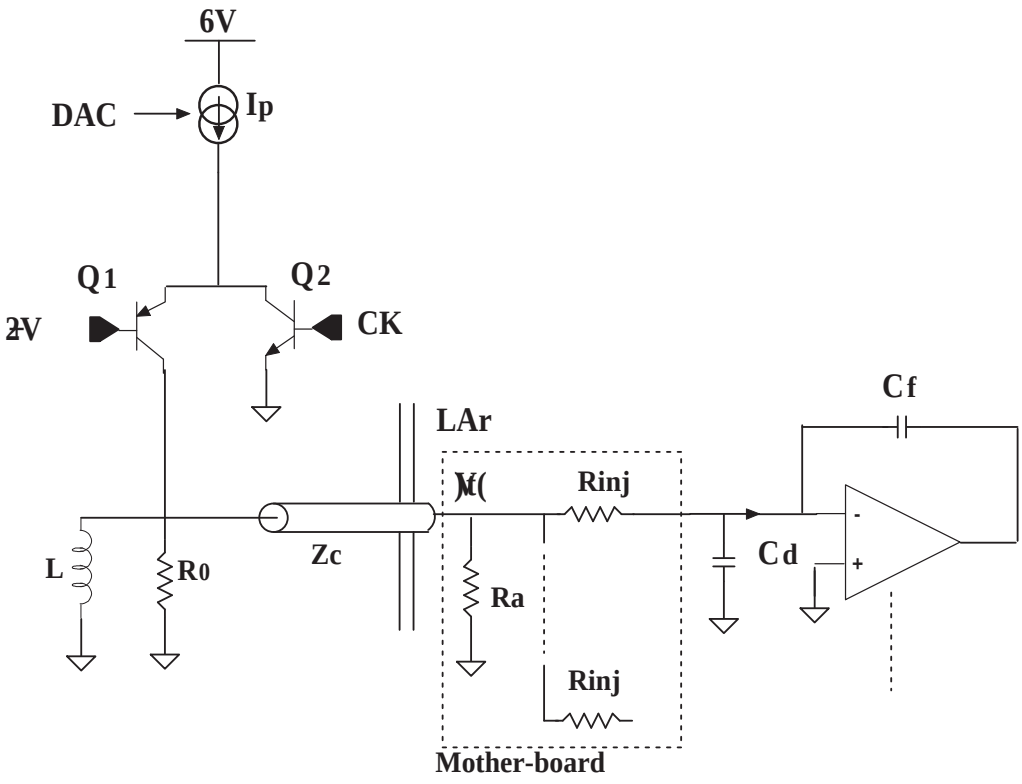

Figure 11. Schematic diagram of the calibration scheme for the LAr EM calorimeters. For more details, see the text.

5. Controller Board

The function of the Controller board is to receive the TTC and SPAC control signals and to fan them out and deliver them to the various FE boards in the same HFEC. Providing a local fanout in the FEC greatly reduces the number of TTC and SPAC links that must be provided from USA15 to the detector. As was shown in Table 1, each EMEC Special HFEC holds two Controllers, while all other HFECs hold one. A total of 122 Controllers are needed for the entire LAr system.

A functional diagram of the Controller is shown in Figure 12. The Controller receives optically from USA15 the TTC and SPAC signals, and converts them to electrical signals. The timing-sensitive TTC signals are distributed to each FE board using point-to-point connections, while the slower SPAC signals are fanned out via a dedicated SPAC bus mounted along the side of the crate. Figure 13 shows a photograph of a Controller.

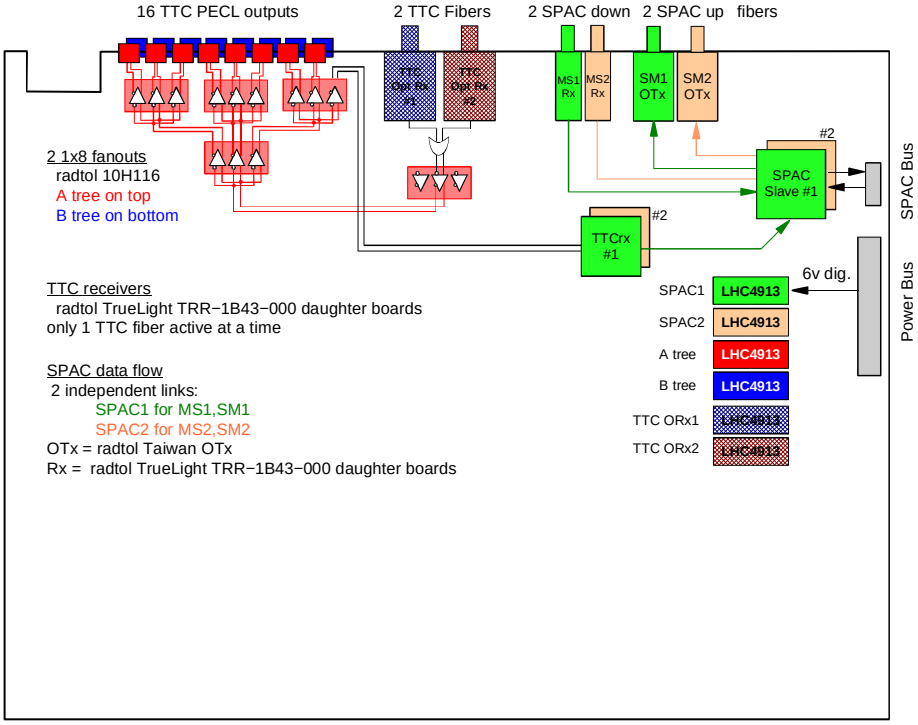

Figure 12. Functional diagram of the Controller board.

Table 2 provides the specifications of the different TTC signals and the SPAC bus to be implemented in each FEC type. Dmax is the maximum distance in slot units between the Controller and any of the boards to which it has to provide the TTC signal.

Trigger, Timing and Control Distribution

The Controller receives the TTC signal from USA15 optically on its front panel. For reliability purpose, it is equipped with two TTC optical receivers, each connected via an optical fiber. To enhance the reliability by reducing the logic on the Controller, no specific choice is made on the Controller to decide which of the two incoming TTC signals to use. This choice is made in USA15,

Figure 13. Photography of a Controller board from the production lot.***strange cropping, plus no panel. can get orientation as for schematic??

	Fanout	SPAC Bus Length	Dmax (slots)	Dmax (mm)
Barrel	16	19	9	183
Std EMEC	15	19	9	183
Spec EMEC1	11	12	9	183
Spec EMEC2	11	12	11	223
Spec HEC	7	12	9	183
FCAL	15	19	11	223

Table 2. Summary of the TTC links and SPAC bus configurations in the various FE crates. ***JP: units are confusing

an accessible area of the ATLAS pit, by connecting the desired optical fiber to the TTC optical output. ***repeated from earlier; consolidate

The Truelight TRR-1B43-0000 1300nm optical receiver is used to receive the TTC signal on the Controller. This component is too high to be mounted directly on the Controller PCB. A tailored implementation using daughter boards has been adopted, enabling the receiver to fit within the two cooling plates enclosing the Controller PCB.

The TTC signal is distributed through a tree of commercial MC10H116D ECL chips, configured in PECL format, with 18 terminations (two of them are used on the board by the two TTCRx used to handle independently the two SPAC slaves of the Controller itself). For reliability purpose, this distribution tree is organised as two independent branches. In case of problems with one of the branches, at most half of the TTC signals are lost.

The PECL TTC signals are output through 16 USB mini-B SMC connectors mounted on the Controller front panel. Custom one-meter halogen-free mini-B/mini-B cables deliver the TTC signal from the Controller to the other boards of the FEC. The differential impedance of the cable was measured to be $\approx 90\Omega$. The corresponding TTC signals assignment is given in Table 4. Due to the tight space requirement, the 16 mini-B connectors are placed on both sides of the Controller

PCB, eight on the top and eight on the bottom. To ease plugging in the cables, the connectors are mounted on SMC-like custom daughterboards.

Pin Number	TTC Pinout	(USB Pinout)
1	GND	(VBUS)
2	TTC-	(D-)
3	TTC+	(D+)
4	Not Connected	(ID)
5	GND	(GND)
Shield	GND	(GND)

Table 3. Cabling of the TTC USB mini-B cables.

SPAC Serial Control System and Distribution

In order to enhance the redundancy of the Controller, two independent links are implemented. Consequently, there are two SPAC slaves per board. Each of them drives one SPAC link : the SPAC #1 (resp. #2), on the top (resp. bottom) side, handles the serial lines MS1 and SM1 (resp. MS2 and SM2). It has its own radhard regulator and its own TTCrx providing the local clock.

The SPAC slaves on the Controller are set in a repeater mode [10], which is a different configuration than the SPAC slaves of the other FE boards. On one way, they are repeating the Master to Slave signal that is optically received by the Controller to one of the two Master to Slave lines of the SPAC bus. On the other way, they are transmitting the Slave to Master signal from the SPAC bus line to the optical tranceivers that send this signal to the SPAC master board.

Moreover, both SPAC slaves receive MS1 and MS2 signals, but drive only one MS signal each on the SPAC bus and return only one SM line back to the master.

The Controller receives optically two download fibers from the readout crate and transmits optically two read-back data links to it. To reduce the amount of optical components to radiation qualified, it was decided to use optical components also radiation qualified for another application, after having validated that the components were adapted to the optical transmission of SPAC signals. The Taiwan OTx components, to be used in the FEB to ROD link are thus used as optical transmitters. On the other hand, the Truelight TRR-1B43-000 optical receivers, already used for the TTC signals reception are used as SPAC optical receivers (mounted on daughter boards as explained before in the TTC reception section). The configuration of the optical components is then the following:

- SPAC Master to Controller : Truelight TRR-1B43-000 (1300 nm PIN receiver)
- Controller to SPAC Master : Taiwan FEB-ROD OTx (850 nm VCSEL based optical transmitter)

Thus, there are 2 Truelight receivers and 2 Taiwan transmitters implemented on each Controller. Let us notice that the optical wavelength of the incoming and outcoming signals are different. The optical transmitters and receivers on the SPAC Master side are of course adapted.

Production and Testing of the Controller

The Controllers are integrated into the LAr FE crates and must, therefore, respect the dimension constraints of the environment [**?**]. Two major constraints are the presence of cooling plates on each side of the board, limiting the thickness of the components to about 5.5mm, and the presence of matter partially covering the top of the FEC, limiting the available space on the front panel.

Including an allowance of 10% for spares, 135 Controllers have been built. ***move later

The Controller PCB is made of eight layers. The most critical lines are routed on impedance-controlled striplines in inner layers between two ground or power planes. For reliability purposes, the different functions of the board are partitioned such that six different power levels are used, routed on two power planes. The consumption of the board was measured as 1.5 Amperes on the digital 6 Volts power supply.

All the active components of the FECont have been radhard qualified. Some custom made components had to be produced on purpose for the LArg calorimeter Electronics in either DMILL or IBM 0.25 μm to implement dedicated functions and to cope with the radiation hardness expected by the experiment. The various active components of the Controller are:

Component	Part Number	#/Board	Manufacturer
SPAC Slave	SPAC 3	2	ATMEL
ECL Line Receiver	MC10H116-D	14	ON Semiconductor
TTCRx	TTCRx 3.2	2	ATMEL
Voltage Regulators	L4913	6	ST Micro
Optical Receiver	TRR-1B43-000	4	TrueLight
Optical Transmitter	OTx	2	Acad. Sinica, Taiwan
Power Connector	KS10-0002	1	Hypertronics
SPAC Connector	SSW-107-02-G-D-RA	1	Samtec
Baseplane Connector	91877-002	1	FCI Electronics
USB mini-B Connector	54819b	16	Molex

***need to combine BOM with other boards to avoid repetition, and need to use std table format if remains as a table

The TTCrx chips are mounted on daughter boards called TTCrxDCU2 boards which integrate one TTCrx and one I^2C interfaced ADC DCU2 chip and are also used on the Tower Builder boards. Building such boards enabled to reduce production costs, as the TTCrx package requires to build high class PCBs and special cabling techniques. The hardwired addresses of the two TTCrx of the board are defined by switches located on the daughter board. The SPAC slaves can configure their attached TTCrx via I^2C commands on the I^2C line 0.

Finally, the Data port of the SPAC ASIC parallel interface is connected through pull-ups to the 6 power supplies of the board.

Test at the BNL crate setup ***shorten and redo

The final prototype of Controller was installed and tested successfully in Brookhaven with a SPAC Master VME64 6U board. Especially, the tests in BNL were focused on the following points:

- Good communication with all the boards in a fully loaded FE crate condition: a crate loaded with one Controller and 16 FEB/CALIB/TBB boards could be configured through SPAC with success. On the other hand, it was measured that the TTC fanout of the Controller and sending the TTC signal to the board through cables did not degrade in a significant manner the quality of TTC signal.

- Effect of SPAC activity on the coherent noise measured in the FEBs: The coherent noise of the different channels of the FEB was calculated when the SPAC bus is completely quiet because it is isolated from the MS fibers (SPAC Off), when the SPAC bus is not isolated from the optical receivers and a carrier is generated on the MS lines (SPAC On) and when frames are being sent on the bus. Typicallyhaving some SPAC activity on the bus increases by 5% the coherent noise on FEBs, except on the boards where the coherent noise is smaller. Whatever the situation, in any case, the coherent noise is always below 3% (to be compared to the requirement of less than 5%).

- Test of redundancy of the SPAC and TTC optical links: The reception of the TTC signal was tested on both receivers without difference. In the way, the duplicated MS and MS lines were also tested. Communication could also be performed with FEBs even when the Controller did not had a valid clock (test performed in Paris test bench), and with or without carrier on the download and readback lines.

- Effect of dead FEBs on SPAC (failure modes): like in Paris test bench, it could be possible to communicate with 1 FEB while the 15 other boards connected to the bus had their power supply off.

The OTx was tested to verify its performance for the relatively slow SPAC signals.

Production and Testing

All the different buses have been tested on a SPAC bus test bench to check the connections and the line impedances and then assembled on the FE crates.

A total of 135 FECont boards have been produced, while 122 are needed for the experiment. The following actions have been taken during the production process:

- The radtol commercial components bought correspond to the number required to equip the 135 Controllers plus 8% spare components.

- The OTx are custom made optical devices made by Academia Sinica Taiwan and tested with the same criteria as for the FEBs.

- The TTCrxDCU2 daughter boards have been produced and tested as an individual component.

- The SPAC slaves have been tested before cabling and a set of 5% spares remains for ATLAS operation.

- After the PCB fabrication, standard continuity tests have been performed.

- The cabling of all the components of the Controller (including the various daughter boards) have been done by the cabling company and the boards were submitted to a standard burn-in procedure.
- A burn-in sequence (with at least the power on) has been performed to each board together with a subsequent functionnal test.
- The quality of the TTC signals on each TTC output have been measured and registered.
- The SPAC functionality (SPAC slaves on the Controller and through the SPAC bus) have also been checked.
- The Controllers having passed the tests have been sent to CERN and registered into a dedicated production database.

***reduce and get rid of itemize

6. L1 Trigger Electronics

The LAr readout electronics must form and transmit to the L1 trigger system analog sums for trigger towers of typical size $\Delta\eta \times \Delta\phi = 0.1 \times 0.1$. The sums are made through a multi-stage analog summing tree. The stages are implemented in the FEB and Tower Builder/Tower Driver Boards mounted in the FEC, and in the L1 Trigger Receiver/Monitor System mounted in USA15.

6.1 Tower Builder Board

The Tower Builder Board (TBB) is a link of the Level 1 (L1) trigger chain for teh EM calorimeters.

The L1 trigger is designed to deliver to the back-end ADCs an analog signal per trigger tower of the calorimeter (3584 trigger towers in total), each signal being proportional to the transverse energy received by the trigger tower. In the Barrel, a trigger tower is a $\Delta\eta \times \Delta\phi = 0.1 \times 0.1$ section of the calorimeter, containing 60 cells distributed among four layers in depth. In the Endcap, the granularity and the cells quantity by trigger tower depend on the η value. Each ADC takes five samples of its corresponding analog signals, and these samples are used to estimate the energy in each tower and so to trigger (or not) the acquisition.

The trigger signals are made by successively adding the signals coming from all the cells of a same tower. This summation is done in two steps: the FEB adds all the signals of a same layer (in the Shapers and Layer Sum Boards), and the TBB adds these four signals coming from each layer.

To summarise, the three functions of the TBB are the adjustment of the input signals shape, gain and delay, the addition of these signals tower by tower, and the driving of the resulting output signals to the back end Receiver in the control cavern, through a 70 m 16-twisted pairs cable.

TBB Requirements - delete title?

The transverse energy is the important quantity. The signal amplitude at every TBB output should be linear with the transverse energy; the integral nonlinearity should be better than 1% for the range of amplitude up to 2.5 V. The gain should be of 2.5 V for ET = 256 GeV for every trigger tower and for every energy distribution between the layers. The gain precision should be better than 5%.

The TBB output signal should have a peaking time of 35 ns, within a few ns. The saturation of the trigger chain is a normal working mode of the trigger. The signal amplitude at the TBB output should not be below 2.5 V when saturation occurs. This implies clamping at all gain and summation stages to avoid the deformation of the decreasing edge. The noise of total trigger chain is expected to be less than 400 MeV (E_T) per trigger tower at η = 0, and the TBB contribution should be negligible.

TBB Architecture **delete title?

One TBB (see Figure 14) includes 32 summation cells (the "towers") devoted to the analog summation, trigger tower by trigger tower, of the signals coming from the 4 layers of the detector (Presampler, Front, Middle, and Back). Each TBB therefore contains 32 $\times$ 4 analog inputs and 32 outputs.

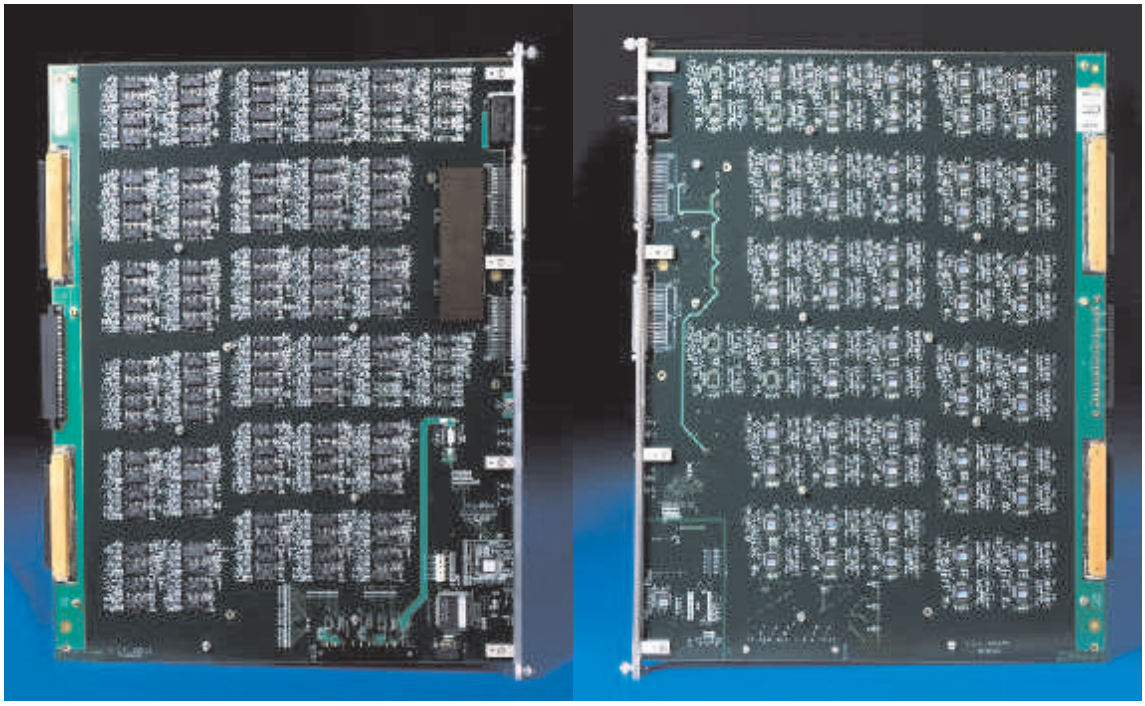

Figure 14. Photographs of both sides of the Tower Builder Board. The 32 analog summation cells of four channels each can be recognised.

Figure 15 shows the schematic diagram of one of this summation cells. Each summation cell is made of six stages (labelled A to F in Figure 15): A) the input receiver (50 Ω termination; gain = -2), B) the pole zero compensation (it adjusts the signal peaking time by integration or differentiation depending if C1 or C2 are removed/short-circuited or not, and compensates the resulting amplitude modification by gain; the magnitude of these corrections is adjusted channel by channel by varying the values of R1, R2 and R3), C) the delay line (it compensates the differences in cable lengths and values of particles flight time between the four inputs; an analog multiplexer (the Bimux) under software control allows to choose among 8 delay values from 0 ns to 17.5 ns), D) the delay line

receiver (100 Ω adaptation; gain = 2), E) the weighted linear mixer (the gain of each channel is adjusted before summation with R7, so that the output amplitude is 2.5 V when ET = 256 GeV ; the amplifier is clamped to limit the saturation), and F) the output differential driver for the 70 m twisted-pair cable that delivers the signal to the counting room.

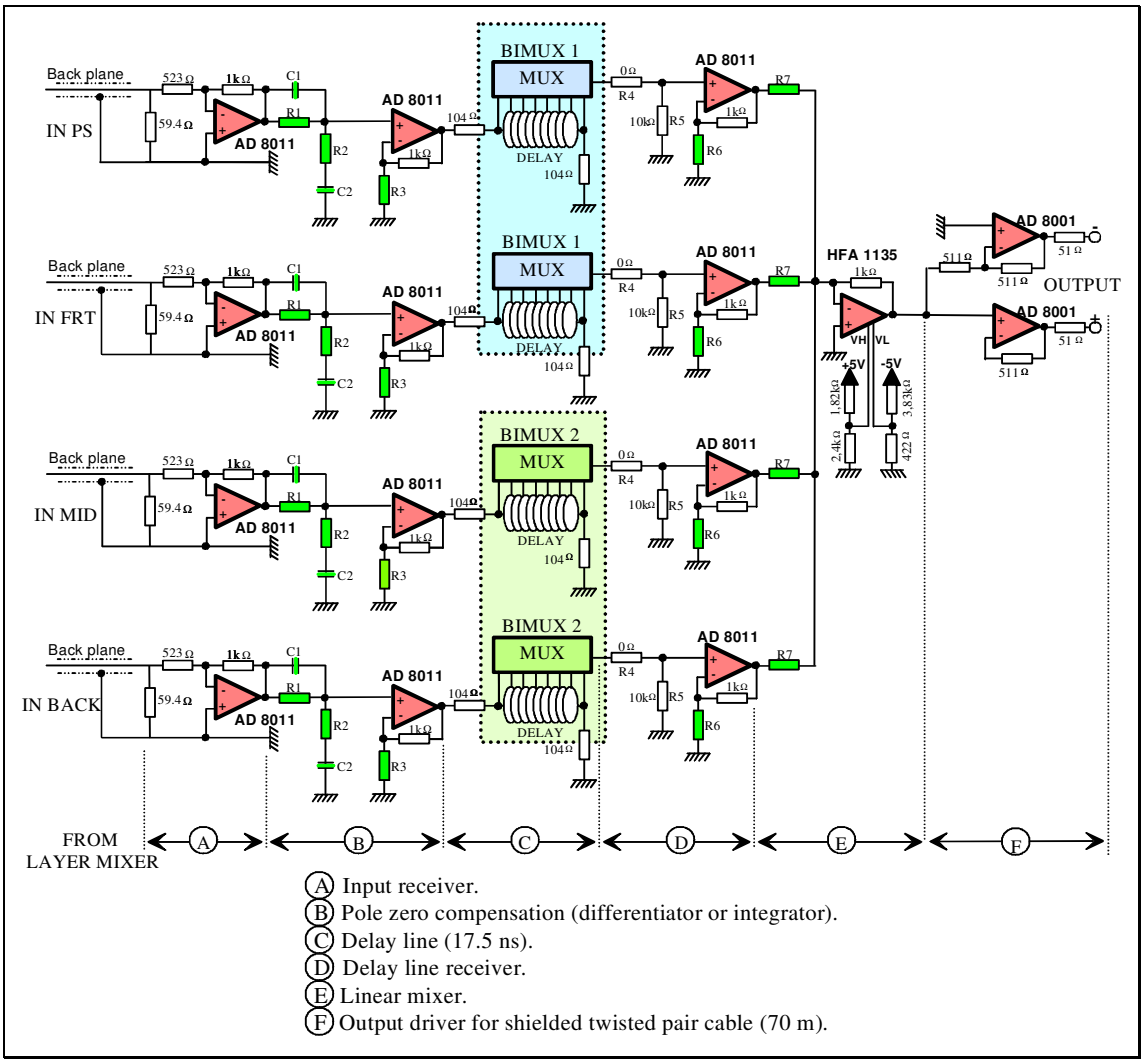

Figure 15. Schematic diagram of one of the 32 analog summation cells of the TBB. See the text for more details.

As the compensations before summation change from one trigger tower to another, the value of some components changes from one summation cell to another. These components are R1, C1, R2, C2, R3, R6 and R7. Their values are different according to the cell, but equal from one TBB to the other, thanks to the cylindrical symmetry of the detector. These components have been calculated from Spice simulations validated by measurements (see Reference [13] for more details).

As it as been shown, the value of certain passive components in each of the board summation cells differs from one cell to another and depends on the electrical characteristics of the concerned

trigger towers. But this variability is attenuated by the cylindrical symmetry of the detector. So to cover all the possible configurations, five versions of TBB boards are necessary : one for the Barrel crates, one for the Standard End Cap crates, and three for the Special End Cap crates. The PCB and the design of these five versions are identical. The only differences between them are the number of cabled towers (certain towers are not cabled), the number of channel in certain towers, and the value of the "variable" components in every towers.

A logic interface is included in the board and devoted to its control and command through the SPAC bus. Four functions are implemented: read/write of the Bimux registers (that determines the delay line output used), control of the board power supply and temperature, reset the logic interface itself, and read the serial number of the board. The logic interface contains four mains chips : the TTCRx, the SPAC 3 Slave, the DCU2 and one Bimux. The TTCRx provides, from the TTC signal, the 40 MHz clock and the reset signal. The SPAC 3 Slave circuit receives the read/write commands and data from the SPAC bus. The DCU2 circuit contains a 12-bits ADC that is used for the monitoring of the supply voltage and of the temperature given by its on-chip sensor. The BiMux circuit is used here to read the serial number that is allocated to each TBB at the time of its production. ***reorganize/shorten this para

TBB Performance

***can shorten this section??

This section summarises the performances of the board, as measured in our laboratory on the Barrel prototype in its final configuration. More details can be found in References [**?**] and [**?**].

The linearity measured in the linear zone (0 V $\rightarrow$ +2.5 V) is contained between +0.2% and -0.6%. The maximal crosstalk between towers is 0.8%. The maximal offset value measured at each TBB differential output is 70 mV on positive and negative. The equivalent noise of one TBB tower at the Receiver output (and so including the transfer function of the 70 m cable and the receiver) is 0.22 mV. The saturation level measured at the outputs of the prototype is 3 V $\pm$ 200 mV.

Each TBB input channel has been tested injecting a reference signal, and comparison of the measured amplitude and peaking time with Spice simulation has been performed. The maximal amplitude error is $\pm$1%, and the maximal peaking time difference is $\pm$ 0.4 ns. The differences between measurement and simulation are due to the limited precision of the Spice model, and the 1% precision of R and C components.

The trigger chain is designed to deliver a signal rising linearly with transverse energy up to 2.5 V at 256 GeV, and for energies above this value the signal should not decrease below 2.5 V. The behaviour of the saturation is controlled by placing operational amplifiers with clamping at all amplifying stages of the trigger chain. However despite this, due to the presence of the shapers that behave like a derivative of the signal, the increasing signal at the chain output is not a priori assured (see Figure 17). In some configurations, the signal amplitude at saturation (when ET is beyond 256 GeV) could be lower than the signal amplitude for ET below 256 GeV, and that could induce trigger errors. This type of behaviour would be totally unsuitable for a trigger system. So it has been important to verify that our trigger system does not suffer from it. The saturation has been studied using three tools : a test bench that reproduce one channel of the trigger chain, one detector module and its electronics during beam tests, and a Spice model of the trigger chain that includes all its channels.

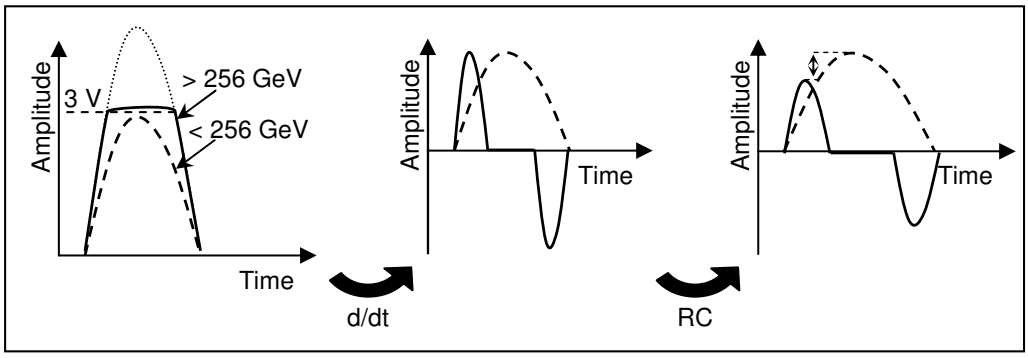

Figure 16. Diagram of the possible undesirable behaviour of saturated signals. Non-saturated signals (ET < 256 GeV) are represented by dashed line, whereas saturated signals (ET > 256 GeV) are represented by solid line. : Both signals at the input of the shaper. : Signals at the output of the shaper behaving like a derivative of the signal. : A possible signal shape after the shaping of the TBB and the receiver - the amplitude of the saturated signal is smaller than the amplitude of the non-saturated signal, inducing trigger error (it is even worse if the signal is sampled at a fixed time : at the peak middle, the saturated signal can give 0). ***fig needed?

The important point is the amplitude finally digitised by ADC. The ADC takes 5 samples separated by 25 ns from the receiver output. The evolution of the amplitude at these five samples is measured when the injection, and thus the energy, is increasing. As an example, Figure 17 shows one of these plots measured when the signal is injected in one unique cell of the middle layer, at η = 0.3. Figure 17(a) represents the receiver output signal versus time for increasing energies (the 256 GeV reference signal is in bold line, and the five sample placed as previously explained are in dotted lines). This figure is used to calculate the Figure 17(b), which represents, versus energy, the signal amplitude at each sampling time. We have made these measurements for many different values of η and layer, controlling that the amplitude of the central sample (line “3”) doesn’t decrease below its level at 256 GeV over all possible configurations.

But when an electromagnetic shower occurs in the calorimeter, it induces signals not in only one, but in numerous cells of the four layers. So we have simulated this with Spice using different shower profile. The same conclusion is reached, namely that in all cases the amplitude at the chain output is linear up to 256 GeV, and that it doesn’t decrease below its value at 256 GeV.

The total quantities of boards produced is 135, and the total quantity of board installed is 120 (15 additional boards have been produced as spares). The quality of the produced boards has been controlled during all the production. The main parameters to control were the amplitude and the width of the output signals when signals similar to the physical signals of the experiment were injected at the input. Table **??** show the results of these controls. The gain standard deviation is about 0.5% for each board version, and the gain maximal deviation is between 3.2% and 1.5% according to the board version. This is below the required maximal deviation (5%). Concerning the signal width, the standard deviation is about 0.25 ns and the maximal deviation is around 1 ns. Again, this is below the required deviation (a few ns). Most of these dispersions between boards are due to the precision of the used components (1%).

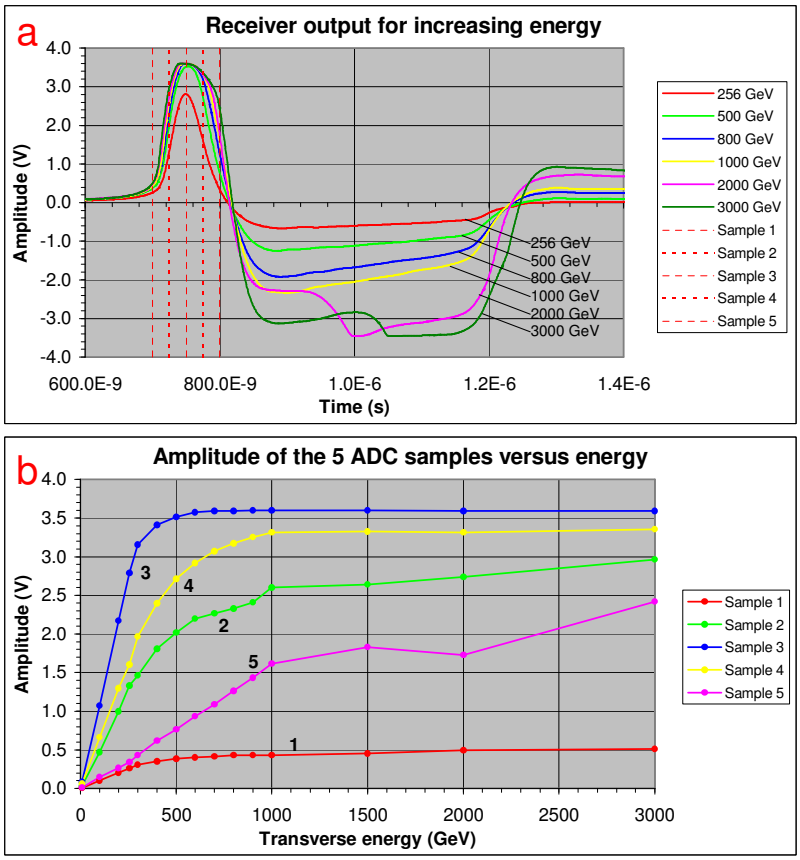

Figure 17. (a) Receiver output signal, versus time, measured for increasing energies on our test bench (the 256 GeV reference signal is in bold line, and the five sampling instants in dotted lines). b) Evolution of the five sample amplitudes versus energy, extracted from figure a measurements (the points of figure b are the intersection between solid lines and dotted lines of figure a). N.B. : The Receiver's gain is 0.73, instead of 1 in final the Receiver, reason why the amplitude of sample 3 for 256 GeV is not 3 V, but 1.9 V. ***re-word

Type		EMB	EC Standard	EC Special 0	EC Special 1	EC Special 2
No. of TBB (incl. spares)		70	35	10	10	10
Gain Error (%)	Std. dev.	0.52	0.55	0.49	0.54	0.50
	Max. dev.	3.05	3.19	2.32	2.39	1.52
Width Error (ns)	Std. dev.	0.26	0.29	0.23	0.26	0.22
	Max. dev.	1.28	1.03	0.70	0.99	0.69

Table 4. ***need to write

6.2 Tower Driver Board

The trigger sums for the Hadronic Endcap Calorimeter (HEC) are formed by summing the longitudinal depth segments at the same η, ϕ coordinates. This summation is performed by the Linear Mixer (LM) of the shaper chip in the FEB. In contrast to the EM calorimeters, therefore, no further summation of signals is needed for the HEC L1 trigger system. The same is true of the forward

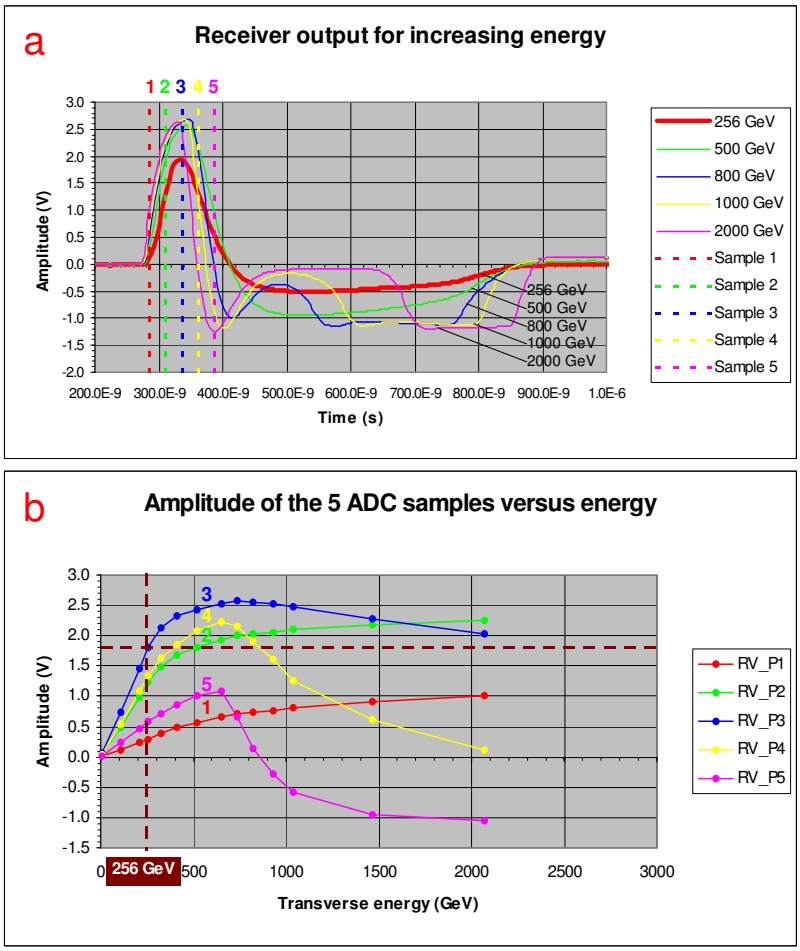

Figure 18. (a) Simulation of the receiver output signal versus time for increasing energies (solid lines) for one electromagnetic shower, and the five samplings (dotted lines). b) Figure calculated from figure a simulations, and representing versus energy the signal amplitude at the sampling instants

calorimeter (FCAL). Therefore, instead of using a TBB as described in the previous section, the HEC and FCAL crates include a Tower Driver Board (TDB). The functions of the TDB are to receive via the baseplane the trigger sums from the LSBs on the various FEBs, convert them into differential signals with approximately unity gain, and drive these differential signals over the 70 m trigger cables to the Receiver system in USA15.

Specifications of the TDB performance are summarized in Table 5. A schematic of one trigger channel of the TDB is shown in Figure 19. The single-ended to differential conversion is performed using the same AD8001 as on the TBB, to take advantange of the radiation qualification performed of these devices.

The TDB is implemented as a six-layer PCB with the same physical dimensions as the other boards in the FEC. Each TDB contains 96 channels. A photograph of a TDB is shown in Figure 20. The total of 192 amplifier chips are all mounted on one side of the PCB, and placed near the input connectors at the bottom of the figure in order to minimize the trace length for the input signalgs

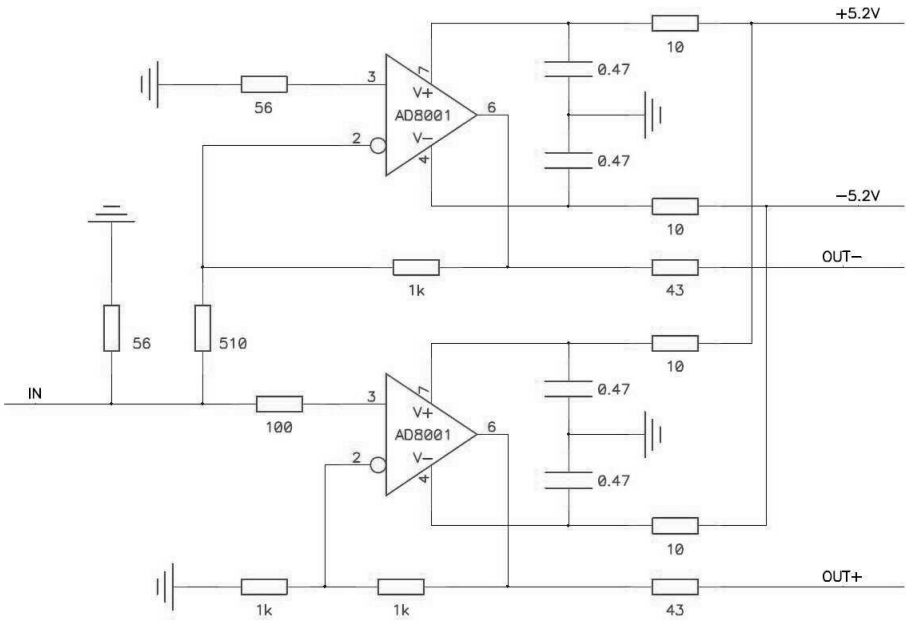

Figure 19. Schematic of one trigger channel as implemented on the Tower Driver Board.

from the FEBs. The six output cable connectors are mounted along the front panel at the top of the figure. Since the TDB is strictly an analog board, with no external control, the TTC and SPAC signals are not connected to the TDB.

The TDB gain and rise time in response to a step function input were mesured for the 96 channels of the preproduction TDB. The mean gain is 0.98 and the channel-to-channel variation of 0.3% is well below the 1% specification. Similarly, the mean rise time of 0.68 ns is well below the 2 ns specification. ***need to refer to fig. 21

The TDB power is very low (< 15 W), so water-cooled cooling plates are not required. Instead, simple aluminum plates are mounted on both sides of each TDB for Faraday shielding as well as protection of the active components.

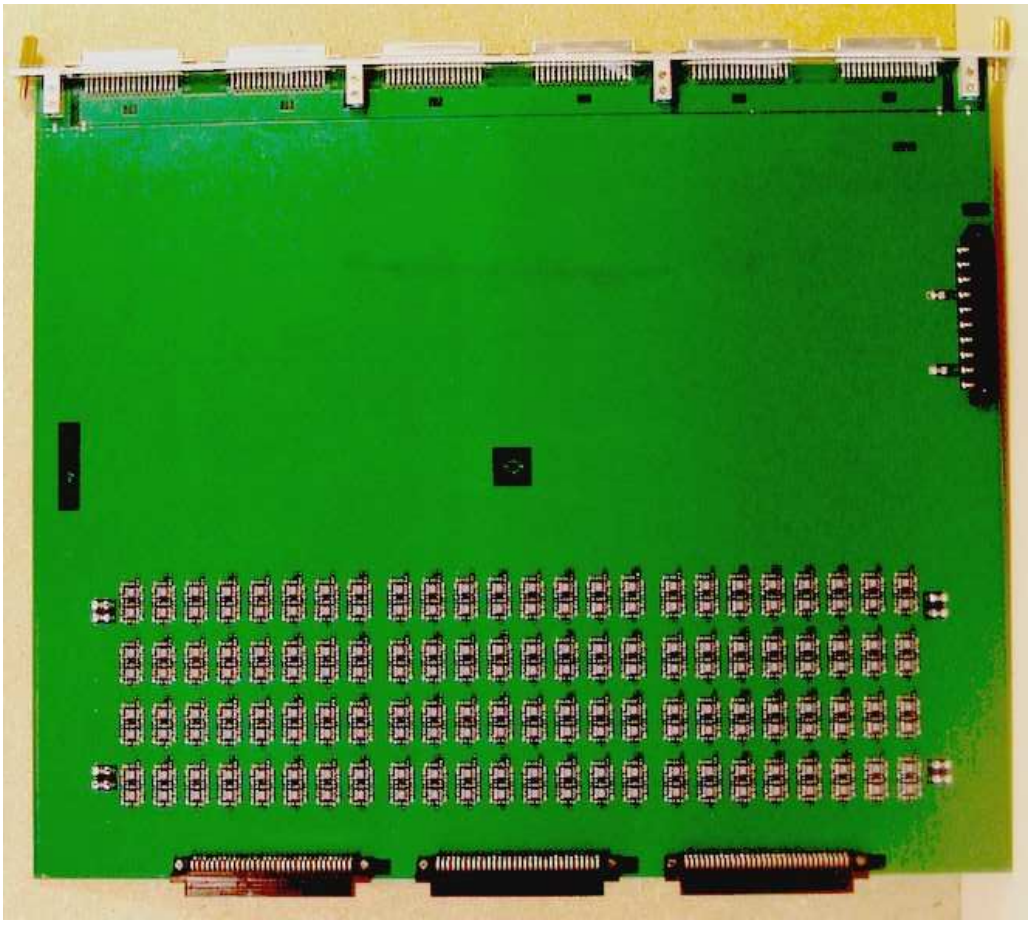

Figure 20. Photograph of the Tower Driver Board.

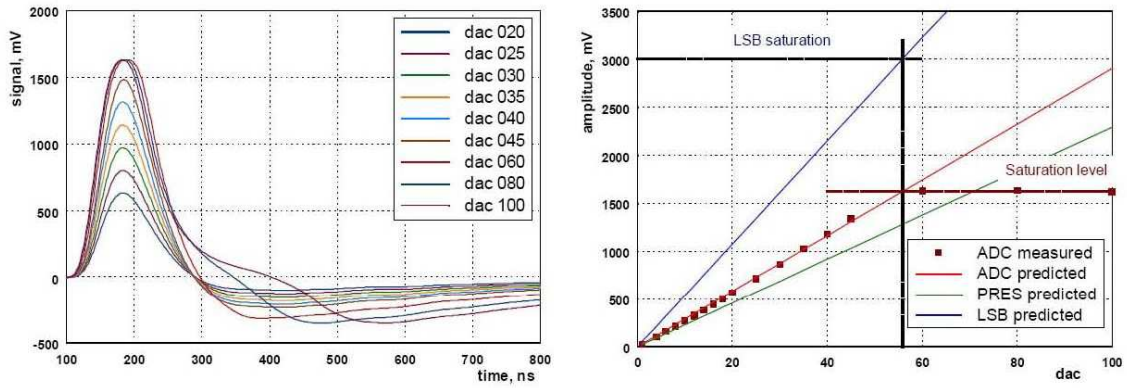

Figure 21. Pulse shapes for the Tower Driver Board.***is this the right figure to include? was using prototype? ***use only left plot

6.3 L1 Trigger Receiver/Monitor System

The receiver system in ATLAS is the electronics at the interface between the FE electronics of the calorimeter systems and the Level 1 Calorimeter Trigger. ***stress is located in USA15, and used also for TileCAL

The system consists of 8 crates, 4 on each side. The system has the following functions (**shorten since details given later, or move after Fig 22):

a) Differential receiver. The analog trigger signals are sent from the detector to USA15 over shielded twisted-pair caibles, containing 16 pairs each. The first section of the Receiver is a wideband stripline transformer, which converts the signal from differential to single-ended format.

b) Gain adjustment. A critical active element in the receiver is the variable gain amplifier whose gain is set by a DC voltage provided by a 12-bit DAC, configured such that the gain of each receiver channel can be varied between 0 and 4.

c) Reordering of signals. The signals arrive at the receiver in an order determined by the physical properties of the calorimeter. The L1 electronics requires signals ordered in a specific pattern in (η, ϕ) space. This reordering is done via a "remapping" daughterboard located on each Receiver.

d) Summation. Most of the summing of the L1 trigger signals is carried out in the on-detector electronics. However, there are certain cases where it is necessary to make additional sums in USA15. These are done in both the Receiver and the L1 preprocessor.

e) Monitoring. In the main readout, the signals are digitized in the FE electronics. Thus the only place where analog signals can be examined is in the trigger sums. The Receiver system contains a monitoring pickoff for each Receiver channel, and routing circuitry permits any input signal to be routed to any output of either of the two monitoring modules in the crate.

f) Differential driver. The outputs of the receiver are sent to the L1 preprocessor module over twisted pair cables identical to the input cables. The final stage of the receiver electronics chain is a transformer-coupled differential driver.

The chain of electronics which accomplishes these requirements is shown in Fig. 22.

Description of the Receiver system

The four receiver crates on either side of the detector (A or C side) house the receiver electronics for different parts of the calorimeter system (EMB, EMEC, HEC and FCAL, TileCal).

The receiver crate is made up of four different type of modules, all in 9U VME mechanics, but as this is an analog system, no VME protocol is used. The system is housed in a standard 9U crate outfitted with a custom backplane. The modules in the receiver crate include transition modules (16 per crate), receiver modules (16 per crate), monitoring modules (2 per crate), and one controller module per crate.

The transition module, containing completely passive electronics, is a PC board 12 cm deep. The other three modules are 400 mm deep PC boards which are plugged into the front of the crate. Each of these modules is discussed below. More detail on the system is available in Reference [15].

The transition module resides in the back of the crate, in the slot occupied by the receiver with which it is associated. Trigger cables from UX15 are plugged into the connectors on the front panel of the transition module and the signals, after conversion to single-ended mode, are fed to the receiver through the connectors on the backplane. Transition modules for three of the four crates are identical; the transition modules for the EM barrel have an additional connector to permit four of the input signals to be routed to the EMEC crate. This provision is required since one of the trigger towers is split across the barrel and endcap, and the summing of the two halves of this tower is carried out in the receiver system.

A schematic diagram for the signal chain is shown in Fig.22. After passing through the 1:1 input transformer, where the conversion from differential to single-ended mode is carried out with the output inverted, the signal enters the VGA (variable gain amplifier) daughterboard. Here it is inverted again and amplified by a gain (max value=2.0) to adjust the signal level to its correct amplitude (10mV=1 GeV at the ADC input). The gain is changed by adjusting the value of a DAC which is also located on the VGA daughterboard. A DAC value of 4096 corresponds to a gain of 2, while a DAC value of 0 corresponds to a gain of 0. At the exit of this daughterboard, the signal, which is bipolar with the first lobe negative, is sent to both a buffer amplifier and to the remapping board. The signal in the monitoring branch is sent to a buffer amplifier, where it enters the monitoring circuitry. The signal sent through the remapping board becomes transposed in its position among the output signals to the ordering required by the L1 Calorimeter Trigger. It then undergoes RC shaping (τ=5 ns) to provide bandwidth reduction and amplification by a fixed gain of 2. This factor of 2 serves as an approximate compensation for the attenuation in the long cables from the detector. A differential driver consisting of an amplifier and a 1:2 wideband transformer converts the signal back to differential mode (with its original polarity) for transport over twisted pair cables to the L1 preprocessor.

The maximum voltage at this point is set by the voltage-limiting op amp HFA1135 to be 3 V, whereas the range of the ADC in the preprocessor module is set to 2.5 V, corresponding to 250 GeV of transverse energy. The gain of the circuit consisting of the differential driver on the receiver and the differential receiver on the preprocessor is unity, so the difference in amplitude ($\approx$ 10%) between the signal level at the output of the HFA1135 in the receiver and that seen by the ADC in the preprocessor module is due to attenuation of the $\approx$ 10 m twisted pair cable between the two units and the final RC shaping of τ=5 ns in the preprocessor.

The receiver motherboard has 64 channels, and contains four VGA daughterboards, one remapping daughterboard, and one SCDB (serial control daughterboard).

The remapping board [20] is a 253 mm $\times$ 50 mm PCB located in the center of the receiver motherboard. Its purpose is to change the ordering of the signals from the input ordering to the one required by the L1 system. It is, in most cases, totally passive, the exception being for the case where two-fold sums are carried out in the receiver.

The SCDB sends and receives digital data over the crate backplane. Mounted directly on the receiver motherboard are the shaper/driver circuitry and the circuitry for driving the monitoring lines, which are located in the crate backplane. A photograph of the receiver and transition modules

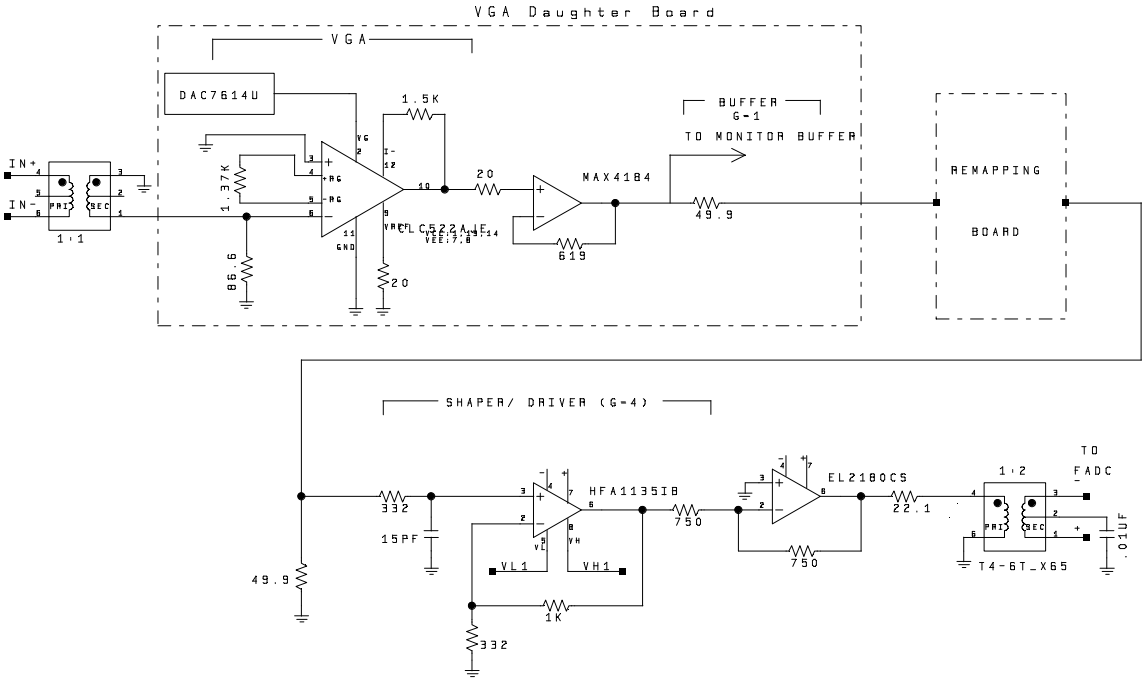

Figure 22. Diagram of the analog circuitry which performs the signal processing for one channel of the Receiver. The trigger sum cable is incident at the upper left, and the input to the cable to the L1 preprocessor at the lower right.

in a test bench setup is shown in Figure 23.

Monitoring is accomplished in this system by picking off an input signal and routing it into one of 16 monitoring channels. Two monitoring boards, each handling 8 channels, present the output of the monitoring lines on two output connectors, one with shaping identical to the signal output and the other with additional filtering, designed to have sensitivity to different regions of the noise spectrum. The heart of the monitoring circuitry is a crosspoint switch (AD8114), located physically on the VGA daughterboard. This device routes a signal on one of its 16 inputs to any of its 16 outputs. The four crosspoint switches in a receiver module are bussed together in such a way that any of the 64 channels in a receiver module can be routed to any of the 16 monitoring channels. The signals pass through a buffer amplifier with an output enable (HA4600). In the monitoring module, the same chip is used (see Figure 24) to select which of the receiver modules are to be transmitted to the monitoring outputs. Enabling the signal at both the source and receiver ends is not logically necessary, but this arrangement reduces possible crosstalk between the active and inactive monitoring lines in the backplane. The gain in the receiver chain is chosen to make equal the monitoring signal and the signal on the front panel of the receiver. Due to attenuation in

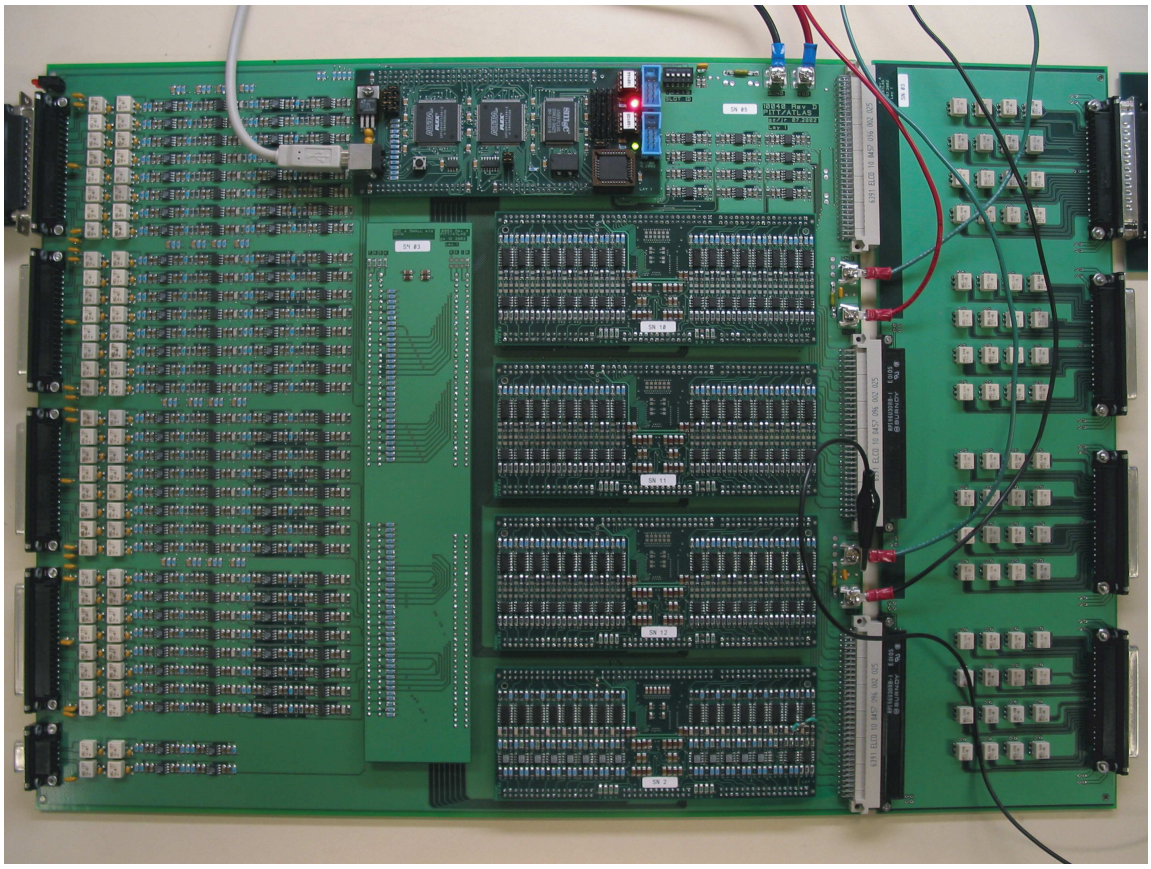

Figure 23. Photograph of the receiver and transition boards in a test setup. The signals enter on the right side at the front panel of the transition module. The elements through which the signals pass can be identified (right to left) as (1) input transformers, (2) backplane connectors, (3) VGA daughterboards, (4) remapping board, (5) output drivers, (6) output transformers, and (7) output connectors on receiver motherboard. The SCDB, top center, is a special testbench version with a USB interface, permitting direct control of the receiver module with a computer. Monitoring line drivers are located just to the right of the SCDB.

the backplane, which depends on the position of the receiver, this equality is accurate only to the level of a few percent.

The receiver system is controlled from a computer via its USB port. The controller module, which resides in slot 1 of each receiver crate, contains two USB ports. One is dedicated to the data acquisition system and is the port through which all digital data are transmitted, including gain data as well as monitoring setup data, and identification information is read from the receiver modules. The second port is used only for monitoring purposes, and it therefore has a more restricted instruction set available to it.

Communications are carried out between the controller and receiver or monitoring modules using a serial link running at 6 MHz. As mentioned above, each receiver or monitor board contains an SCDB, which communicates with the controller and carries out the required digital operations on the board. More information on the digital communications in the receiver system is contained in Reference [16].

Due to the fact that the receiver module must rearrange the order of signals between its input

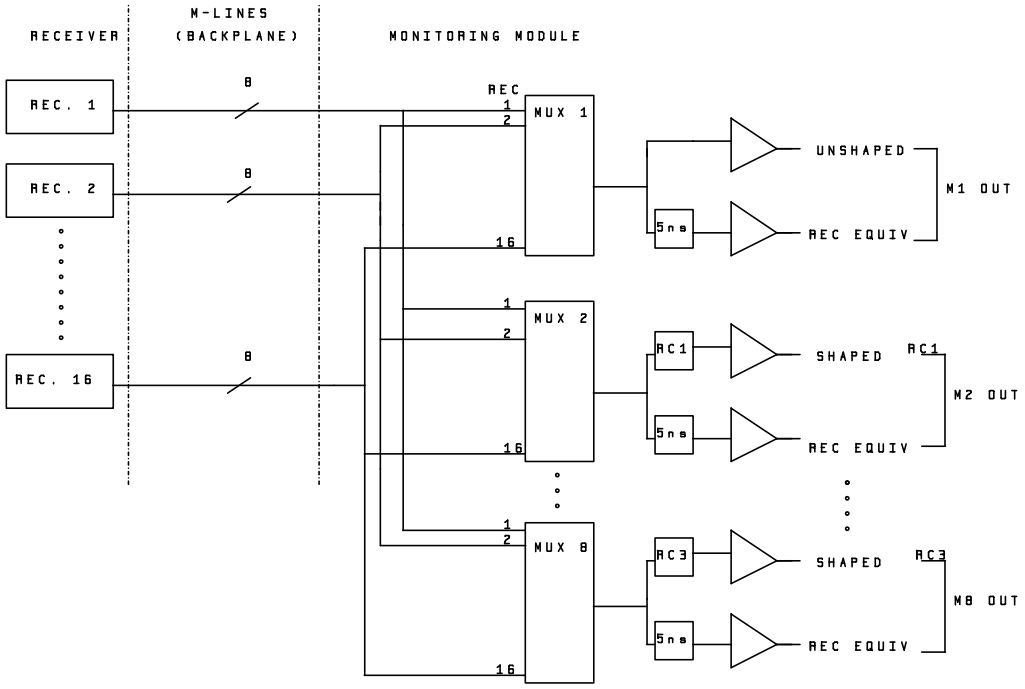

Figure 24. Block diagram of the monitoring module. For more details, see the text. ***fig not needed?

and output, it is of utmost important that receiver modules are placed in the slot for which they were configured and that each module is correctly configured for its slot. For this reason, all daughterboards and the receiver motherboard have been given electronically readable ID numbers.

The backplane in the crate has several functions. The receiver and monitoring modules each contain three 96-pin DIN connectors which mate with connectors on the backplane. On the receiver, the two lower connectors transport the signals from the transition module into the receiver module. The upper connector is used to transmit digital signals from the controller to each receiver module over a common set of lines, which are carried by the backplane. This connector is also used to transport the 16 monitoring signals out of the receiver module. On the monitoring module, the two lower connectors are used to input the 128 monitoring lines from 16 receiver modules, and the upper connector is used for digital communications. The traces in the backplane carry the monitoring signals from the receivers to the monitoring boards. Monitoring lines 1-8 are sent to monitoring board No. 1, which resides in slots 2 and 3, while lines 9-16 are transmitted to monitoring board No. 2 in slots 4 and 5. Power is also distributed over the backplane, using the power bus provided by the crate manufacturer.

Analog power for the system is provided by two 100 Ampere power supplies running at ± 5 V (one for each polarity). Digital power is provided by an identical but separate +5 volt power supply. A full crate consumes about 730 watts, and is air cooled in a closed rack with recirculating water-cooled air.

Performance tests

Several automated test stations were set up to evaluate the motherboards and daughterboards in the receiver system during the acceptance tests, which were carried out in laboratories at the University

of Pittsburgh. A complete discussion of the testing program is contained in Refreence [17]; here we give the salient results of the more important tests.

The most critical component in the analog chain is the VGA, which has its own test bench where each unit was evaluated thoroughly for dynamic range and linearity. In Figure 25 is shown how the integral nonlinearity is evaluated for each channel of this daughterboard. In this test a standard value of the DAC (2700) is used, which corresponds to a gain of about 1.4. A DC signal is ramped at the input, from -3.5 V to +3.5 V, and the output is measured on a digital voltmeter, yielding the DC response curve for each of the 16 channels. The slope of this curve is the gain, which is evaluated separately for each channel. The integral nonlinearity is evaluated separately for negative and positive voltages. Note that the response curve is asymmetric, with a larger dynamic range on the negative side, and this gives rise to a lower integral nonlinearity for negative voltages. This is a property of the CLC522 chip, and is the reason that we have chosen a double inversion of the signal in the receiver, which results in the leading lobe of the pulse in the CLC522 being negative.

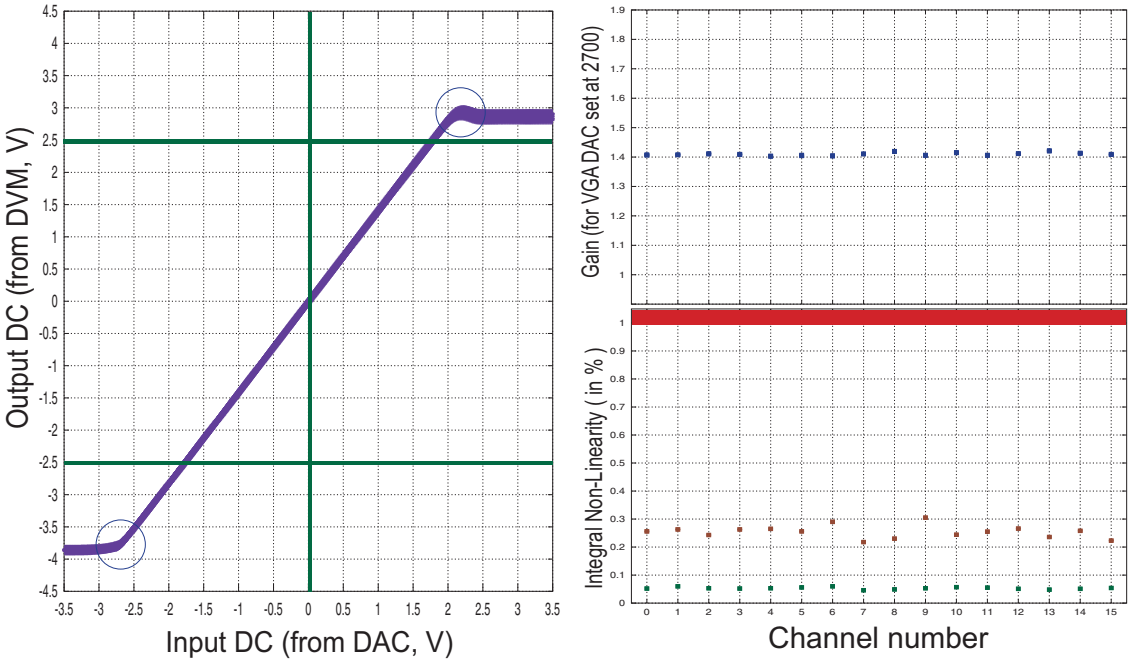

Figure 25. Left: DC response curves of the 16 channels of one VGA board, with all channels set at DAC=2700. The black oorixontal lines represent the maximum signal height expected. The slope of each curve yields a value for the gain, which is plotted in the upper right hand graph. Integral nonlinearity is evaluated separately for the positive and negative portions of the response curve, and the values are plotted in the lower right hand graph. The lower set of points (all below 0.1%) are for the negative region and the upper set of points (between 0.2 and 0.3%) are for the positive region. The heavy black line at 1% represents the specification for the nonlinearity for the entire electronics chain in the receiver.

Another quantity which is measured for the VGA is the variation of the gain as the control voltage is varied using the DAC on the VGA daughterboard. This relationship is a linear one, and the behaviour can be quantified as a nonlinearity, but in our application it is not essential that the

gain vs voltage relationship be linear, as the gains are set iteratively. The gain nonlinearity is better than 1% over the full range. ***shorten and combine with previous para.

One of the more important quantities measured in our acceptance tests is the overall integral nonlinearity of the receiver circuit. This measurement, carried out with bipolar pulses of 38 ns rise time, simulates closely the situation encountered in the experiment. Due to the short rise time of the pulse and the relatively long RC time constant of 15 ns (later reduced to 5 ns) the midrange gain of the channel is 1.7 instead of its DC value of 2.0.

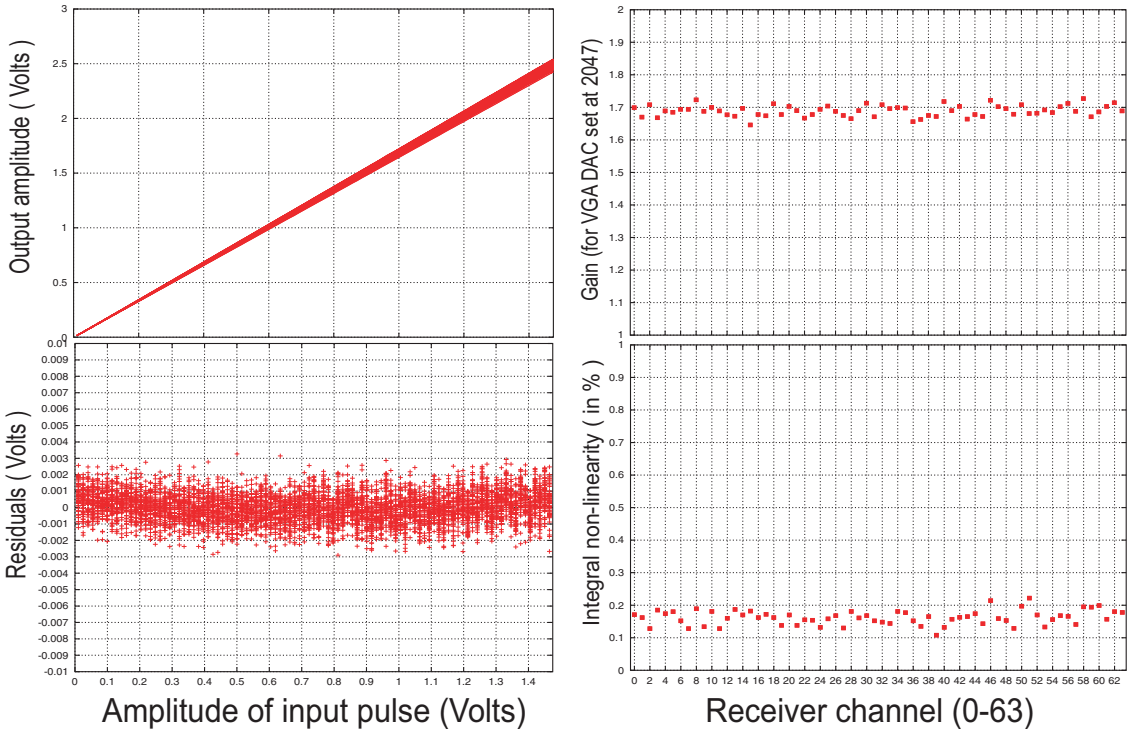

Figure 26. Pulse linearity test of the 64 channels of a receiver board, with all channels set at DAC=2047. Upper left: Response curve for a bipolar pulse of 38 ns rise time. Lower left: residuals of linear fit of response curve. upper right: gain value for each channel. Lower right: integral nonlinearity (for maximum output pulse height of 2.5 V) for each channel. ***not needed?

Another important aspect of the receiver is the noise which is injected into the system by the receiver module. The noise is dominated by the contribution from the CLC522 chip, which, according to a model given by the manufacturer [18], depends upon the gain of the circuit. In Fig. 27 we show measured values of the noise at the output of the receiver, along with the evaluation of the noise model for our circuit. The dependence on gain is well described by the model, but it gives values which are some 10% higher than our measurements. We view the agreement as reasonable, given that we are operating the chip with very low gain (G=2) compared to common applications. The maximum noise seen in the test (where τ=15 ns) is about 0.5 mV, corresponding to 50 MeV. Reduction of the time constant from 15 ns to 5 ns increases the noise to about 0.7 mV or 70 MeV. Typical values of noise in the trigger sums are $\approx$ 500 MeV.

Tests of the digital logic of the system were also made in an automated test bench into which was integrated a Tektronix Prism 3001 Logic Analyzer. Commands were downloaded into the

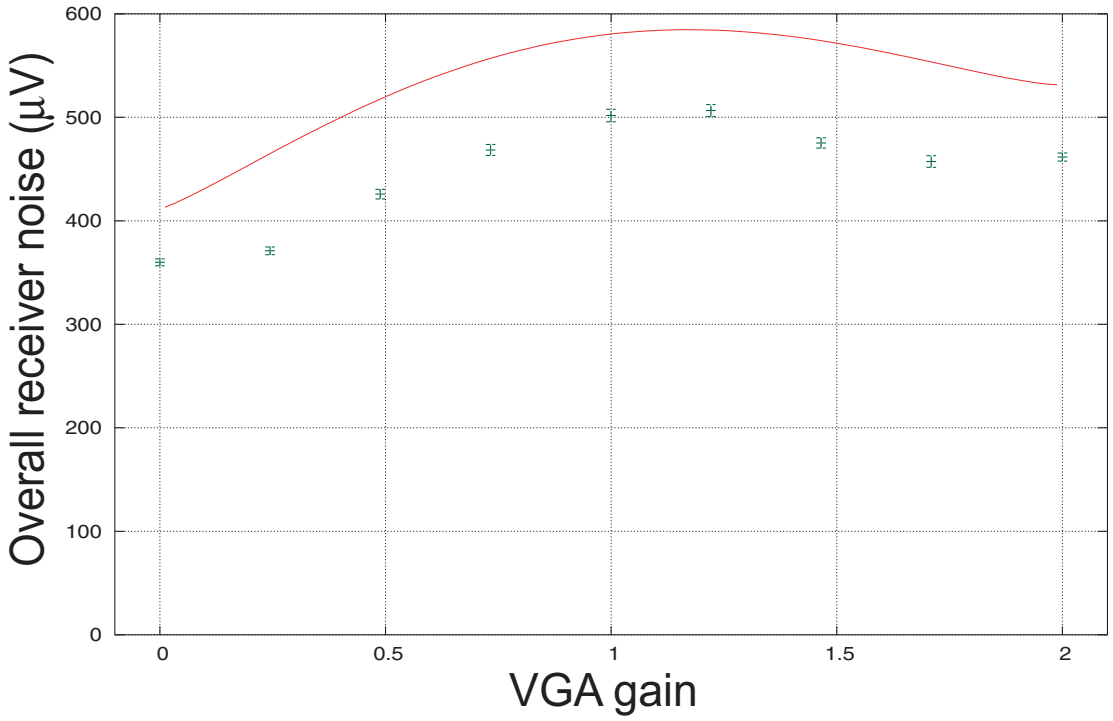

Figure 27. Receiver noise vs gain, as measured with a wideband RMS voltmeter at the receiver output. The solid curve is an evaluation of the noise model provided by the manufacturer of the CLC522 for our particular circuit.

controller, and its output bit pattern in the internal serial link was recorded in the logic analyzer and compared to a standard pattern, produced by a controller known to be operating properly. Similar tests were carried out for each SCDB. Any board which failed a test was either repaired, or, in rare cases where repair was not possible, rejected.

Tests of two passive components–the remapping boards and the crate backplane– were also part of the test program. The position of output vs input signals was measured and compared with the required mapping [20]. For the backplane tests, a receiver module was moved systematically from slot 6 to slot 21 while automated performance tests were carried out. This test not only checked the proper connectivity of the backplane but also validated the operation of the serial link over the full length of the communication paths in the receiver crate backplane.

Implementation in ATLAS ***can move this earlier and just give refs?

Information relevant to the implementation of the receiver system is ATLAS is contained in several internal ATLAS documents. One [19] contains tables indicating how the cabling of the system between the detector and the receiver system is done, as well as the detailed composition of the receiver crates. Another [20] contains the specifications for each of the remapping boards, *i.e.* the relationship between the order of the receiver input and output signals. A third [21] summarizes the connectivity of the L1 Calorimeter Trigger signals from the signals on the detector to the inputs of the L1 processors and establishes naming conventions for the receiver input and output signals.

Remapping boards

There are a total of 22 remapping boards defined for the entire receiver system, but in one case, the specifications for two boards (EMB and Tilecal, side A) overlap completely, so the same board serves both purposes. Most of the boards are completely passive, but on six of them (three on each side), twofold sums are carried out:

1. Summing of EMB and EMEC portions of the shared trigger tower. The trigger tower in the region $1.4 < |\eta| < 1.5$ is split between the EM barrel and EM endcap, which are in separate FECs. The portions within each calorimeter are summed in the appropriate TBBs, but the sum of the two halves needs to be carried out in the Receiver. This is done by splitting off 4 signals from each transition module in the EMB and bringing them as inputs into the EMEC transition module at the corresponding value of ϕ. Summation is carried out in the remapping board in the EMEC receiver.

2. Summing of FCAL η bins. The η granularity of the FCAL trigger sums reaching the receiver is 4, whereas the current L1 trigger has only one bin in η. The higher granularity may be exploited in the L1 trigger at a later date, but at the start of the experiment, it is necessary to reduce the η granularity ahead of the L1 processors. In the preprocessor, it is possible to create a digital sum of four, but in the case of FCAL2 and FCAL3, both hadronic calorimeters, an additional two-fold sum is required to add together the two hadronic sections. Thus one level of summing is carried out in the receiver. Due to the similarity of signal shapes, a sum of neighbors in η is made in the receiver, leaving the remaining summuations to be done digitally.

7. Frontend Crate Infrastructure

7.1 FEC Mechanics

Dimensioning of the crate and pedestal has been done with the aid of finite element analysis (FEA). The total weight of the electronics installed in the crate is approximately 190 kg. Crates mounted at 90° present the largest problem. At this position and with crates mounted from its base stresses may induce deformation of the crate which may result in difficult insertion and extraction of boards. Stresses at high values may also induce rupture at weld joints if not properly dimensioned. Results of the study revealed weak points in the design. Calculations were performed assuming a uniform load of 400 lb (200 kg). Deformations were found to be minimum. However stresses at the pedestal base were unacceptable and very near to aluminum yield values.

The results of the analysis were then used to modify the design of the crate and pedestal. Stresses in the pedestal were solved by eliminating as much as possible weld joints at the mounting points near to the feed through. The new design is shown in Figure ***. ***remove history and update

7.2 FEC Baseplane

***something about springs, ground posts, etc.

The FEC baseplane is mounted at the back of the crate, much like a traditional crate backplane. It is a printed circuit board containing three rows of connectors (96-pin DIN) which mate with the connectors on the various FE boards. As shown in Fig. 28, there are four different configurations of FECs, which employ five different types of baseplanes. The main functions of the baseplane are to provide mechanical support and guidance via alignment pins for the boards in the FEC, to provide an electrical interface between the warm cables in the pedestal and the FEBs, to shield the warm cables from noise radiated from the FEBs, and to transport the trigger sum components from the FEBs to the TBB or TDB mounted in the same HFEC.

Slot	EM Barrel	EC Standard	EC Special	FCAL
1	FEB PS		FEB PS	CALIB
2	FEB FR 0	FEB PS	FEB FR 0	CAL SHAP
3	FEB FR 1	FEB FR 0	FEB MID 0	FEB F1 0
4	FEB FR 2	FEB FR 1	FEB MID 1	FEB F1 1
5	FEB FR 3	FEB FR 2	FEB FR 1	FEB F1 2
6	FEB FR 4	FEB FR 3	FEB FR 2	FEB F1 3
7	FEB FR 5	FEB FR 4	FEB FR 3	TDB 0
8	FEB FR 6	FEB FR 5	FEB FR 4	FEB F1 4
9	TBB	TBB	TBB 0	FEB F1 5
10	CONT **A**	CONT **B**	CONT 1 **C**	FEB F1 6 **E**
11	FEB BK 0	FEB BK 0	FEB BK 0	FEB F1 7
12	FEB BK 1	FEB BK 1	FEB MID 2	CONT
13	FEB MID 0	FEB MID 0	FEB MID 3	FEB F2 0
14	FEB MID 1	FEB MID 1	FEB FR 5	FEB F2 1
15	FEB MID 2	FEB MID 2	FEB BK 1	FEB F2 2
16	FEB MID 3	FEB MID 3	TBB 1	FEB F2 3
17	MON	MON	FEB MID 4	TDB 1
18	CALIB	MON	FEB MID 5	FEB F3 1
19		CALIB	FEB L1	FEB F3 2
20	FEB PS		TBB 2	MON
21	FEB FR 0	FEB PS	FEB L2	
22	FEB FR 1	FEB FR 0	CALIB 0	
23	FEB FR 2	FEB FR 1	CALIB 1	
24	FEB FR 3	FEB FR 2	CONT 2	
25	FEB FR 4	FEB FR 3	FEB 1	
26	FEB FR 5	FEB FR 4	FEB 2	
27	FEB FR 6	FEB FR 5	TDB 1	
28	TBB	TBB	FEB 3	
29	CONT **A**	CONT **B**	FEB 4 **D**	
30	FEB BK 0	FEB BK 0	FEB 5	
31	FEB BK 1	FEB BK 1	TDB 2	
32	FEB MID 0	FEB MID 0	FEB 6	
33	FEB MID 1	FEB MID 1	MON	
34	FEB MID 2	FEB MID 2	CONT 3	
35	FEB MID 3	FEB MID 3	CALIB	
36	MON	MON	LV	
37	CALIB	MON	LV	
38		CALIB	LV	

Figure 28. Configurations of the different FEC baseplanes. The columns are labelled by FEC type, and the slot number is shown in the first column. Entries in the table show the type of module, for which the following abbreviations are used: PS=Presampler, FR=Front Section, MID = Middle Section, BK = Back Section, L1 = First section of EMEC Inner Wheel, L2 = Second Section of EMEC Inner Wheel, F1, F2, F3 = FCAL1, FCAL2, FCAL3, MON = Monitor Board, CAL SHAP= Calibration Shaper (used for FCAL calibration). All FEC except those for the FCAL contain two baseplanes.

The mapping of the trigger signals out of the FEBs is determined by the cabling from the calorimeter electrodes to the FEBs. The order of the trigger sum signals out of the TBB and TDB is determined by the layout of the baseplanes. The mapping is documented in detail in References [22] and [23] for the EMB/EMEC and for the HEC/FCAL, respectively. The routing of the trigger signals in the baseplane requires care to minimize signal distortions and crosstalk, and to

avoid the introduction of oscillations. The impedance of all signal lines is specified at $50\pm2\ \Omega$. Routes were chosen to avoid capacitative coupling between the trace and the input of any preamp whose output contributes to the sum being routed. The pinout patterns on the connectors on the FEBs, TBBs, and TDBs were chosen mainly to minimize crosstalk, and are shown in Figure 29.

The FCAL baseplane has an additional feature not found in the other baseplanes. Since the calibration signal for the FCAL is not sent to the electrodes, as is done for all other calorimeters, it is necessary to distribute the calibration pulse at the entrance of the signal to the preamps. This is done by a separate PCB which is mounted underneath the baseplane, just behind the middle row of DIN connectors. The calibration signals for FCAL therefore have a somewhat different nature than those for the other calorimeters and need to receive special treatment in the analysis.

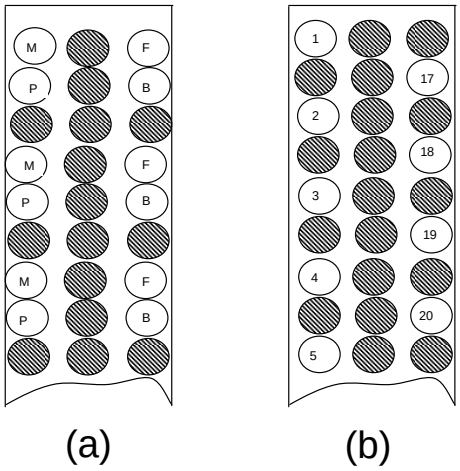

Figure 29. Signal patterns used in the trigger sum connectors (96-pin DIN) in the baseplane. The shaded pins are connected to ground. Figure (a) shows the pattern used at the TBB input, with the pins labelled P, F, M and B corresponding to the four depth layers (Presampler, Front, Middle, Back) for a trigger tower. A row of grounded pins grounds is placed between each group to reduce crosstalk between trigger towers. Figure (b) shows the pattern used on the TDB input as well as the FEB output. To reduce crosstalk between signals, each pin carrying a signal is surrounded by grounded pins.

As part of the verification process for the prototype baseplanes, electrical tests were carried out at Brookhaven National Lab and the University of Pittsburgh. Continuity checks were made for each of the traces in the baseplane. The impedance of the signal lines was measured using a Time Domain Reflectometer for a few cases and verified to be within the specifications. To check for possible shorts or other anomalies, the capacitance of each trace was measured and plotted against its length. No anomalies were found in any of the baseplanes.

Crosstalk is an important parameter for the trigger system. One of the trigger conditions is an isolated high energy EM shower. Isolation is determined at L1 by examining pulseheights in trigger towers which are neighbors to the trigger tower of interest, and crosstalk to such a tower would reduce the sensitivity to detect such showers. Since the maximum pulseheight considered at L1 is 250 GeV and isolation thresholds are set at a small multiple of the noise, typically 0.5 GeV, crosstalk values of more than ≈ 2 GeV induced by a 250 GeV signal would be problematic. For this reason the maximum permissible crosstalk for the entire analog chain for the Level 1 trigger

has been set at 1%. A study of the crosstalk was carried out for the EMB baseplane. In this study, the trace representing the middle layer of a given trigger tower was excited with a 3 V pulse of rise time 38 ns, similar in shape to calorimeter signals. An analog sum of the four layers for all other trigger towers was then displayed on an oscilloscope, and the peak-to-peak amplitude determined. The typical waveform resembled a derivitive of the exciting pulse, as expected for capacitative coupling between the traces. The maximum crosstalk value was determined for each trigger tower as the ratio of the maximum value of the signal in the channel in question divided by the amplitude of the source signal. In no case did this ratio exceed 0.2%. Due to the nature of derivative coupling, the first-order effect of the crosstalk is to shift the timing of the pulse rather than its amplitude, so the effect of baseplane crosstalk in the amplitude is completely negligible.

7.3 Power Bus Implementation

The FE LV power distribution scheme is different from schemes typically used in electronics crates. Since sensitive low-level analog signals are entering along the FEC baseplane at the bottom of the FEC, the power distribution to the FE boards is mounted along the sides of the crate. A power bus is installed with Hypertronics contact inserts. These inserts provide pass-through connections. After a board is inserted into the FEC, a “comb” holding a set of pins is inserted through the power bus. Each pin mates with a connector on the board. A detail of the connection scheme is shown in Figure **??**. The contacts are rated to 10 A, and have a nominal resistance of 2.5 mΩ. At the maximum current foreseen, a temperature increase of 10 deg C above ambient temperature is expected.

Hypertronics KS10-0002 Signal Description 1 GND 2 +6V Digital 3 +11V 4 +7V 5 +6V Analog 6 GND 7 +4V 8 -4.25V 9 -7V 10 GND

7.4 SPAC Bus Implementation

The SPAC bus consists of a PCB attached on one side of the FEC. The connection between the PCB and the electronics boards is achieved by inserting a traversing pin comb through the SPAC bus PCB and a connector on the receiving board. This design enables removal of a single electronic board from the FEC without needing to disconnect all the connections.

The connector on the PCB is a right angle female connector from Samtec [**?**] (SSW series, reference is SSW-107-02-G-D-RA). The connector on the SPAC bus is a female “pass-thru” connector (Samtec HLE series, reference HLE-107-02-G-DV-PE). The traversing pins comb that mates with both the female connector on the FEB (SSW) and on the connector on the SPAC bus (HLE) belongs to the Samtec ZW series (reference ZW-07-20-G-D-310-820).

Two or three SPAC bus PCB are needed to equip a full FEC. Most of the FE crates are equipped with two 19-position buses, one bus covering the slots 1 to 19, the second the slots 20 to 38. However, the special EMEC/HEC FEC contains three 12-position buses, the middle bus differing from the left and right ones. The two identical left and right buses cover the slots 1 to 12 and 25 to 36. The middle bus covers the slots 13 to 24, and differs from the left and right buses by the gap between slots 19 and 20, which is larger than the standard pitch of the other slots. To equip all of the FE crates, 98 SPAC19 standard buses, 16 SPAC12 buses and 8 SPAC12 middle buses are required.

The buses are 1.6 mm, four-layer stripline PCBs. The four differential SPAC signals are routed on the two inner layers (100Ω characteristic impedance), and enclosed between two ground planes. The lines are 100Ω terminated on both sides of the bus. The buses printed circuits are not directly screwed on the FEC frame, but through copper spacers which are soldered on the PCB. The aim of the copper spaces is to guarantee a gap between the bus and the FEC frame, and to make a good ground connection between the bus and the FEC. More details on the connections between the SPAC ASICs and the bus are given in [10]. Simulations on the bus performance have been done. The results can be found in [**?**].

Prototypes of the SPAC19 bus was also installed on a FEC in Brookhaven and could therefore be validated. Concerning the SPAC12 buses, given the small amount of samples to be produced, the full production was done directly. The mechanics of the SPAC12 buses was validated on a FEC in Brookhaven, and their functionality could also be tested at the Electronics Maintenance Facility (EMF) at CERN, within the Back End Crate test setup.

The reliability of the bus was validated, at the design step, with simulations of the SPAC bus and was also verified by measurements on the SPAC19 bus prototype. The bus was integrated into a system containing a SPAC slave ASIC configured in repeater mode (dedicated configuration for the Controller) and several SPAC ASICs configured as standard slaves. Some passive loads were also added to the bus to simulate a partially or fully loaded FE crate.

Figures 30 to 32 are a few plots of the measurements performed on the bus. The measurements have confirmed a good communication with all the boards on a partially or fully loaded bus; the ability to still communicate both on the download and the readback lines with one board, even when all the other boards are in power failure conditions. Some worst conditions were also tested: (example in Figure 32) when one of the signal pair wire is shorted to ground on one slave output on the readback bus, the signal pairs is unbalanced, but communication can still be done with 75% success.

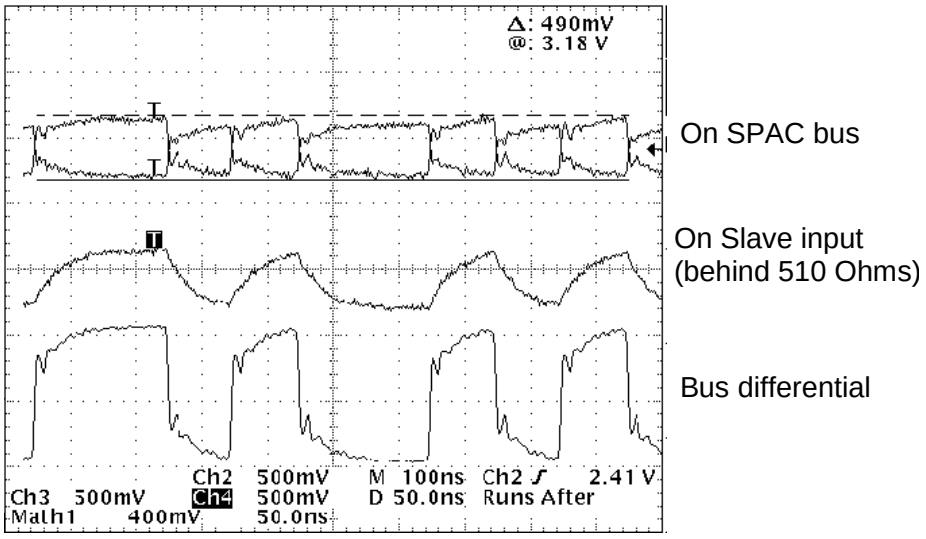

Figure 30. Download line MS1, fully loaded 19-slot bus. The ripples present on the bus are smoothed at the slave inputs by the isolation resistors.

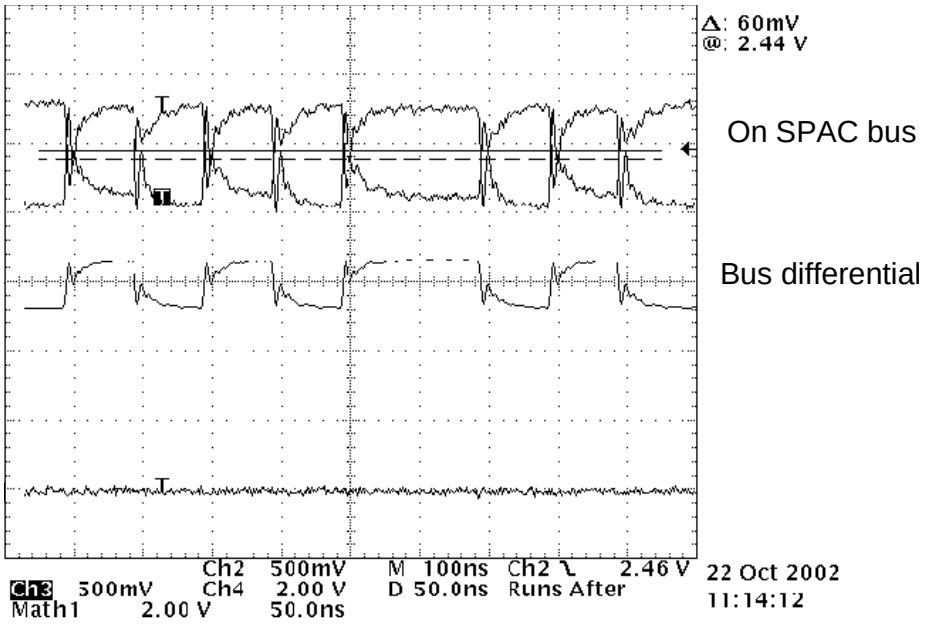

Figure 31. Readback line SM1, fully loaded 19-slot bus. The ripples present on the bus are smoothed at the receiving slave inputs. ***combine with previous fig into a,b?

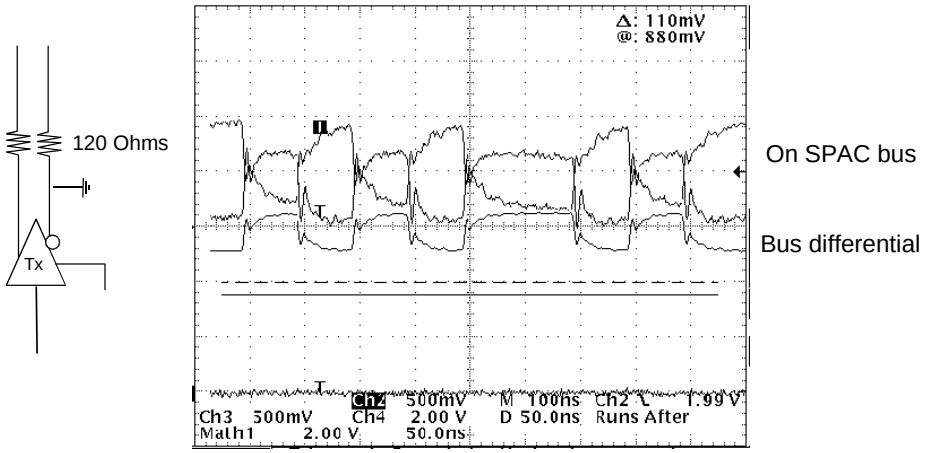

Figure 32. Readback line SM1, fully loaded 19-slot bus, one line is forced to ground. 25% of the frames are read back with errors.

7.5 FE Electronics Cooling

Cooling is required to remove the ≈ *** W dissipated in one LVPS and the ≈ *** W dissipated among the electronics boards in one FEC. Given the space constraints plus the requirement to not disturb other nearby detector systems, air cooing is not practical. In addition, the magnetic field in the region of the FE electronics would present problems to the use of fans in this area.

Instead, a water cooling system is employed. This solution poses some particular issues to be addressed. To avoid water leaks, the cooling water is circulated at an under-pressure, ≈ 600 mbar

below atmospheric pressure. Small leaks will, therefore, lead to air migrating into the cooling system, rather than to water leaks. Since the cooling is conductive, water-cooled heat exchangers need to be placed in contact with active components to remove the dissipated heat. Given the space constraints, plus the desire to minimize the presence of high atomic number material, most of the cooling infrastructure is manufactured from aluminum, which requires special care when bonding, welding, etc.

The coolant circulator will be dimensioned to provide water at around 18 deg C below atmospheric pressure. As illustrated in Figure 33, the circulator is a semi-leakless unit. The circulator consists of a water reservoir where the top part is kept below the atmospheric pressure. The pump is locate at the bottom of the reservoir and compresses the water on the way up. With enough negative pressure in the reservoir the pressure at the input of the cooling plates is already negative.

To operate such a unit it is necessary a PLC (Programmable logic controller). Constant monitoring of the vacuum and water ow is required.

Figure 33. Schematic diagram showing the under-pressure water cooling system. ***helio's fig 13

In the case of the present electronics one of the largest problems is the space constraint. In theory a thicker plate in contact with the component would be desirable since it would spread the heat more uniformly. However with 2 mm of space available this requirement is hard to be satisfied. The water flow channel alone would take this space. Therefore the option that was chosen is to manufacture very thin plates and have many flow channels. This increases the contact points between water and components. However the plate itself is not a good heat spreader.

To eliminate gaps between components and cooling plate silicone impregnated with aluminum oxide is used. This material has a heat conductivity of ≈ 1 W/(m $\times$ K), which is roughly 300 times lower than aluminum. Therefore places with large gaps between components and cooling plates are filled with metallic (aluminum) heat spreaders of proper thickness. Note however that the metallic spreaders themselves are not appropriate to guarantee good thermal contact between cooling plate and components. Mechanical tolerances and surface quality still requires the use of foam, but in reduced thicknesses.

Thin heat exchangers are fabricated as two bonded plates. In one of the plates a flow pattern is embossed by hydro forming channels against another aluminum mold. This process is slower than traditional stamping. However it is more appropriate to form soft metals. The next step in the manufacture is to provide surface treatment for the aluminum. Aluminum is known for its corrosion problems. Pure aluminum will oxidize in contact with air in matter of minutes. There are several types of treatment that can be used to prevent corrosion. Widely used by the aircraft and electronics industry is the chemical surface conversion. This is covered in length by MIL-C-5541E. The advantages of this process are: readily available and cost. Tests in the lab with chemically active water (with chlorine) showed that this type of treatment is not adequate for our applications. Microscopic analysis of the aluminum material showed that during hydro forming, microfissures are introduced in the bends and those cannot be protected by chemical treatment. The surface also becomes too smooth for bonding purposes.

A second method to protect aluminum from corrosion is anodizing. In anodizing process a layer of aluminum oxide is formed on the surface. The **lm formed by anodizing penetrates in fissures and thus preventing corrosion at these points. The surface is also appropriate for bonding. Therefore we used this process for the surface treatment. Plates, one flat and one with flow channels, are bonded next with glue from DuPont. This bonding agent has a kapton carrier that helps to keep the adhesive in place. Tests with the channels during the curing processes. When bonded the important parameter to watch is the peel strength. The chosen adhesive has a peel strength of 8 lb/in2 which is adequate for our purposes. Tests made with water running at 60 lb/in2 for 8 hours showed that bonding can withstand the pressure. Samples cut from the bonding were examined using metallurgical techniques. Analysis show a good adhesive surface. A second exploratory technique was used to examine the bond - X-Ray micro-tomography. This also shows good surface adhesion. Figure 34 shows a photograph of a final cooling plate. The channels for the water flow are clearly visible.

Figure 34. Photograph of one cooling plate.***helio's fig 12

Cooling plates are attached to the water manifolds by Manifold Blocks. These blocks provide a side entrance and exit of water. Early tests with water injected and extracted from top using tubing show a large impedance due to the thickness of the plate. At this point the plate is sealed by two O-rings. Plates are attached to the electronics board on aluminum stand-offs Amatom 19053-A-2545 Female Standoff and Amatom 19931-A-2545 Male/Female Standoff. The stand-offs are made of aluminum and establishes a distance of 6 mm from the board surface to the cooling plate. The space between the cooling plate and components are taken by space occupiers. Screws for the attachment of plates are low head profile screws.

7.6 FEC Monitoring

The Crate Monitoring Board (CMB) plugs into the FEC to provide monitoring information of the crate power levels to the ATLAS Detector Control System (DCS) [**?**]. There is one CMB installed in each of the 58 FECs. The CMB is not a full-sizeed FE board, since it does not need to connect to the baseplane. The CMB measures 489 mm $\times$ 203.2 mm. Below is the list of functionalities of CMB.

- Crate Voltage Monitoring. The CMB monitors the seven voltage lines in the FEC. The CMB gets these voltage signals from the FEC power bus through the 10-pin power connector (Hypertronics KS10-0002). The analog voltage signals are attenuated (202:1) on the CMB and transmitted to the Embedded Local Monitoring Board (ELMB) [29] which is installed locally for each FEC. The ELMB digitizes the analog signals and the digital results are retrieved by the DCS server through CANbus.

  ***move connector ref no's up to previous section

- ELMB Analog Power Supply. Digital power of the ELMB is supplied from CANbus power supply installed in USA15. However, to avoid potential ground loops, the CMB uses +11V voltage line from the crate power bus to supply analog power to ELMB.

- Noise and Ripple Filtering. CMB provides additional filtering to voltage lines on the crate, there are 500uF ceramic capacitors mounted on each of seven voltage lines, this provides additional noise and ripple filtering to LVPS output locally in the crate.

- Radiation Monitoring. CMB is chosen as mounting board of LAr radiation monitoring sensor board. To monitor the radiation level inside the FEC, LAr radiation monitoring sensor board is mounted on empty space of CMB, the cable is going through front panel of CMB and connect to radiation monitoring readout.

There are two 10-pin connectors on CMB, one is Hypertronics KS10-0002 which is a custom connector manufactured for all of the front end electronics board, CMB is connected to power bus of FEC using power comb connector (Hypertronics KS10-0001) which penetrates through power bus and plugged into KS10-0002. The other is Molex 70555-0044, this connector send attenuated voltage signals and +11V analog power to ELMB through a custom made cable. ***not needed?

8. Low Voltage Power Supplies and Distribution

The FE electronics are powered by AC-DC primary power supplies (PS) located in the underground USA15 counting room. These primary supplies are fed from the 400 V three-phase AC network in the ATLAS pit. Each primary PS delivers an output current of 10-11 A at 280 V DC and powers a single FE LVPS placed on the detector adjacent to the corresponding FEC. The one-to-one connections are made via long 70-100 m cables.

8.1 280 V Power Supplies

The 280 V supplies were supplied by industry [24]. Their main specifications are listed in Table 6.

The power supplies are controlled and monitored by the ATLAS Detector Control System (DCS) [27, 28]. The DCS is run by the Supervisory Control And Data Acquisition system PVSS, a commercial software product [25] which executes many of its control and data acquisition functions, including the temperatures and voltages of the FE LVPS, via the CAN fieldbus protocol. A fast hardware interlock powers the units off in case of an alarm (e.g. cooling water failure), independently of software processes.

The power supplies are housed in closed racks in USA15, 8 units to a rack (see Figure 35). Each rack has a closed-loop ventilation system with a turbine on top of the rack. Air is forced through ducts along the sides of the racks and then deflected up through the power supplies. Fan trays below each power supply enhance the air flow. The heat is removed by air/water heat exchangers using medium temperature (“mixed water”) cooling water provided for the experiment.

The racks are part of the ATLAS “infrastructure” and are remotely controlled (on/off power) and monitored (temperature, smoke) by the DCS system. The racks are equipped with a fire extinction system using CO_2 release in the closed rack volume.

Parameter	Value	Unit	Condition
Input Voltage	400 $\pm$40	V rms	
Phases	3 + N	-	Balanced
Frequency	47-63	Hz	
Inrush Current	$\leq$ 35	A peak	
Input Power	$\leq$5.5	kW	Operating at full load
Powerfactor	$\leq$ 0.95	-	
Output Voltage	280 (+20 / -0)	V	output terminals
Voltage Adjustment	-	-	Not required
Output Current	$\leq$16	A	
Load Regulation	$\leq$ 100	mV	Load varied from 0 $\rightarrow$ 100%
Line Regulation	$\leq$ 100	mV	Line input varied by $\pm$15%
Efficiency	$\geq$ 85	%	Load range 10 $\rightarrow$ 100%
Ripple and noise	$\leq$ 500	mV p.p	f $\leq$ 10MHz
Stability	-	-	Not a key requirement
Voltage rise time	$\geq$150, $\leq$300	V/s	At start up or Interlock enable

Table 6. Specifications for the 280 V AC-DC power supplies.

8.2 Low Voltage Power Supplies

8.3 HEC Low Voltage System

The HEC LV System has to provide the low voltage power for the Preamplifier and Summing Boards (PSBs) mounted on the HEC detector in the cold (details of HEC cryogenic electronics are presented in Reference [**?**]). In each HEC endcap there are 160 PSBs.

The HEC LV system begins with the ATLAS three-phase 400 VAC network, which is converted to 300 VDC by a 4.8 kW power supply located in USA15. The 300 VDC output is distributed to eight LV boxes on the cryostat, each of which provides power to 40 PSBs. The LV box uses DC-to-DC converters to produce three intermediate voltages (9 V, 5 V and -3 V). Two DC-to-DC Converters are used for each output voltage, with their outputs coupled via diodes.

The LV box outputs are routed to LV Distribution Boards mounted in the HEC FECs. On the Distribution Board the three intermediate voltages are regulated via Low Dropout Voltage Regulators to provide the final three supply voltages (7.2 V, 3.2 V and -1.6 V) for the PSBs. The voltages and currents are measured, and can be individually switched on or off.

The HEC LV system is controlled by PVSS via the CAN fieldbus. Each 300 VDC PS is controlled and monitored. Each LV box contains a monitor board with microcontroller and CAN-Interface, and measures a total of 1920 PSB voltages and currents. In addition, 28 internal voltages and currents are monitored.

9. High Voltage Power Supplies and Distribution

The HV PS system provides the drift voltage across the LAr sampling gaps between electrodes and absorbers. For illustration, the layout of a HEC HV channel is shown in Figure 36.

Figure 35. Racks housing the 280V supplies.

The LAr calorimeter cells are connected in about 4700 HV supply groups, roughly equal numbers in each of the three cryostats. Each HV group is wired from the calorimeter via a cryostat feedthrough port to a single HV channel. A total of 157 commercial 32-channel HVPS modules[26] are used, mounted eight to a subrack in 20 subracks. The total HV system occupies five racks in USA15. During integration in ATLAS, several upgrades [31] to the HVPS modules were necessary, mainly due to component failures. A summary of the HV module count with channel parameters is listed in Table 7.

In order to avoid stresses to the LAr detectors caused by loss of voltage, the HV system is powered via a UPS (Uninterruptible Power Supply) system. Each rack has closed-circuit air-cooling with water-cooled heat exchangers similar to the LVPS racks, as described Section 8. In case of loss of the primary cooling water, the cooling system switches automatically to an alternative non-recycling water circulation system.

Each HV channel is individually controlled (on/off, voltage, trip current, voltage ramp speed)

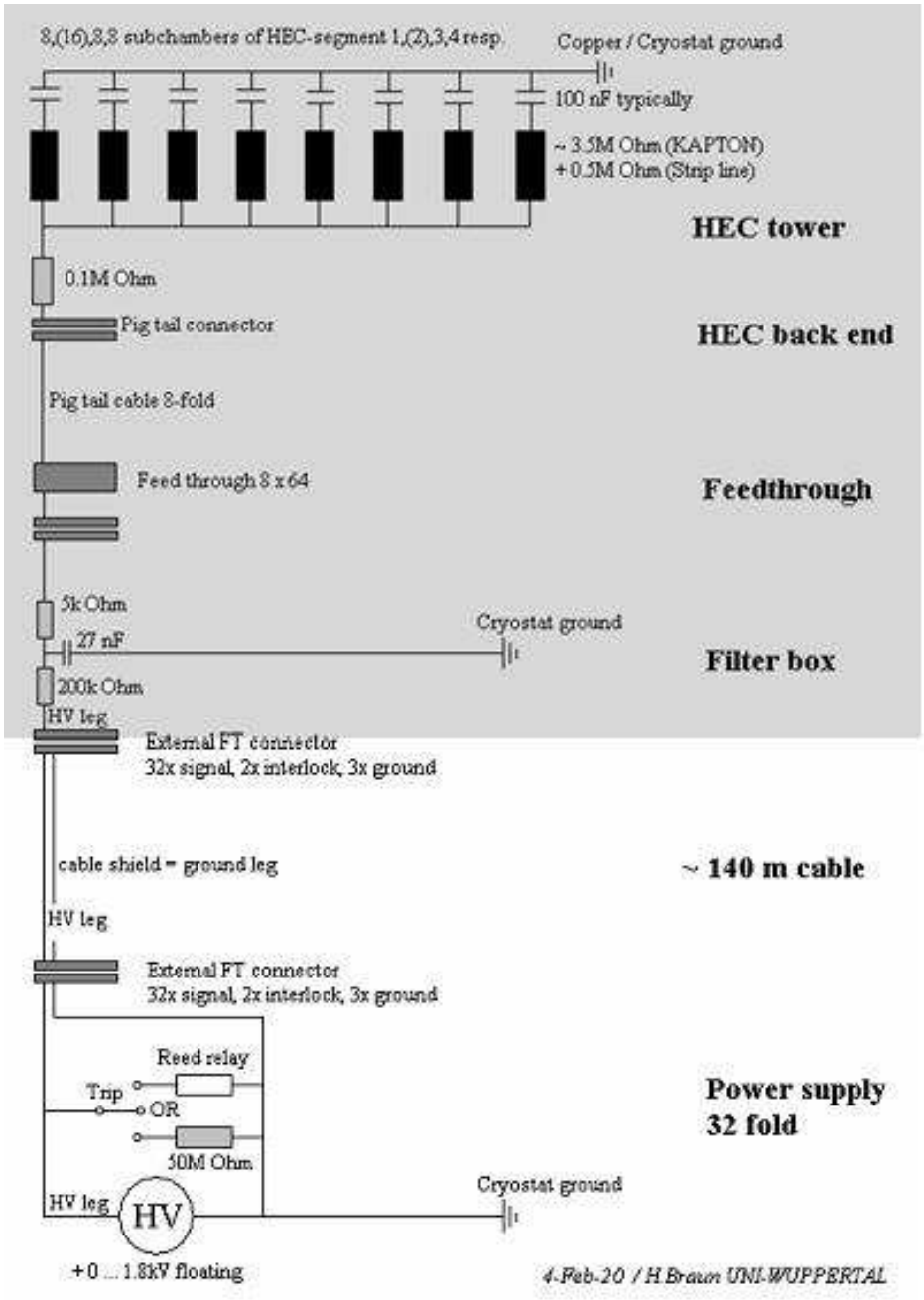

Figure 36. Schematic layout for one HV channel connected to the HEC calorimeter. ***poor quality fig

by software. For additional protection, per-module voltage and current limits for a HVPS are selectable in hardware. As an example, the specifications of a 200 μA HV module are summarized in Table 8.

The control and monitoring of the subracks and modules uses the CAN fieldbus. The computers for HV control and monitoring are located in an adjacent rack. The software sets the demanded values of the voltages and current limits and, in continuous communication with the modules, monitors and logs the actual voltage, current and channel status. A description of the control system

Number of 32-channel modules	detector	Operating Voltage (V)	Max. Current (μA)
53	EMB	2000	75
56	EMEc	1000 to 2500	200
32	HEC	1800	75
14	FCAL	250,375,500	6000
2	3×10 purity detectors	2500	75

Table 7. List of HV modules used for the various parts of the LAr calorimeter system. ***move nmodules to last column?

Parameter	EDS 20 025p-204-KB3
Channel density	32-channels in 6U Euro cassette (40,64 mm $\times$ 220 mm)
Output current I_O	max. 200 μA
per channel at V_O	+ 2550 V
Ripple and noise	f = 10-100 MHz: < 20 mV (at max. load)
Current limit I_{max}	Potentiometer (I_{max} same for 32 channels)
Voltage limit Vmax	Potentiometer (V_{max} same for 32 channels)
Interface	CAN-Interface
Data format (setting, measurement)	floating-point single precision
Voltage measurement	resolution better than 50 mV
Current measurement	resolution better than 4 nA
Accuracy of voltage measurement	$\pm(0.01\% \times V_O + 0.02\% \times V_{Onom})$ for one year
Accuracy of current measurement	$\pm(0.1\% \times I_O + 0.4\% \times I_{Onom})$ for one year
Temperature coefficient	$<5 \cdot 10^5/K$ ***not correct
Stability	$<5 \cdot 10^{-5}$ (no load/load and ΔV_{IN})
Rate of change of output voltage via softw.	Up to 500 V/s
Power requirements V_{IN}	+ 24 V (2.0 A) and + 5 V (0.4 A)

Table 8. Specifications for a 200μ A HV module.

can be found in Reference [30].

Each subrack and module is equipped with hardware interlock connections which will ramp down the HV in case of an alarm condition (e.g. cable disconnection, cryogenics failure). The modules are equipped with a crowbar relay which, if operated, discharges the detector capacitance within seconds rather than many minutes. The relay functionality can be programmed by software and is normally disabled.

A functional diagram of a HV module and its connection to the filters and cryostats is shown in Figure 37. The HV source is electrically floating relative to cavern ground and is only referenced to the cryostat's potential. For electrical safety, each subrack is equipped with a back-to-back diode pair connecting the HV reference ground and the general rack ground.

Shielded 37-conductor HV cables, rated for 3 kV and tested to 6 kV, bring HV from USA15 to the detector. The cables have a 13 mm outer diameter and are typically 120 m long. They are

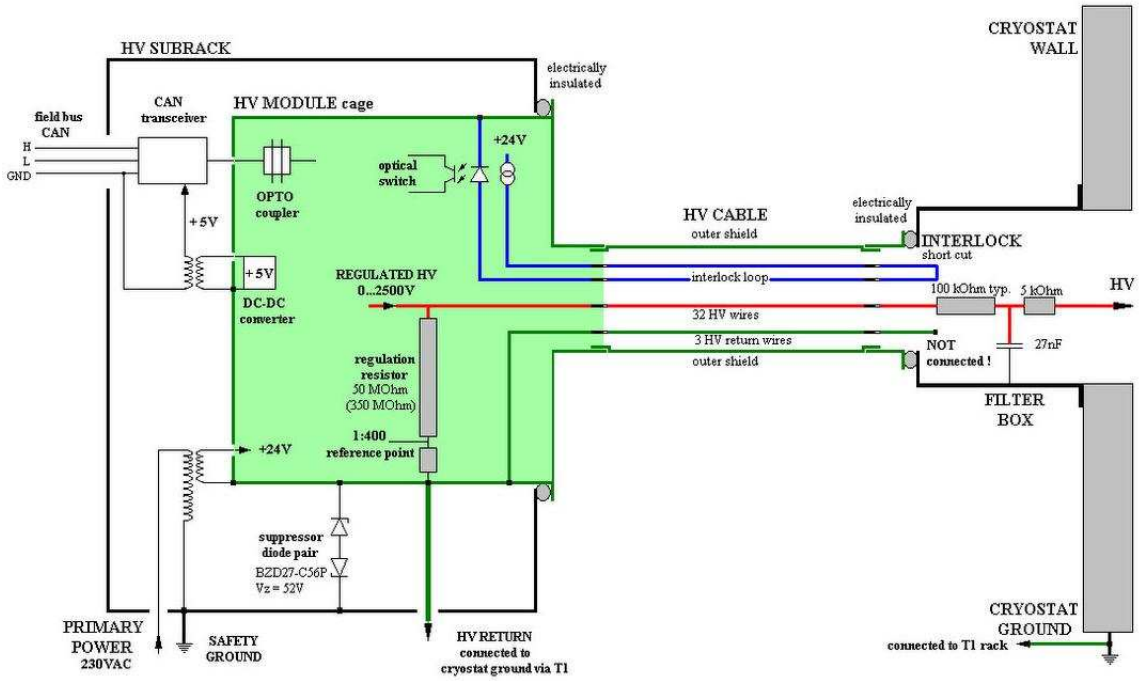

Figure 37. A HV module output and a multi-conductor cable connector (EMB).**wrong caption; poor quality fig

terminated by 51-pin multi-contact HV connectors like the one shown in Figure 38.

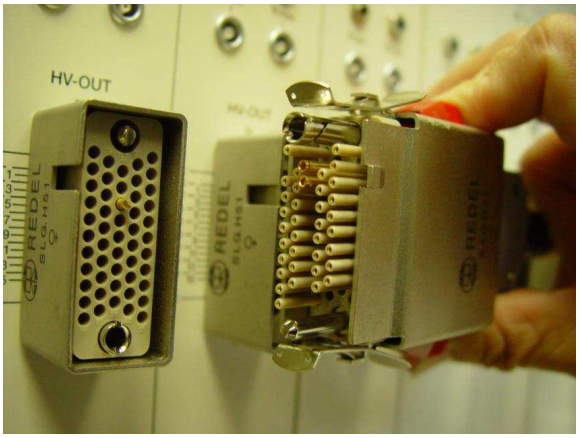

Figure 38. A HV module output and a multi-conductor cable connector (EMB) produced by LEMO/REDEL.

The HV cables ground wires and the cable shields are interrupted at the entrance of the filters in order to avoid ground loops (see next section). The HV current returns to the HV modules via the safety ground links of the corresponding cryostat.

At the detector, the HV cables are connected to HV Filter modules mounted on the HV Feedthroughs of the LAr Cryostats [32]. RC filters in these modules reduce potential electrical pick-up noise entering on the HV lines. Each 3U $\times$ 10HP filter module contains 64 RC filters,

divided over four daughter boards, with typical component values R=200 kΩ and C=27 nF (5 kV). Individual filter sections are well separated electrically to prevent leakage, corona, and discharges

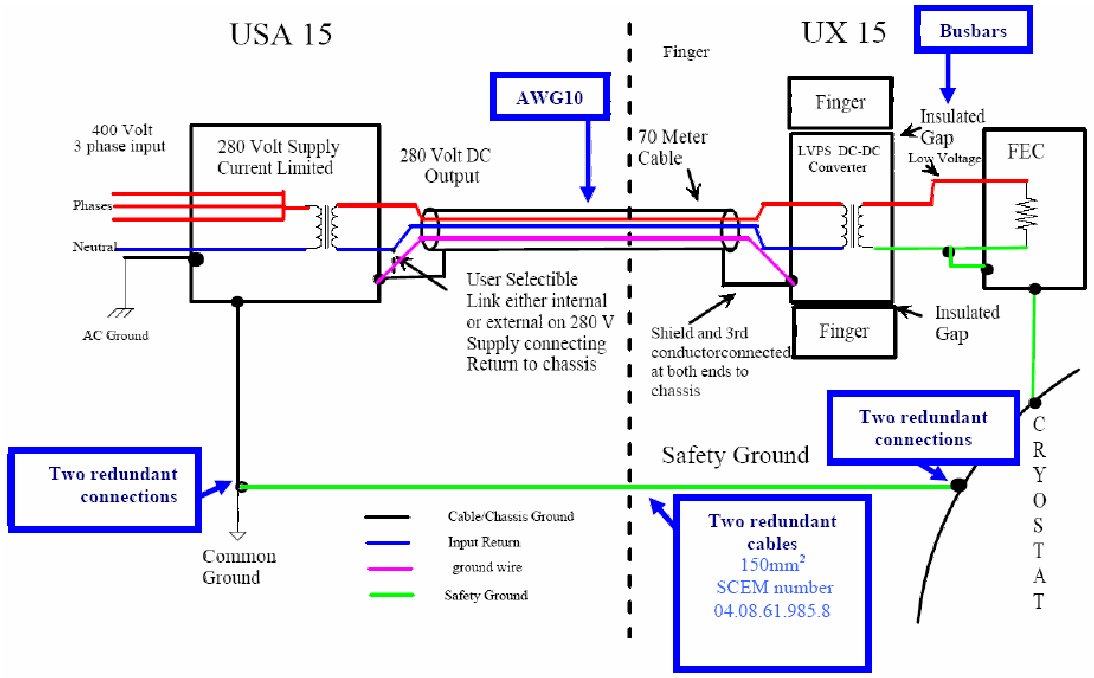

Figure 39. Grounding scheme for the Low Voltage system.

As mentioned in Section 9, the shields of the HV cables are connected on the side of the USA15 ground but left disconnected at the cryostat end***mod being made now?. On the contrary, as discussed in Section **??**, the trigger cables (the only LAr analog signals between USA15 and the detector) have their shield connected at the cryostat but not at the USA15 end, keeping the possibility of an AC connection. As shown in Figure 39, the shield of the 280V DC cable is connected to the USA15 ground. At the cryostat end it is connected only to the case of the LVPS for safety. The DC-DC converters inside the LVPS on the detector provide DC-isolation to the cryostat ground.

During installation and cabling, a ground short detection mechanism (incorporating an audible alarm) has been operating on each cryostat to prevent accidental ground connections.

In summary, all LAr services and connections to the cryostats are electrically insulated from them. The single DC current return path (in particular for the HV return current) is a single connection (composed of two cables for redundancy) linking the cryostats to a single grounding point

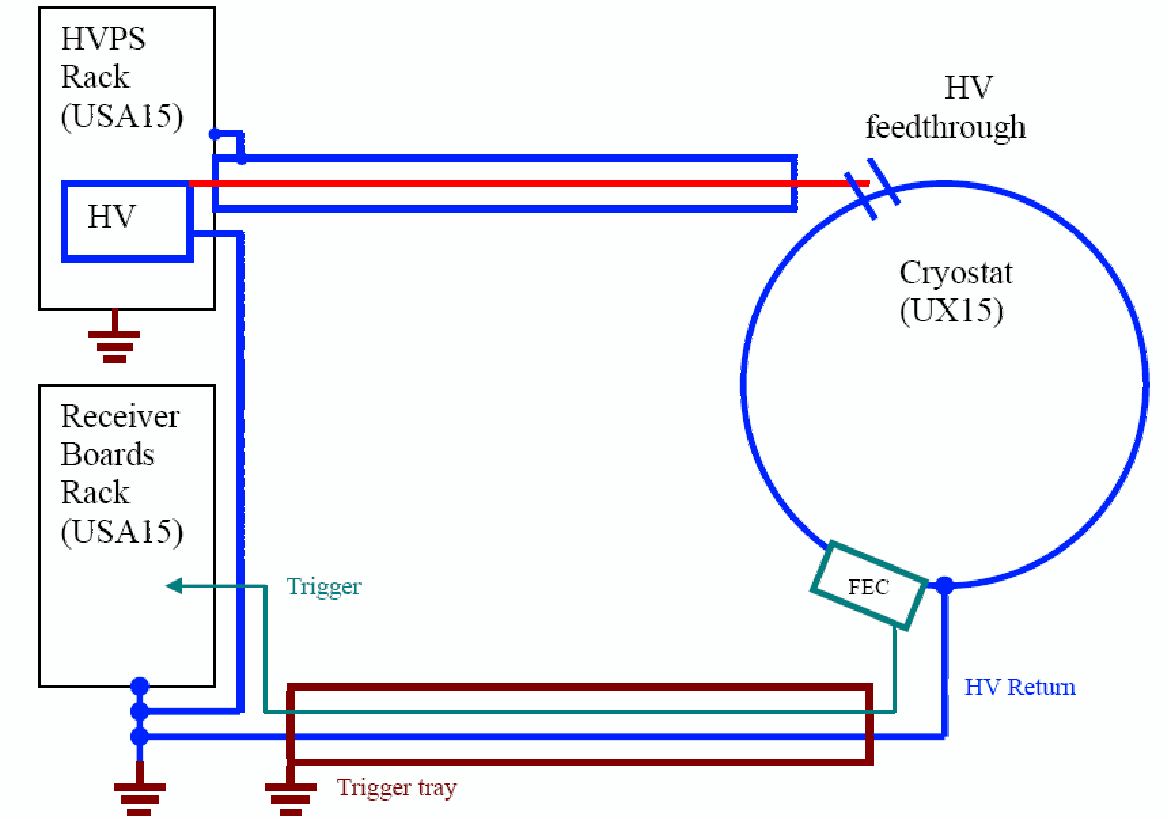

Figure 40. Grounding scheme for the High Voltage systems.

in the USA15 counting room close to the LVL1 trigger racks. This configuration avoids parasitic ground loops.

**section from Bill C.; need to integrate with other parts

It is very important to control the electrical connections between the detector and USA15, as multiple conducting paths introduce the possibility of ground loops, which cause unwanted additional sources of noise and baseline shifts. The connection of the trigger cables and their shields are therefore carried out with some attention to detail. The basic principle is to extend the Faraday cage of the calorimeter to the far end of the cable in USA15, but not to make a DC connection at USA15. Instead, we leave the possibility to connect the shield to the analog ground on the receiver through a capacitor, permitting noise which is common to both the signal and ground to be reduced if necessary. The signal itself is passed through a transformer whose center tap at the input is connected to the receiver analog ground. AC coupling is possible in this system without the undesirable effects of rate-depedendent baseline shifts as the LAr signals are bipolar with area balance. (Baseline shifts are expected for the tilecal signals, which are monopolar, but given their amplitude distribution and expected rates, their effect is expected to be negligible.) The common terminal of the receiver power supplies is connected to the crate ground, which is in turn connected to the ground line running between USA15 and the cryostats.

The output signals from the receiver are also transformer-coupled, and they are sent over twisted-pair cables which are identical to the input cables. The shields are handled in a similar way

as the shields on the input cables, only the DC connection is made at the receiving (preprocessor) end. The purpose of this arrangement is not so much to prevent ground loops but to reduce the effects of digital noise generated in the preprocessor modules on the receiver signals.

11. Cable Plant

The cabling of the ATLAS detector has been a major task with substantial manpower and many teams involved in planning and execution. For the LAr system there are many long cables connecting the FE and BE electronics. Their repetition unit of repetition is one FEC. For each FEC the connections include one 280 VDC power cable, four Cu trigger cables, one optical fiber cable bundle containing 48 individual fiber connections for digital signal data transmission, and one optical fiber bundle with six individual fibers for the TTC signals.

Additionally, other services arrive at a FEC from different points in the cavern and counting room. These include temperature probes and anti-condensation heaters on the feedthroughs, cryostat and calorimeter temperature probes located inside the LAr volume, and LAr purity probes inside the LAr volume.

Cables and services, enter the cavern from USA15 via the cable galleries and typically follow one of the following routes (marked in Figures 41 and 42:

1. Barrel outer ring route.
2. Barrel inner ring route for time-critical cables (Trigger, TTC).
3. End Cap chain at sector 9.
4. End Cap chains at sectors 11 and 15.
5. *** get rid of itemized list

From the middle ($z = 0$) of the cylindrical Tile calorimeter at the correct azimuth, the cables are routed in horizontal cable trays towards the end faces to the spaces in-between the "finger-boxes" of the Tile calorimeter. From there radially inwards they reach the FEC. This region is shown in Figure 3.

12. Summary

Acknowledgements

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References

[1] ATLAS Collaboration, "ATLAS Technical Proposal", CERN/LHCC/94-43 (1994), available at `http://atlasinfo.cern.ch/ATLAS/TP/tp.html`.

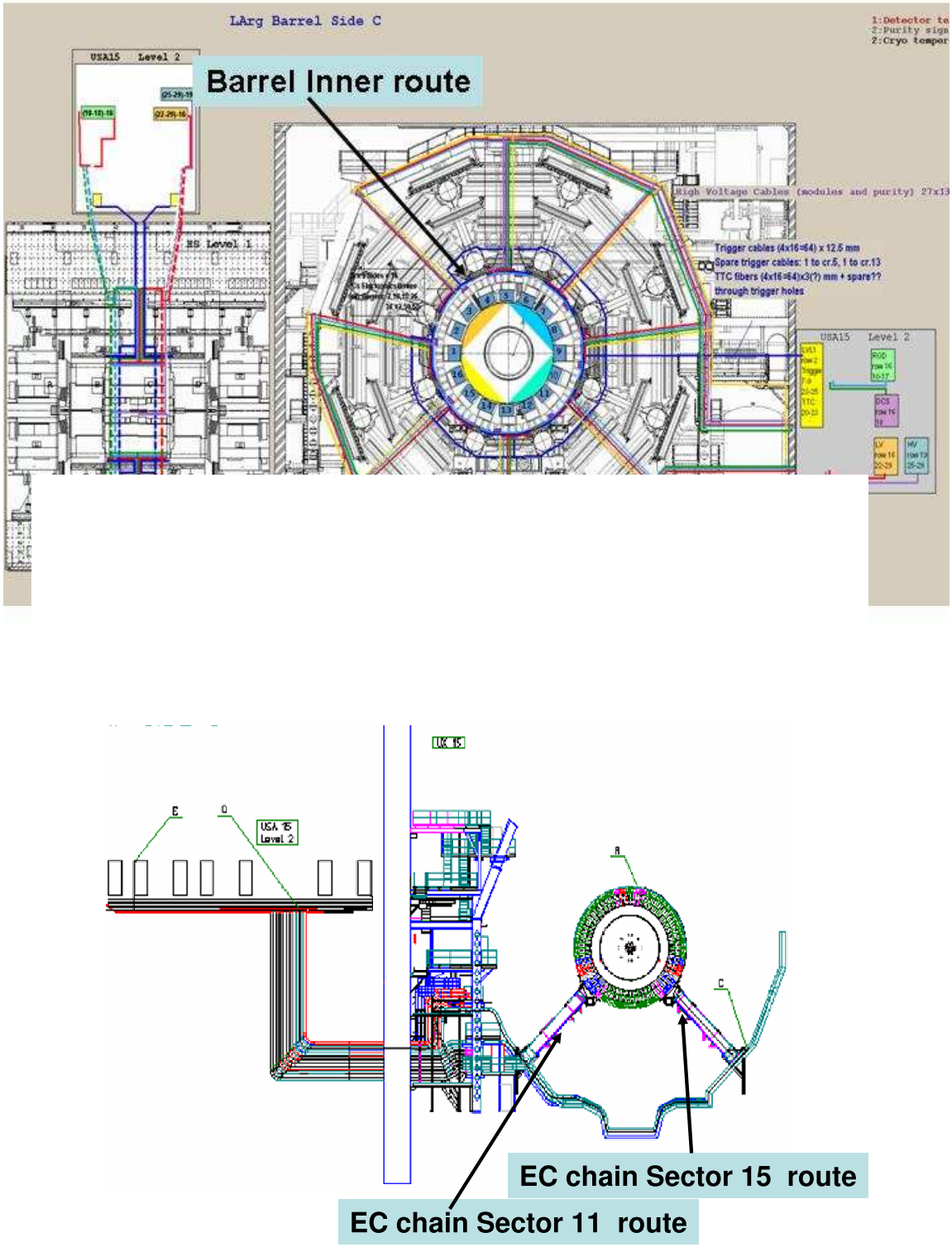

Figure 42. Cable routing to reach the LAr EndCaps. ***fig needed?

[2] ATLAS LAr Collaboration, “ATLAS Liquid Argon Calorimeter Technical Design Report”, CERN/LHCC/96-41 (1996), available at

http://atlas.web.cern.ch/Atlas/GROUPS/LIQARGEXT/TDR/;
B. Aubert et al., “Performance of the ATLAS Electromagnetic Calorimeter Endcap Module 0”, Nucl. Instr. and Meth. A **500** (2003) 178-201;
B. Aubert et al., “Performance of the ATLAS Electromagnetic Calorimeter Barrel Module 0”, Nucl. Instr. and Meth. A **500** (2003) 202-231;
J. Colas et al., “Position Resolution and Particle Identification with the ATLAS EM Calorimeter”, Nucl. Instr. and Meth. A **550** (2005) 96-115;
B. Aubert et al, “Construction, Assembly and Tests of the ATLAS Electromagnetic Barrel Calorimeter”, Nucl. Instr. and Meth. A **558** (2006) 388-418;
M. Aharrouche et al., “Energy Linearity and Resolution of the ATLAS Electromagnetic Barrel Calorimeter in an Electron Testbeam,” Nucl. Instrum. Meth. A **568** (2006) 601-623;
M. Aharrouche et al., “Response Uniformity of the ATLAS Liquid Argon Electromagnetic Calorimeter”, Nucl. Instr. and Meth. A **582** (2007) 429-455.

[3] A. Bazan, et al., “ATLAS Liquid Argon Calorimeter Back End Electronics”, JINST 2:P06002, 2007.

[4] N.J. Buchanan, et al., “Design and Implementation of the Front End Board for the Readout of the ATLAS Liquid Argon Calorimeters”, submitted for publication to JINST.

[5] J. Colas et al., “Electronics Calibration Board for the ATLAS Liquid Argon Calorimeters”, submitted for publication to Nucl. Instrum. Meth.

[6] Details of the ATLAS policy on radiation tolerant electronics can be found at http://atlas.web.cern.ch/Atlas/GROUPS/FRONTEND/radhard.htm.

[7] M. Dentan, et al., “DMILL, A Mixed Analog-Digital Radiation-Hard BiCMOS Technology for High Energy Physics Electronics”, IEEE Trans. Nucl. Sci. **43** (1996) 1763-1767.

[8] G. Anelli, et al., “Radiation Tolerant VLSI Circuits in Standard Deep Submicron CMOS Technologies for the LHC Experiments: Practical Design Aspects”, IEEE Trans. Nucl. Sci. **46** (1999) 1690-1696.

[9] Information about the LHC TTC system is available at http://ttc.web.cern.ch/TTC/intro.html.

[10] F. Hubaut, et al., “Specifications of the Serial Protocol for the ATLAS LAr Calorimeters: The SPAC3 Protocol and Slave ASIC”, available at https://edms.cern.ch/file/110351/3/.

[11] Data sheet for On Semiconductor 10H116 triple line receiver, available at http://www.onsemi.com/pub/Collateral/MC10H116-D.PDF.

[12] M. Dhellot, et al., “The SPAC Master Module of the LAr Calorimeter Readout Crates”, (2004), available at https://edms.cern.ch/document/478402/1.2.

[13] P. Borgeaud, et al., “The ATLAS Tower Builder Board: Calculation, Simulation, Measurements", (2002) available at https://edms.cern.ch/document/870843/1.

[14] X. de la Broise, A. Le Coguie, and J. Schwindling, “The Tower Builder Board: Results at the Front End Crate Test”, (2004) available at https://edms.cern.ch/document/870850/1.

[15] W. E. Cleland, et al., “Receiver/Monitor System for the ATLAS Liquid Argon Calorimeters”, (2006), available at https://edms.cern.ch/document/347184/4.

[16] W. E. Cleland, et al., “Digital Communications in the ATLAS Receiver/Monitor System”, (2003), available at https://edms.cern.ch/document/411279/1.

[17] Vladimir Savinov, “Pitt Tests of the Receiver/Monitor Stations for the ATLAS Calorimeters: Part 1”, ATL-AL-EN-0049 (2003), available at https://edms.cern.ch/document/411281/1.

[18] Application Note OA23, National Semiconductor Corp.

[19] W. E. Cleland, “Cabling of the ATLAS Liquid Argon Receiver System”, ATL-AL-EN-0042 (2003), available at https://edms.cern.ch/document/347182/2.

[20] V. Paolone, “Remapping Boards for the ATLAS Liquid Argon Receiver System”, ATL-AL-EN-0046 (2002), available at https://edms.cern.ch/document/366640/3.

[21] L1Cal Group, “Level-1 Calorimeter Trigger: Cable Mappings and Crate Layouts from Analog Inputs to Processors”, ATL-DA-ES-0036 **.

[22] W. E. Cleland, “Cabling of the Barrel and EMEC Level 1 Trigger Sums”, ATL-AL-ES-0010 (2002), available at https://edms.cern.ch/document/110534/2.

[23] W. E. Cleland, “Cabling of the HEC and FCAL Level 1 Trigger Sums”, ATL-AL-ES-0017 (2002), available at https://edms.cern.ch/document/347183/1.

[24] O.C.E.M. S.p.A., Via 2 Agosto 1980, n.11, I-40016 San Giorgio di Piano, Bologna, www.ocem.com.

[25] Prozessvisualisierungs- u. Steuerungssytem, ETM Co., Austria.

[26] Iseg Spezialelektronik GmbH, Bautzner Landstr. 23, D-01454 Radeberg / Rossendorf, www.iseg-hv.com.

[27] H. Boterenbrood, et al., “Design and Implementation of the ATLAS Detector Control System”, Proceedings of the 2003 IEEE Real Time Conference, Montreal (2003). [TO BE REPLACED BY FINAL PUBLICATION].

[28] Atlasdss

[29] elmb

[30] Milano document

[31] H. Braun, et al., “Report on Running Channels in ISEG 32-Channel HV Power Supplies”, ATLAS note *** (2006).

[32] HV FT note

[33] G. Blanchot and L. Hervas. “Liquid Argon Installation and Safety Report”, EDMS NUMBER: ATC-TE-IR-0001 (2004), available at https://edms.cern.ch/document/499605/3.