Functional and Acceptance Tests of Configuration Controller Chips

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Abstract

We discuss the functional tests and acceptance process for DMILL Configuration Controller chips, an ASIC which was designed for use on the Front End Boards of the ATLAS LAr readout.

1 Introduction

Radiation hardening the design of the ATLAS LAr Front End Boards (FEB) [1] has required the development of several custom ASICs using radiation-hard processes. The DMILL-based Configuration Controller (Config) [2] was designed to provide the interface between the "SPAC" serial control bus and the various devices which require configuration or control on the FEB. The devices to which the Config interfaces include voltage regulators, custom BiCMOS shaper chips, and several varieties of both DMILL and DSM digital ASICs. The Config is clocked on the FEB with a 5 MHz clock.

2 Functional Test Procedure

We have developed a test setup for complete functional testing of Config chips. The device-under-test (DUT) is placed in a socket on the DUT jig. The real-time control of the Config DUT is driven by an Altera FPGA mounted on an "FPGA testjig" connected to the DUT testjig via short cables ($\approx$ 20 cm, long enough to allow the FPGA to be sufficiently shielded from the beam when the same setup is used for radiation tests). All I/O pins of the Config are connected in this way to the FPGA, which can therefore monitor all Config activity in real time.

For testing, the chips are powered and clocked at their nominal frequency of 5 MHz. The power supply current and voltage are recorded.

Each of the major functional blocks of the Config (for more details of the Config design, see reference [2]) is tested. These tests can be divided into several classes:

- serial port tests - each of the 4 Config serial ports is tested with broadcast Write commands, individual Write commands, and individual Read commands,

- shaper tests - it is verified that the Config can write and read from each of the shaper switch setting addresses,
- voltage regulator tests - all 8 Inhibit lines are tested, as are the over-current sense lines,
- flag tests - it is verified that all 4 flags could be set properly.

The complete test takes ≈ 30 s, dominated by the chip handling time.

3 Config Prototype Test Results

The Config design was submitted for prototyping as part of Europractice MPW Run 511 submitted in September 2000. In February 2001, shortly before the chips were scheduled to be delivered, the foundry announced that they had detected a processing error which resulted in a substantial via misalignment in this MPW run. We decided to accept delivery of the chips anyway, hoping that the error might not be so serious as to prevent us from testing and verifying the design. This did in fact turn out to be the case. This initial set of 20 packaged chips was received in March 2001. In the meantime, the foundry processed an additional set of wafers, and delivered a new set of 20 chips, without the via problem, in May 2001.

All 40 Config samples were subject to complete functional testing using the setup described above. Of the 20 original chips, 19 passed all tests. A total of 18 of the 20 additional chips also passed all tests. The combined yield was $37/40 = 92.5\%$.

4 Config Production Test/Acceptance Procedure

Each production Config chip will be labelled with a unique serial number. Each chip will then be submitted to the complete functional test. Only chips which pass all tests and which have a reasonable power supply consumption will be accepted. The supply current will be stored in a file along with the serial number and the results of the test. The log will include information on which tests, if any, failed in order to look for patterns among rejected chips.

The chip testing will be performed manually, with the chips handled carefully using a hand-held vacuum handling tool. Even allowing one minute per chip for testing, it will take only a few days to test the total of ≈ 2000 chips required.

5 Summary

A test setup has been developed for complete functional testing of the production DMILL Config chips. The setup was used for the 40 prototype Config chips received, and determined a yield of 92.5%. The identical setup will be used for the acceptance tests of the production Config chips.

References

[1] J. Ban, S. Negroni, J. Parsons, S. Simion, and B. Sippach, "Design and Implementation of the ATLAS LAr Front End Board"; available at `http://www.nevis.columbia.edu/~atlas/electronics/ATLASFEB/FEBnote.pdf`.

[2] P. Cros, M. Bouchel, J. Parsons, B. Sippach, and S. Böttcher, "The Configuration Controller", available at `http://www.nevis.columbia.edu/~atlas/electronics/asics/conf_ctrl.pdf`.