Design and Functional Tests of the DSM Clock Fanout for the ATLAS LAr Front End Board

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Abstract

We describe the design, functional tests and yield measurements of the deep-submicron (DSM) Clock Fanout ASIC designed for use on the ATLAS LAr Front End Board.

1 Introduction

Radiation hardening the design of the ATLAS LAr Front End Boards (FEB) has required the development of a number of custom ASICs using radiation-tolerant processes. The Clock Fanout (CLKFO) ASIC was designed using the radiation-tolerant DSM library. It serves a variety of functions in the clock distribution on the FEB, thereby eliminating the need for a number of COTs components.

In this note we provide some details on the CLKFO design, and discuss the functionality testing of the chips. The results of radiation testing are described in a separate note [1].

2 CLKFO Design

A block diagram of the CLKFO is shown in Figure 1. It is designed to serve a variety of functions in the FEB clock distribution:

- for optimal noise performance, the SCA chips require a narrow differential WCLK signal, generated by the CLKFO by clipping the input 40 MHz clock,
- the fanout functionality is realized by the CLKFO providing a number of output copies of its input clock,
- to optimize the FEB noise performance, most of the clock fanout utilizes LVDS signal levels,

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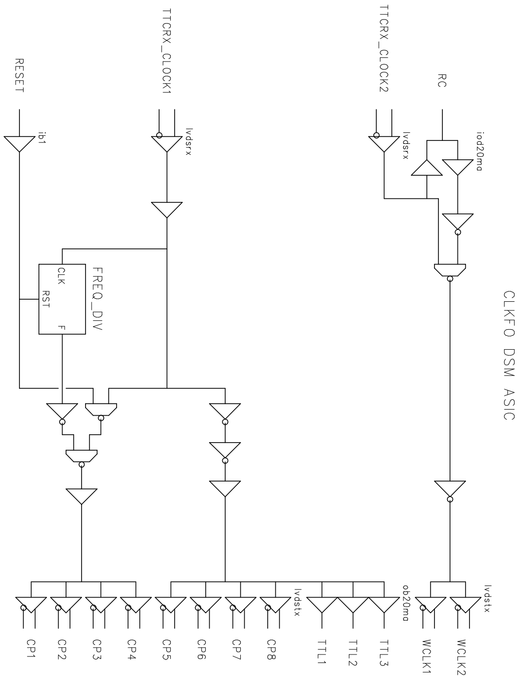

Figure 1: Block diagram of the DSM CLKFO ASIC.

- a few DMILL chips on the FEB require single-end TTL clock signals, also provided by the CLKFO,
- the Read operation of the FEB operates at 5 MHz. The CLKFO generates the RCLK by counting down the input 40 MHz clock. The down-counter is implemented using triply-redundant logic and majority voting in order to increase the SEU tolerance.

The CLKFO receives two differential clocks. One (CLOCK2) is clipped using timing from an external RC, and two copies of the differential clipped clock are output. The other input clock (CLOCK1) is fanned out to 3 single-ended TTL copies and up to 8 LVDS copies. The 8 LVDS outputs are shared between 4 copies which have the same frequency as the input (CP5 through CP8) and 4 outputs (CP1 through CP4) which, depending on the Reset pin, are either the same frequency or are counted down by a factor of 8 (see Figure 1).

The rather simple CLKFO design was expressed in Verilog and then targeted onto the rad-tol standard cell library using CADENCE tools. The resulting layout, shown in Figure 2, measures only 2 mm $\times$ 2 mm and is strongly pin-limited.

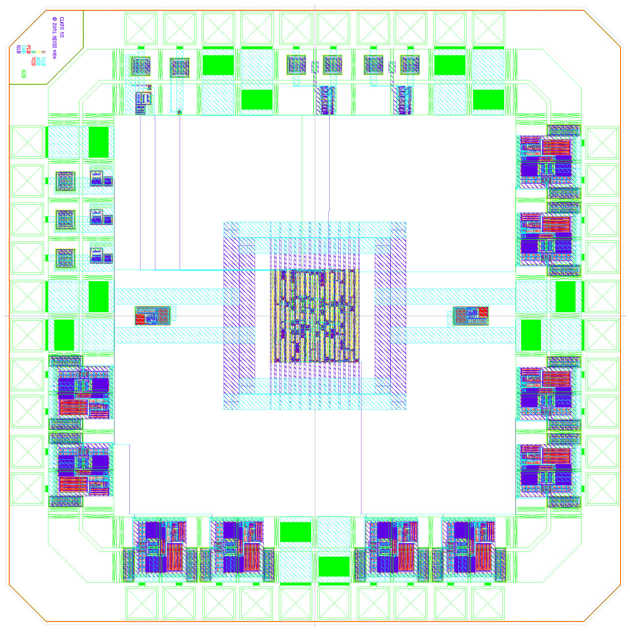

Figure 2: Layout of the DSM CLKFO ASIC.

The CLKFO is packaged in a 44-pin PLCC, with pinout as shown in Figure 3. If pin 43 (RESET_N) is pulled LOW on the PCB, the counter is enabled and generates 5 MHz clocks. If this pin is pulled HIGH, the counter is disable and all CLKFO outputs are at the same frequency as the inputs.

3 CLKFO Functional Tests

When the first CLKFO prototypes were received from MPW4, an issue of interest was the propagate delays through the chip, since we rely at the FEB level on a good understanding

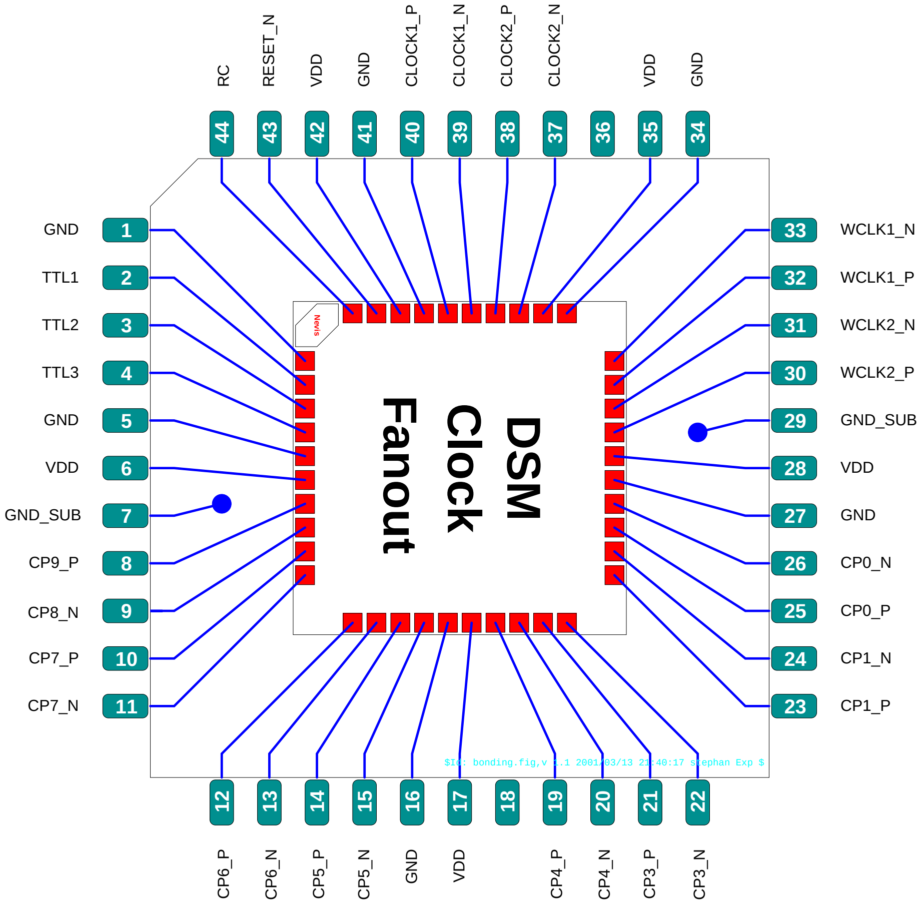

Figure 3: Pinout of the DSM CLKFO ASIC.

of the timing properties of the clock fanout. A socketed test jig was developed which was well suited to characterizing the CLKFO performance via oscilloscope measurements.

A sample of 37 CLKFO chips from MPW4 were measured using this jig. For example, Figure 4 shows the measured propagate times for the rising and falling edges, versus the supply current drawn. Due to the "striping" of the wafer, a variety of currents were observed. However, the propagate times show a nice narrow spread. Additional tests revealed that the CLKFO would function properly up to speeds of about 300 MHz, providing a very wide margin.

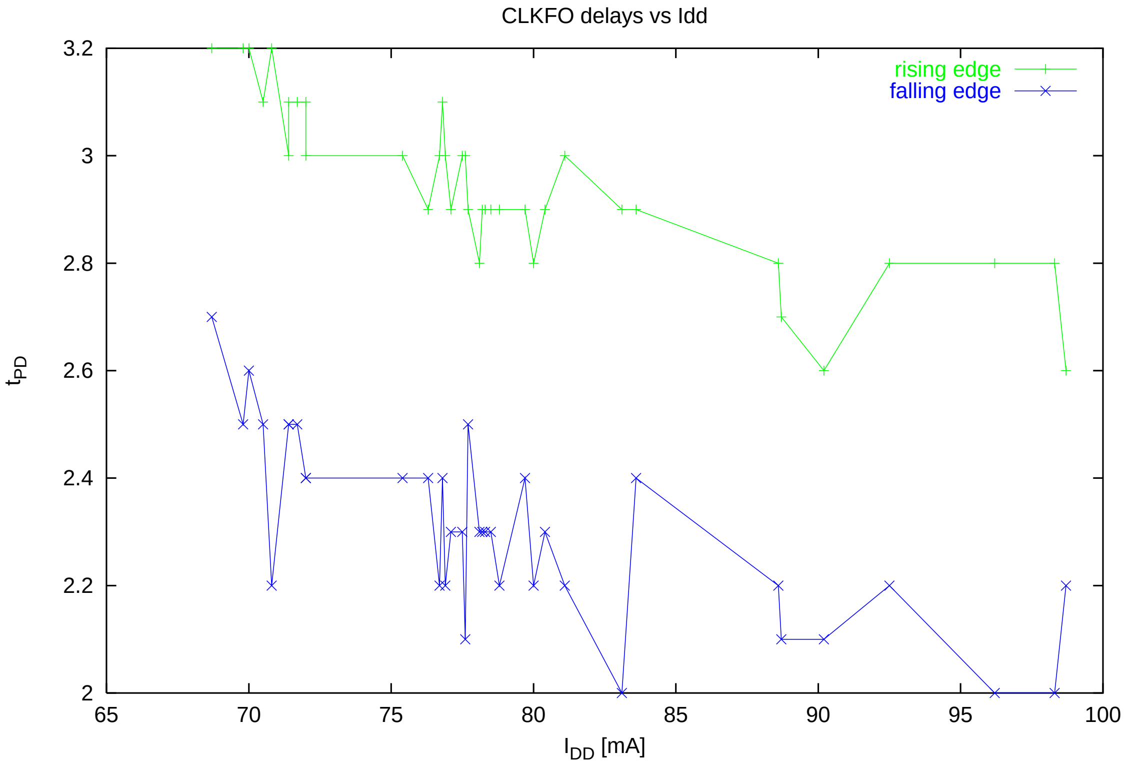

Figure 4: Measured propagate delays versus current for 37 DSM CLKFO chips from MPW4.

Given the excellent performance of the chips, and their successful tests on the FEB prototypes, we then designed a new test jig which would be suitable for production testing of the approximately 12,000 chips needed for ATLAS. The goal of this jig was to thoroughly test the "analog" functioning of the CLKFO, but in a "digital" environment. Given the sensitivity of the FEB to the quality of the clock distribution, we wanted, for example, to ensure that accepted CLKFO chips were not only fully functional, but also had acceptable timing behavior. In addition, we wanted to check that both signals of the differential outputs were separately working, and were within acceptable voltage ranges.

The test jig interfaces the CLKFO DUT to an FPGA through commercial LVDS-to-TTL receivers. Each signal of each CLKFO LVDS output is sent to its own receiver, with the other input tied to the LVDS threshold, in order to guarantee that both signals of each differential pair are working properly. The input logic stage of the FPGA usually manually placed FlipFlop chains to test the arrival time of the signal with a bin size related to the FF propagate time of about 0.7 ns.

The FPGA on the test jig provides clocks which are sent to the CLKFO DUT; to further stress the timing, all tests are performed with a clock frequency of 75 MHz. The test jig performs the following tests:

- the current drawn by the chip is measured and required to lie within an acceptance window,
- the four signals of the two clipped WCLK outputs are analyzed, requiring that all four signals are functional and that the pulse width of each lies within an acceptance window
- the 16 signals of the 8 LVDS CP outputs and the 3 TTL outputs are analyzed in a similar way
- a sequence of exactly 16k clocks are sent by the FPGA and the number of resultant clocks for each CLKFO output is counted to verify that exactly the correct number is received
- the down-counter is tested by sending exactly 16k clocks and counting that the correct number of counted down clocks is received

3.1 DSM CLKFO Yield Results

Using the production test jig, the additional 83 samples from MPW4 were tested. All chips passed the test and were accepted. (As for the GainSel, the incompletely processed chips were removed from the sample via visual inspection of the die before packaging.)

Testing of the 159 CLKFO chips from MPW6 resulted in 137 good chips, 21 chips which drew no current (consistent with the $\approx 10\%$ expected to be incompletely processed) and 1 chip with anomalously high power consumption. The resulting yield is $137/138 = 99.3\%$ if one eliminates the zero current chips, or $137/159 = 86.2\%$ if one includes all chips.

4 Summary

The DSM CLKFO chip provides the several functions needed in the clock distribution of the FEB, and eliminates the need for several COTs components. A test jig has been developed which is suitable for functional testing the production chips. Test results on the CLKFO prototypes from MPW4 and MPW6 revealed excellent yields.

References

[1] S. Böttcher et. al., "Preselection Radiation Tests of DSM ASICs for the ATLAS LAr Front End Board" (available at `www.nevis.columbia.edu/~atlas/electronics/radiation/dsm.ps`).