Functional Tests of the DSM Gain Selector for the ATLAS LAr Front End Board

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Abstract

We report the results of functional tests and yeild measurements of the deep-submicron (DSM) Gain Selector ASIC designed for use on the ATLAS LAr Front End Board.

1 Introduction

Radiation hardening the design of the ATLAS LAr Front End Boards (FEB) has required the development of a number of custom ASICs using radiation-tolerant processes. The Gain Selector(GainSel) [1] was designed first with the DMILL technology. However, the same Verilog design was then targeted to the radiation-tolerant DSM library, and the DSM version will be used in ATLAS.

The DSM GainSel was first prototyped as part of run MPW4 submitted in February 2001. The version of standard cell library used at that time was discovered to have incomplete ESD protection, leading to an update of the library. The GainSel design was therefore updated by targeting the original Verilog code on to the updated library. The updated design was submitted for prototyping in MPW6 in November 2001.

In this note, we report on functional tests of the DSM GainSel chips from both the MPW4 and the MPW6 runs. Radiation tests of the GainSel are reported in a separate note [2].

2 GainSel Functional Testing Procedure

A socketed GainSel functional test jig was designed to permit testing of the GainSel ASICs with the goal of rejecting faulty chips. The jig is interfaced to a DAQ PC in a similar way to as described in the radiation testing setup (see [2]).

Tests which are performed include:

- the power consumption of the DUT is measured and recorded,

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- the DUT is serially configured and read back using different chip IDs, in order to exercise all chip address bits,
- the DUT's response to sample commands which originate from the SCA Controller is tested,
- all of the DUT's outputs are tested, including to the MUX, to the SCA, and to the SCA controller
- proper operation of the the DUT in fixed one-gain mode and then in auto-gain mode with various thresholds is verified
- all ADC input bits are tested. As part of this test, the lower 4 ADC bits are gray-coded and incremented every 25ns so that we can verify, in a crude way, that the ADC outputs are sampled at the right time.

Note that not all of the possible modes are tested. For example, there is no explicit testing of multiple gain readout or of the "backporch feature". In addition, while the differential outputs are tested logically with a differential receiver in the controlling FPGA, the separate signals (eg. voltage levels) of the GainSel differential outputs are not tested individually. However, experience so far has shown that the tests are sufficiently exhaustive to reject faulty chips, and the yields are in fact very high.

3 GainSel Functional Test Results

During packaging of the MPW4 chips, it was realized that the die included devices from near the edge of the wafer which were incompletely processed (in particular, power Vias were missing). Discussion with CERN verified that this was to be expected for $\approx 10\%$ of the chips, which would subsequently draw no current.

Since the MPW4 chips were not yet packaged, we visually inspected the die to remove from the sample the incompletely processed chips. We then packaged and tested the remaining 140 chips. Of these, two were found to be faulty, one with an anomalously high current and the other with reasonable power consumption but logical errors. The resultant yield was then $138/140 = 98.6\%$.

For the MPW6 chips, we received the samples only after packaging in plastic packages, and therefore could not remove the incompletely processed die. Of the 162 chips, 18 were observed to draw no current; this is consistent with the $\approx 10\%$ expected to be incompletely processed. Of the remaining 144 chips, 138 were classified as good, 4 were completely non-functional and had anomalously high power consumption, and 2 had logical errors. The resultant yield is $138/144 = 95.8\%$ if one counts only the chips which draw current, or $138/162 = 85.2\%$ counting all chips.

Figure 1 shows the distribution of measured currents for the MPW4 chips (left plot) and MPW6 plots (right plot). The large spread for the MPW4 chips shows clearly the effects of the "striping" performed in that run in order to evaluate the corners of the paramter space. The MPW6 plot is much narrower, as expected since no striping was done, and also shows the chips which draw no current.

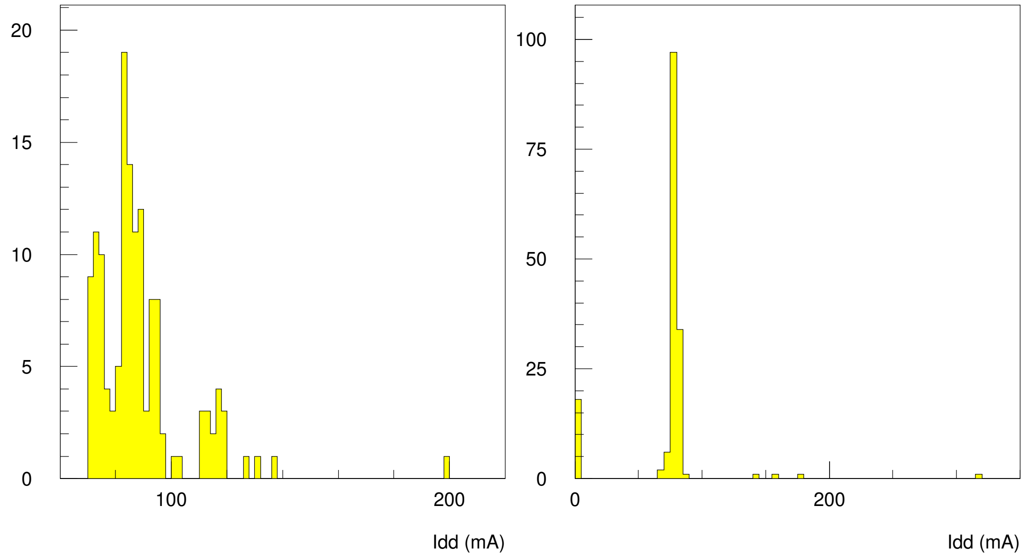

Figure 1: Current drawn by the DSM GainSel chips from the MPW4 (left plot) and MPW6 (right plot) runs.

4 Summary

A functional test procedure has been developed for the DSM GainSel chips. Excellent yields were observed for both the MPW4 and MPW6 samples.

The test jig and procedure will be used for production testing the GainSel chips.

References

[1] S. Böttcher et. al., "The Gain Selector ASIC for the ATLAS LAr Calorimeter" (available at `www.nevis.columbia.edu/~atlas/electronics/asics/ggains/gainsel.ps`).

[2] S. Böttcher et. al., "Preselection Radiation Tests of DSM ASICs for the ATLAS LAr Front End Board" (available at `www.nevis.columbia.edu/~atlas/electronics/radiation/dsm.ps`).