Preselection Radiation Tests of DSM ASICs for the ATLAS LAr Front End Board

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Abstract

We report the results of pre-selection radiation tests of the deep-submicron (DSM) ASICs designed for use on the ATLAS LAr Front End Board. Samples of the devices have been exposed to high intensity proton beams in order to simultaneously evaluate their tolerance to ionizing radiation, hadrons, and possible single event effects. The DSM ASICs were shown to be sufficiently radiation tolerant to be suitable for use in the LAr readout.

1 Introduction

Radiation hardening the design of the ATLAS LAr Front End Boards (FEB) has required the development of a number of custom ASICs using radiation-tolerant processes. In addition to several ASICs developed using the DMILL technology, three ASICs were developed using the CERN-based standard cell library targeted on a 0.25 μm CMOS DSM process.

Prototypes of all three DSM ASICs, namely the SCA Controller (SCAC) [1], the Gain Selector (GainSel) [2], and the Clock Fanout (CLKFO) [3], were first produced as part of run MPW4 submitted in February 2001. Functional tests showed all three designs were functional, though two non-critical bugs were discovered in the SCAC design (more details can be found in reference [1]). In addition, the version of standard cell library used for the first prototypes was discovered to have incomplete ESD protection, leading to an update of the library.

The designs of the three chips were therefore updated with the newer library version. The GainSel and CLKFO designs were not modified; the original Verilog code was simply targeted on to the updated library. The SCAC logic was slightly modified to fix the two bugs. All three updated designs were submitted for prototyping in MPW6 in November 2001. Subsequent functional tests revealed that all three ASIC designs were, once again, functional.

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A report on our radiation tests of the SCAC prototypes from MPW4 can be found in reference [4]. Further SCAC testing by the University of Alberta group included a demonstration that the two SCAC bugs had indeed been successfully fixed in the MPW6 design, as well as irradiation tests of the MPW6 SCAC prototypes; details of these tests can be found in reference [5].

In this note, we report the results of proton irradiation tests we performed on samples of GainSel and CLKFO samples from both MPW runs.

2 Radiation Tolerance Requirements

Simulations of the ATLAS detector have been performed to estimate the radiation levels to which the electronics will be exposed over 10 years of LHC operation. Separate levels are provided for Total Ionizing Dose (TID in kRad), neutron-induced damage (NIEL, in 1 MeV equivalent neutrons/cm^2), and for single event effects (SEE, calculated for the total fluence of hadrons of momentum greater than 20 MeV).

The FEBs will be installed in the ATLAS detector in crates mounted directly on the signal feedthroughs of the barrel and endcap cryostats. The expected radiation levels [6] to which the FEBs will be exposed in the EM barrel are summarized in Table 1. Since the expected levels in the endcaps are approximately ten times lower than in the barrel, the qualification procedure concentrates on the case of the EM barrel.

Type of Radiation	Simulated Level
TID	5 kRad
NIEL	$1.6 \times 10^{12}\ n/cm^2$
SEE	$7.7 \times 10^{11}\ h/cm^2$

Table 1: Expected radiation levels for the FEBs mounted in the EM barrel crates, integrated for 10 years of LHC operation.

The ATLAS radiation qualification criteria require irradiation of electronics to the expected levels multiplied by the product of “safety factors” (SF) which account for uncertainties in the simulation of the expected radiation levels (SF_{sim}), in possible low dose rate effects (SF_{ldr}), and in possible lot-to-lot variations (SF_{lot}). The safety factors to be used depend on the type of component and type of test being performed.

2.1 Radiation Levels and Safety Factors

The DSM ASICs are CMOS devices which are produced with a process which is not guaranteed by the vendor to be radiation-tolerant. Therefore, for radiation qualification purposes, we treat the DSM ASICs like CMOS COTS devices which, for production, we would purchase from a known homogeneous lot. Table 2 summarizes the appropriate safety factors to use for the pre-selection tests, as well as the resultant Radiation Tolerance Criteria (RTC).

Test Type	Preselection Safety Factors				RTC
	SF$_{sim}$	SF$_{ldr}$	SF$_{lot}$	Total	
TID	3.5	5	2	35	170 kRad
NIEL	5	1	2	10	$1.6 \times 10^{13}\ n/cm^2$
SEE	5	1	2	10	$7.7 \times 10^{12}\ h/cm^2$

Table 2: Summary of safety factors, and the resultant Radiation Tolerance Criteria (RTC) to be used in the preselection of the DSM ASICs.

3 Radiation Facility

The irradiation runs were performed at the *Harvard Cyclotron Laboratory (HCL)* [7] in Cambridge, Massachusetts. The HCL, which was de-commissioned on June 2, 2002, used a proton synchrocyclotron to generate proton beams, primarily for radiation therapy. The facility could be used during the weekends for other purposes, including radiation qualification of electronics.

The HCL proton beam had a maximum energy of 158 MeV on target; irradiation at lower proton energies could be achieved by insertion in the beamline of lucite absorbers of varying thicknesses. The beam energy resolution was typically 2 - 5 MeV for energies above 100 MeV, and about 10 MeV for lower energies.

The HCL high-intensity beamline delivered a maximum flux of $\approx 3.5\times10^{10}$ protons/cm^2/s. The uniformity of the flux was within $\approx \pm 20\%$ over the beamspot of $\approx$ 1 cm diameter. The proton fluence was measured online using a calibrated ion chamber positioned in the proton beam, the signal from which was integrated and used to generated "Monitoring Pulses" (MON) after given increments of integrated proton fluence. The MON were used by the cyclotron control room to monitor the operation of the machine.

Using a 20 - 160 MeV proton beam allows us to simultaneously accumulate total ionizing dose (TID), 1 MeV-equivalent neutron fluence, and hadrons with sufficient energy to potentially cause SEE. The conversion factors are energy-dependent. For protons in this energy range, the 1 MeV-equivalent neutron fluence is somewhat higher than the actual proton fluence, though we assume a conversion factor of unity in order to be conservative. Table 3 summarizes the conversion for calculating the equivalent TID from the proton fluence.

Proton Energy (MeV)	Proton Fluence per MRad TID (10^{13} p/cm^2)
158	1.47
100	1.06
50	0.67
20	0.31

Table 3: Fluence of protons required to accumulate 1 MRad total ionizing dose, as a function of proton energy.

4 DAQ and Test Procedure

The radiation test setup utilizes the portable DAQ we developed for a variety of electronics testing and radiation qualification purposes. The DAQ is driven by a portable PC equipped with two National Instruments DAQ boards, one for digital I/O and the other for analog I/O and power connections.

A cable from the cyclotron control room provided a pulse for every MON unit. The pulses were counted using a general-purpose counter on the analog I/O board and read by the DAQ PC in order to provide online measurements of the integrated exposure.

Each DAQ I/O board is connected via its own 50-pin 75-foot twisted-pair cable to a "Sample Driver" board. The Sample Driver contains voltage regulators for providing power to the Device-Under-Test (DUT) fixture; the power supply currents and voltages can be measured through the analog I/O. In addition, four analog inputs and two DAC outputs are available to the DUT fixture. The digital I/O implements two 8-bit TTL ports, with strong TTL drivers and terminations on both ends of the cable.

For typical runs, the supply voltage and current of the DUT were monitored during the irradiation with a time resolution of $200\,\mu$s. Every second, the DAQ would record to disk the average value, RMS, maximum value and minimum value of both the voltage and current. The DAQ was programmed to record the entire history to disk if there was a significant variation of any of the values during any one second interval.

In case of an SEL occurrence, the supply current would be expected to rise dramatically. To prevent a possible fire hazard, the DAQ was programmed to switch off the power to the DUT if its supply current exceeded a pre-set limit. To see if the device would recover from a possible occurrence of SEL, the DAQ would automatically turn the power on again after 30 seconds. After 20 such power cycles, the DAQ would turn off the power permanently, and abort the run.

5 GainSel Tests

Table 4 summarizes the DSM GainSel chips irradiated during the two sets of pre-selection tests, all of which were performed with 158 MeV protons.

5.1 GainSel Test Procedure

Part of the GainSel logic operates at 40 MHz. Due to the long cables required to remove the PC from the radiation environment, it was not possible for the DAQ PC to directly verify the correct 40 MHz operation of the GainSel. Instead, the real-time control of the GainSel DUT was driven by an FPGA mounted on an "FPGA testjig" connected to the DUT testjig via short cables ($\approx$ 20 cm, long enough to allow the FPGA to be sufficiently shielded from the proton beam). All I/O pins of the GainSel were connected in this way to the FPGA, which could therefore monitor all GainSel activity in real time.

The FPGA compared all GainSel outputs cycle-by-cycle with its own emulated outputs in order to search for discrepancies signalling SEU or other error conditions. The test sequence would run until the FPGA detected a mismatch between any DUT output and the

MPW Run	Irradiation Test Date	Sample Number	Total Fluence ($p/cm^2/s$)	TID (MRad)	Total No. of SEU Errors
MPW4	7/29/01	C	8.3×10^{13}	5.6	24
	7/29/01	F	6.8×10^{13}	4.6	13
	8/19/01	G	22×10^{13}	15.0	26
	9/8/01	H	6.9×10^{13}	4.7	18
MPW6	5/16/02	1	1.76×10^{13}	1.2	0
	5/16/02	12	1.76×10^{13}	1.2	2
	5/16/02	2	1.76×10^{13}	1.2	2
	5/16/02	3	3.52×10^{13}	2.4	3
	5/17/02	4	1.76×10^{13}	1.2	1
	5/17/02	5	1.76×10^{13}	1.2	1

Table 4: Summary of DSM GainSel samples irradiated for the pre-selection radiation tests.

corresponding output from the GainSel emulator inside the FPGA. In case of a mismatch, the FPGA immediately stopped the test so that the internal registers of the FPGA could be read in order to diagnose the cause of the mismatch.

During the irradiation, the GainSel tests were performed with a fixed pattern of signals that were repeated until an SEU was detected by the FPGA. The length of the pattern was 256 clock cycles at 5 MHz. During the first half, the GainSel was triggered and configured to read out three events with three samples each. For the second half of the test pattern the signals were kept idle, to test for spurious GainSel output. Most of the SEUs observed were correctable bit flips in the stored configuration parameters (eg. gain thresholds), indicated by the setting of the appropriate error flags in the event format.

5.2 GainSel Current Monitoring Results

The current drawn by the DSM GainSel DUT was monitored during irradiation. As the integrated dose increased, the current exhibited a slight decrease; the current versus proton fluence is shown in Figure 1 for the six devices from MPW6 that were irradiated. Similar behavior has been seen in other chips produced with the same DSM process (for example, see reference [8]), where it has been attributed to an increase (in absolute value) of the threshold voltages of both the n-channel and p-channel transistors. This very small effect is of no concern for operation in ATLAS.

Apart from this gradual and steady decrease in current, the voltages and currents of all samples were stable during irradiation. No occurrences of latchup were observed.

5.3 GainSel SEU Results

During the irradiation, some logic errors were observed in the operation of the GainSel DUTs. These SEU-induced errors are summarized in the final column of Table 4.

Summing over all irradiated samples, a total of 90 SEU errors were observed for a total fluence of $56.3 \times 10^{13}\ p/cm^2$, yielding an SEU cross-section for the GainSel of $1.6 \times 10^{-13}\ cm^{-2}$.

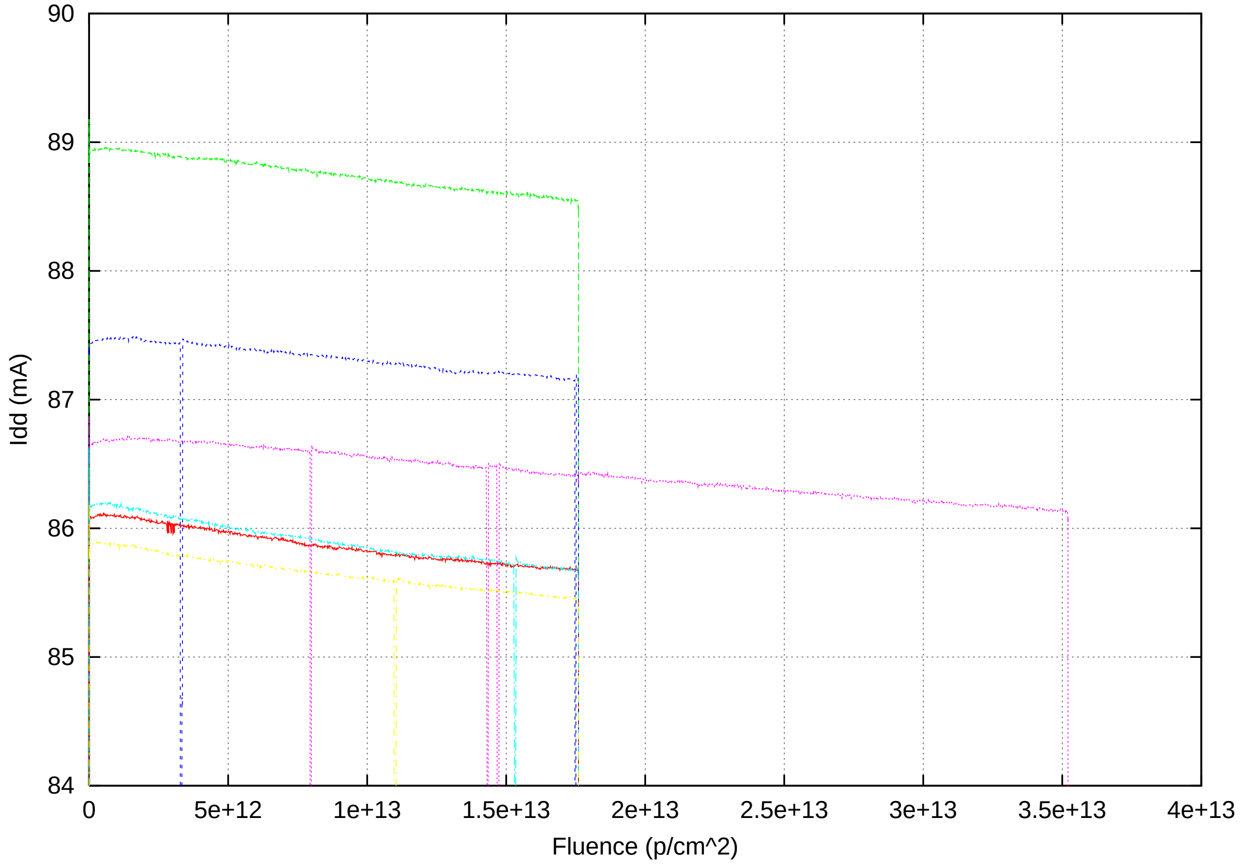

Figure 1: Measured supply current as a function of proton fluence for the six DSM GainSel chips from MPW6 that were irradiated.

This value is approximately a factor of 7.5 lower than the value of 12.0×10^{-13} cm^{-2} determined for the DMILL version of the GainSel chip, which was derived from the same Verilog code and therefore has the same design logically.

Analyzing the data of Table 4 separately for the chips from the two different MPW runs yields SEU cross-sections of $(1.8 \pm 0.2) \times 10^{-13}$ cm^{-2} and $(0.7 \pm 0.2) \times 10^{-13}$ cm^{-2} for the MPW4 and MPW6 chips, respectively (where the errors shown are purely statistical). This difference likely arises not from differences in the GainSel chips themselves but in the test setup; after the MPW4 tests were completed, it was discovered that the oscillator used on the FPGA jig was not well matched to the FPGA used, increasing the possibility that some of the observed errors were due in fact to FPGA errors. This was corrected before the MPW6 runs. To be conservative, we attribute all errors to SEU in the GainSel DUT and take the cross-section value of 1.6×10^{-13} cm^{-2} determined averaging the results for both sets of chips.

5.4 Discussion of GainSel Results

Since a total of 896 FEBs are required to instrument the full EM Barrel and each FEB contains 8 GainSel chips, the EM Barrel readout includes a total of 7168 GainSel chips. The measured SEU cross-section per GainSel chip of 1.6×10^{-13} cm^{-2} implies a total of 8830 SEU errors per 10 years of LHC operation at design luminosity, including a safety factor of 10. Assuming 10^7 s of LHC operation per year, this corresponds to an SEU-induced error in the EM Barrel readout every 3.1 hours. Even this very low rate is a conservative estimate, since most of the errors are automatically corrected via the redundant storage and SEU protection of the GainSel design, and we have applied the measured cross-section for 158 MeV protons to all hadrons above 20 MeV.

6 CLKFO Tests

Table 5 summarizes the DSM CLKFO chips irradiated during the two sets of pre-selection tests, all of which were performed with 158 MeV protons.

MPW Run	Irradiation Test Date	Sample Number	Total Fluence ($p/cm^2/s$)	TID (MRad)
MPW4	9/8/01	A	6.9×10^{13}	4.7
	9/8/01	C	13.7×10^{13}	9.3
MPW6	5/19/02	A2	1.6×10^{13}	1.1
	5/19/02	B2	1.6×10^{13}	1.1
	5/19/02	C2	1.6×10^{13}	1.1
	5/19/02	D2	1.6×10^{13}	1.1

Table 5: Summary of DSM CLKFO samples irradiated for the pre-selection radiation tests.

During the irradiation, we used an external pulse generator to send a 40 MHz differential clock signal to the input of the CLKFO DUT, and were able to observe one of the CLKFO output signals on an oscilloscope. Depending on jumper settings on the DUT jig, the observed output could be either the clipped WCLK signal or the signal generated by the counter. The input and output differential signals were transmitted over ≈ 50 m coax cables installed between the control room and the cyclotron vault.

For example, Figure 2 displays the clipped WCLK signal measured using the infinite persistence setting of the oscilloscope during the irradiation of one CLKFO sample. Shown is the input signal (upper traces), the output signal (lower traces) and the resultant signal after the differential reception.

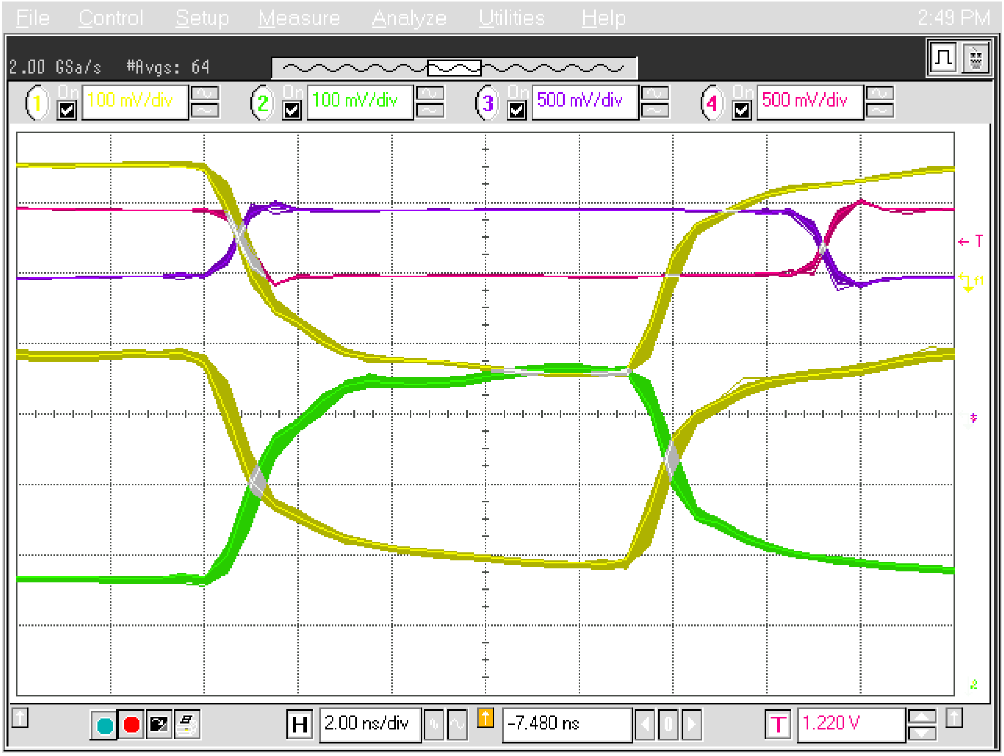

Figure 2: Signals measured during the CLKFO irradiation. For further details, see the text.

The DUT jig also allowed the current to be monitored online. Figure 3 shows the test jig current versus fluence for the six CLKFO chips which were irradiated.

During monitoring of the 5 MHz output, performed for three of the chips, no occurrences of SEU of the triple-redundant counter were observed.

7 Summary and Conclusions

A number of DSM GainSel and CLKFO samples have been irradiated to 158 MeV proton beams. The results demonstrate the devices are sufficiently tolerant to radiation to pass the pre-selection criteria for use in the FEBs of the ATLAS LAr readout.

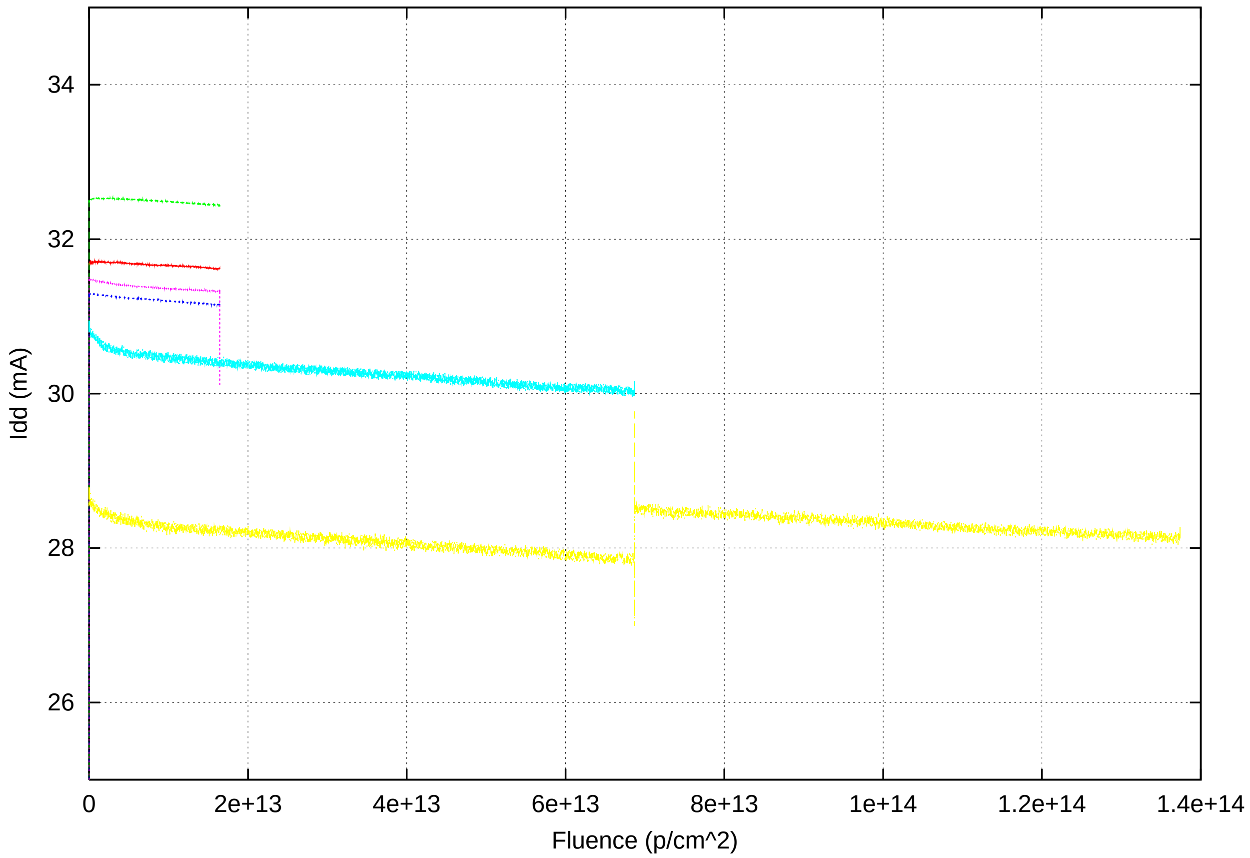

Figure 3: Measured supply current as a function of proton fluence for the six DSM CLKFO chips that were irradiated.

References

[1] S. Böttcher et. al., "The SCA Controller for the ATLAS LAr Calorimeter" (available at `www.nevis.columbia.edu/~atlas/electronics/asics/scac/scac-dsm.ps`).

[2] S. Böttcher et. al., "The Gain Selector ASIC for the ATLAS LAr Calorimeter" (available at `www.nevis.columbia.edu/~atlas/electronics/asics/ggains/gainsel.ps`).

[3] S. Böttcher et. al., "The Clock Fanout ASIC for the ATLAS LAr Calorimeter" (available at `www.nevis.columbia.edu/~atlas/electronics/asics/clkfo/clkfo.ps`).

[4] S. Böttcher et. al., "Status of Functional and Radiation Testing of the Deep Submicron SCA Controller" (available at `www.nevis.columbia.edu/~atlas/electronics/asics/scac/SCACtest.ps`).

[5] D. Gingrich et. al., "Radiation Qualification of the SCA Controller Preselection" (available at `/~ftp://jever.phys.ualberta.ca/pub/atlas/dsm/prr/scac-preselection.pdf`).

[6] These radiation levels are based on the November 18, 2000 baseline and are available at `atlas.web.cern.ch/Atlas/GROUPS/FRONTEND/radhard.htm`.

[7] For more information on the Harvard Cyclotron Laboratory, see `neurosurgery.mgh.harvard.edu/hcl/flyer.htm`.

[8] Ph.D. thesis of G. Anelli, Grenoble (2000).