14. Package Information for Arria GX Devices

AGX52014-1.0

Introduction

This chapter provides package information for Altera® Arria™ GX devices, including:

- Device and package cross reference
- Thermal resistance values
- Package outlines

Tables 14–1 shows which Altera Arria GX devices, respectively, are available in FineLine BGA® (FBGA) packages.

Table 14–1. Arria GX Devices in FBGA Packages

Device	Package	Pins
EP1AGX20	Flip-chip FBGA	484
	Flip-chip FBGA	780
EP1AGX35	Flip-chip FBGA	484
	Flip-chip FBGA	780
EP1AGX50	Flip-chip FBGA	484
	Flip-chip FBGA	780
	Flip-chip FBGA	1152
EP1AGX60	Flip-chip FBGA	484
	Flip-chip FBGA	780
	Flip-chip FBGA	1152
EP1AGX90	Flip-chip FBGA	1152

Thermal Resistance

Thermal resistance values for Arria GX devices are provided for a board that meets JDEC specifications and for a typical board. The following values are provided:

- θ_{JA} (°C / W) still air—Junction-to-ambient thermal resistance with no air flow when a heat sink is not used.
- θ_{JA} (°C / W) 100 ft. / min.—Junction-to-ambient thermal resistance with 100 ft. / min. airflow when a heat sink is not used.
- θ_{JA} (°C / W) 200 ft. / min.—Junction-to-ambient thermal resistance with 200 ft. / min. airflow when a heat sink is not used.
- θ_{JA} (°C / W) 400 ft. / min.—Junction-to-ambient thermal resistance with 400 ft. / min. airflow when a heat sink is not used.
- θ_{JC}—Junction-to-case thermal resistance for device.
- θ_{JB}—Junction-to-board thermal resistance for device.

Table 14–2 provides θ_{JA} (junction-to-ambient thermal resistance), θ_{JC} (junction-to-case thermal resistance), and θ_{JB} (junction-to-board thermal resistance) values for Arria GX devices.

Table 14–2. Arria GX GX Device Thermal Resistance

Device	Pin Count	Package	θ_{JA} (° C/W) Still Air	θ_{JA} (° C/W) 100 ft./min.	θ_{JA} (° C/W) 200 ft./min.	θ_{JA} (° C/W) 400 ft./min.	θ_{JC} (° C/W)	θ_{JB} (° C/W)
EP1AGX20	484	FBGA	12.8	10.3	8.7	7.5	0.3	3.14
	780	FBGA	11.1	8.6	7.2	6.0	0.24	3.14
EP1AGX35	484	FBGA	12.8	10.3	8.7	7.5	0.3	3.14
	780	FBGA	11.1	8.6	7.2	6.0	0.24	3.14
EP1AGX50	484	FBGA	12.7	10.2	8.6	7.3	0.2	2.86
	780	FBGA	10.9	8.4	6.9	5.8	0.15	2.84
	1152	FBGA	9.9	7.5	6.1	5.0	0.15	2.5
EP1AGX60	484	FBGA	12.7	10.2	8.6	7.3	0.2	2.86
	780	FBGA	10.9	8.4	6.9	5.8	0.15	2.84
	1152	FBGA	9.9	7.5	6.1	5.0	0.15	2.5
EP1AGX90	1152	FBGA	9.6	7.3	5.9	4.9	0.11	2.33

Package Outlines

The package outlines are listed in order of ascending pin count. Altera package outlines meet the requirements of *JEDEC Publication No. 95.*

484-Pin FBGA - Flip Chip

- All dimensions and tolerances conform to ASME Y14.5M – 1994.
- Controlling dimension is in millimeters.
- Pin A1 may be indicated by an ID dot, or a special feature, in its proximity on the package surface.

Tables 14–3 and 14–4 show the package information and package outline figure references, respectively, for the 484-pin FBGA packaging.

Table 14–3. 484-Pin FBGA Package Information

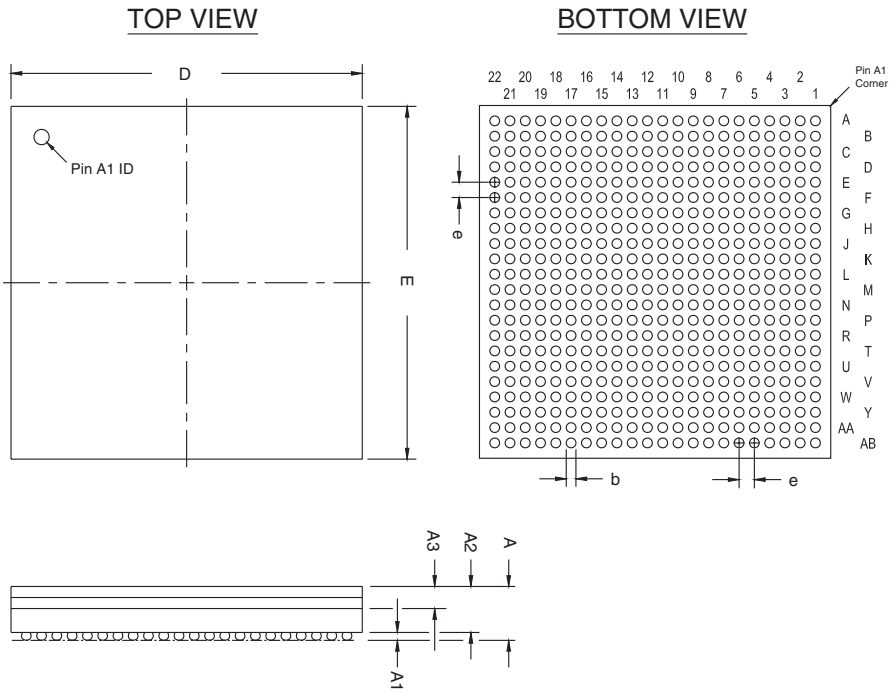
Description	Specification
Ordering code reference	F
Package acronym	FBGA
Substrate material	BT
Solder ball composition	Regular: 63Sn:37Pb (Typ.) Pb-free: Sn:3Ag:0.5Cu (Typ.)
JEDEC outline reference	MS-034 variation: AAJ-1
Maximum lead coplanarity	0.008 inches (0.20 mm)
Weight	7.1 g
Moisture sensitivity level	Printed on moisture barrier bag

Table 14–4. 484-Pin FBGA Package Outline Dimensions

Symbol	Millimeter		
	Min.	Nom.	Max.
A	–	–	3.50
A1	0.30	–	–
A2	0.25	–	3.00
A3	–	–	2.50
D	23.00 BSC		
E	23.00 BSC		
b	0.50	0.60	0.70
e	1.00 BSC		

Figure 14–1 shows a package outline for the 484-pin FineLine BGA packaging.

Figure 14–1. 484-Pin FBGA Package Outline



780-Pin FBGA - Flip Chip

- Arria GX Device Handbook, Volume 2All dimensions and tolerances conform to ASME Y14.5M - 1994.
- Controlling dimension is in millimeters.
- Pin A1 may be indicated by an ID dot, or a special feature, in its proximity on package surface.

Tables 14–5 and 14–6 show the package information and package outline figure references, respectively, for the 780-pin FBGA packaging.

Table 14–5. 780-Pin FBGA Package Information

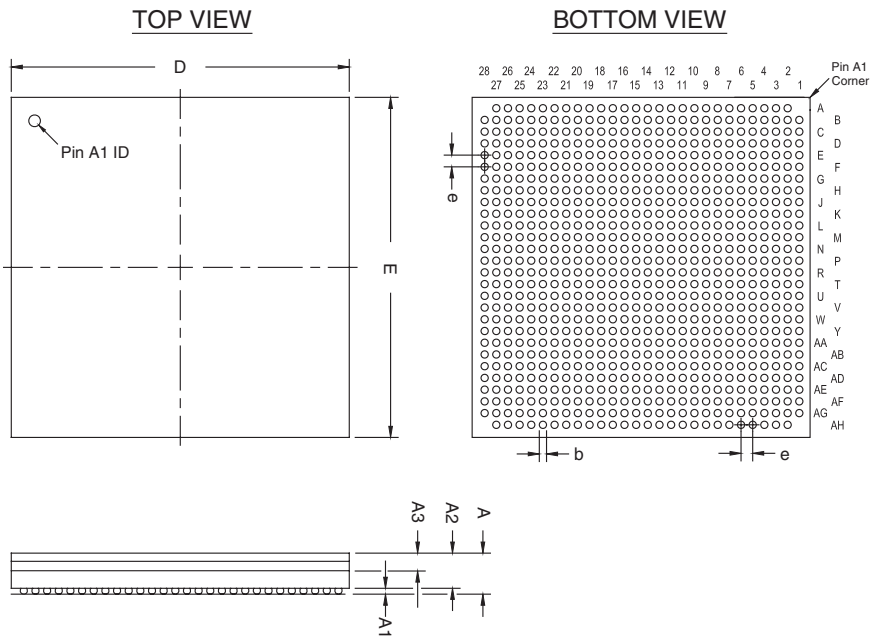
Description	Specification
Ordering code reference	F
Package acronym	FBGA
Substrate material	BT
Solder ball composition	Regular: 63Sn:37Pb (Typ.) Pb-free: Sn:3Ag:0.5Cu (Typ.)
JEDEC outline reference	MS-034 variation: AAM-1
Maximum lead coplanarity	0.008 inches (0.20 mm)
Weight	11.9 g
Moisture Sensitivity Level	Printed on moisture barrier bag

Table 14–6. 780-Pin FBGA Package Outline Dimensions

Symbol	Millimeters		
	Min.	Nom.	Max.
A	–	–	3.50
A1	0.30	–	–
A2	0.25	–	3.00
A3	–	–	2.50
D	29.00 BSC		
E	29.00 BSC		
b	0.50	0.60	0.70
e	1.00 BSC		

Figure 14–2 shows a package outline for the 780-pin FineLine BGA packaging.

Figure 14–2. 780-Pin FBGA Package Outline



1,152-Pin FBGA - Flip Chip

- All dimensions and tolerances conform to ASME Y14.5M - 1994.
- Controlling dimension is in millimeters.
- Pin A1 may be indicated by an ID dot, or a special feature, in its proximity on package surface.

Tables 14–7 and 14–8 show the package information and package outline figure references, respectively, for the 1,152-pin FBGA packaging.

Table 14–7. 1,152-Pin FBGA Package Information

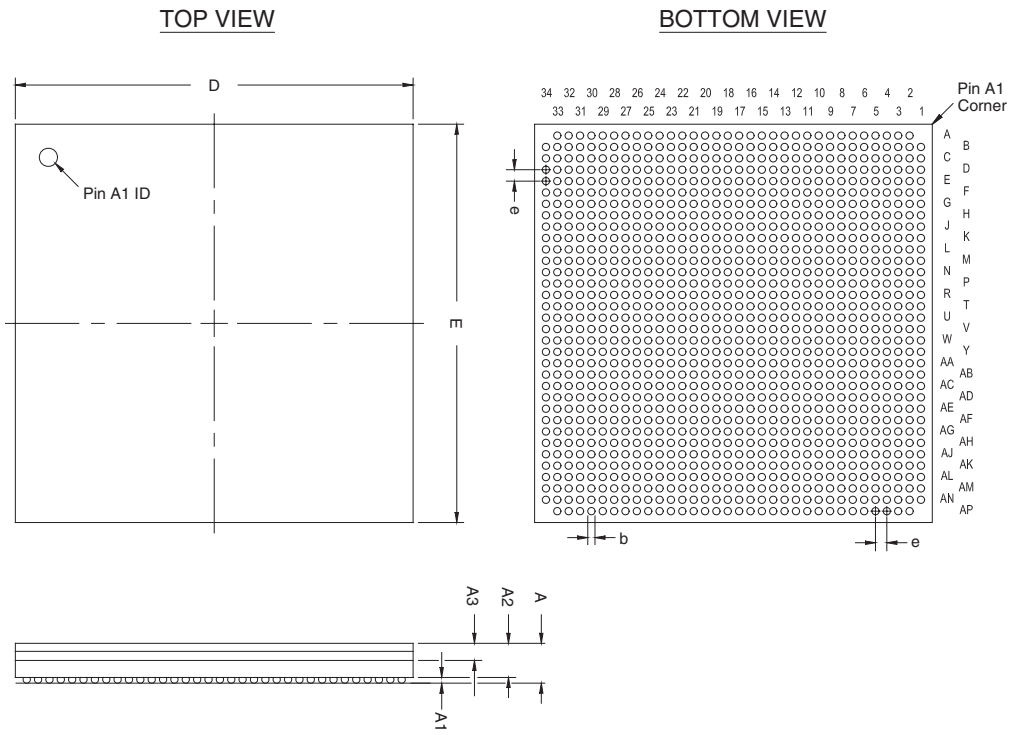
Description	Specification
Ordering code reference	F
Package acronym	FBGA
Substrate material	BT
Solder ball composition	Regular: 63Sn:37Pb (Typ.) Pb-free: Sn:3Ag:0.5Cu (Typ.)
JEDEC outline reference	MS-034 variation: AAR-1
Maximum lead coplanarity	0.008 inches (0.20 mm)
Weight	15.8 g
Moisture sensitivity level	Printed on moisture barrier bag

Table 14–8. 1,152-Pin FBGA Package Outline Dimensions

Symbol	Millimeters		
	Min.	Nom.	Max.
A	–	–	3.50
A1	0.30	–	–
A2	0.25	–	3.00
A3	–	–	2.50
D	35.00 BSC		
E	35.00 BSC		
b	0.50	0.60	0.70
e	1.00 BSC		

Figure 14–3 shows a package outline for the 1,152-pin FineLine BGA packaging.

Figure 14–3. 1,152-Pin FBGA Package Outline



Document Revision History

Table 14–9 shows the revision history for this document.

Table 14–9. Document Revision History

Date and Document Version	Changes Made	Summary of Changes
May 2007 v1.0	Initial Release	N/A