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I/O Specification for Serial Receiver Daughter Board (PCB-0140-RCV)

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1.0 Introduction

The Serial Receiver Daughter Board accepts an 8b/10b encoded serial data stream, operating at rates from 956 Mbits/sec to 1,168 Mbits/sec, and converts it to 16 parallel data lines operating at data rates from 47.8 MHz to 58.4 MHz. This document is intended to explain the electrical and physical requirements for using this board.

2.0 Input and Outputs

The following sections describe the I/O connectors on the Serial Daughter Board.

2.1 Serial Inputs

The serial input to the Serial Receiver Daughter Board is through a MCX 50 Ω coax connector that is mounted directly on the board.

2.2 Parallel Outputs

The parallel data is output through a 30 pin connector (Samtec P/N TFM-115-02-S-D-LC). The outputs and power connections are shown in Table 1. The output levels are compatible with either 5V or 3.3V logic families. Ref_Clock is input from the motherboard and should be at the RF Clock frequency, this signal is used to keep the on board PLL operating when there is no input signal.

Receive_Clock is the extracted clock from the input signal, which operates at the RF frequency, all other outputs are referenced to this clock. This clock is the same frequency as the RF Clock but may not be phase aligned with the clock on the board where it is mounted since the phase of this clock depends on the length of the cable carrying the serial input data. Most users will use a FIFO to switch the parallel data from the received clock to the local clock.

The DAV* is low when there is valid data on the Data_Out lines.

The Parity_Error signal indicates that the longitudinal parity on the 7th received word has been detected as having an error, this signal stays true for a full word time (7 rf clock pulses). The Receiver Daughter Board starts counting words as soon as the serial input data stream switches from idles (Fiber Channel K28.5) to data and then assumes every 7th word contains parity. User's who are not using parity can ignore this signal.

The Enable signal allows normal operation of the receiver when at a high level. The Enable signal being low will cause all data lines to be in a high impedance state. The DAV signal will operate normally independent of the state of this signal.

The Lock_Okay / Reset signal serves as both an output and an input signal. It has an internal pull up resistor and is high during normal operation when the receiver is receiving good data. When the receiver drives this signal low, it is not receiving good data (i.e. when the input cable is not connected) and the receiver is forced into a reset state. The receiver can also be forced into a reset state by externally driving this signal low when it is high. An open collector signal or a signal with a passive pull up should drive this signal.

The Out_Control_0 and Out_Control_1 signals are used, in combination with an internal Lock detect signal, to control the state of the parallel outputs of the board. Table 2 shows the states of these control signals.

Table 1 - Parallel Outputs

Pin #	Signal Name	I/O	Level	Description
1	GND	-	-	Ground
2	GND	-	-	Ground
3	Data_Out_0	O		LSB of Output Data
4	Data_ Out _1	O		Output Data
5	Data_ Out _2	O		"
6	Data_ Out _3	O		"
7	Data_ Out _4	O		"
8	Data_ Out _5	O		"
9	Data_ Out _6	O		"
10	Data_ Out _7	O		"
11	Data_ Out _8	O		"
	Data_ Out _9	O		"
13	Data_ Out _10	O		"
14	Data_ Out _11	O		"
15	Data_ Out _12	O		"
16	Data_ Out _13	O		"
17	Data_ Out _14	O		"
18	Data_ Out _15	O		MSB of Output Data
19	DAV*	O		Data Available
20	Ref_Clock	I		Reference Clock Input
21	Out_Control_0	I		See Table 2
22	Parity_Error	O		Indicates Parity Error in previous word.
23	Receive_Clock	O		RF Clock Output
24	GND	-		Ground
25	Lock_Okay / Reset	O / I		Dual purpose signal (see below)
26	+5V	-		+5 volt Power Supply
27	-	-		Not Used
28	Out_Control_1	I		See Table 2
29	+3.3V	-		+3.3 volt Power Supply
30	+3.3V	-		+3.3 volt Power Supply

2.3 JTAG/Programming Connector

A 10 pin connector (Samtec P/N TFM-105-02-S-D-A) is provided for those users who wish to use the JTAG Boundary Scan Test capabilities of the Altera EPLD that drives the output lines of the Serial Receiver Daughter Board, or to reprogram the EPLD in circuit. Users that do not wish to use the Boundary Scan Test or to reprogram the Serial Transmitter card in system can ignore this connector. Table 3 shows the pin assignments for this connector.

Table 2 - Output Control

Out_Control_0	Out_Control_1	Lock_Detect[1]	Function
0	0	-	Outputs Tri-state
0	1	-	Outputs Enabled, All Data Low
1	0	0	Outputs Enabled, Data Normal
1	0	1	Outputs Tri-state
1	1	-	Outputs Tri-state

NOTE 1: Lock_Detect is an internal signal indicating valid serial data is present

3.1 Timing Requirements

Table 3 - JTAG Connections

Pin #	Label	Description
1	TCK	Test Clock In
2	GND	Ground
3	TDO	Test Data Out
4	Vcc	+5v
5	TMS	Test Mode Select
6	GND	Ground
7	GND	Ground
8	GND	Ground
9	TDI	Test Data In
10	GND	Ground

Figure 1 shows the relationship between Receive_Clock and the parallel data lines. Note that the Parity Error signal is one bunch crossing behind the data that is being received. All output lines change a maximum of 4.5ns after the rising edge of the Receive_Clock.22

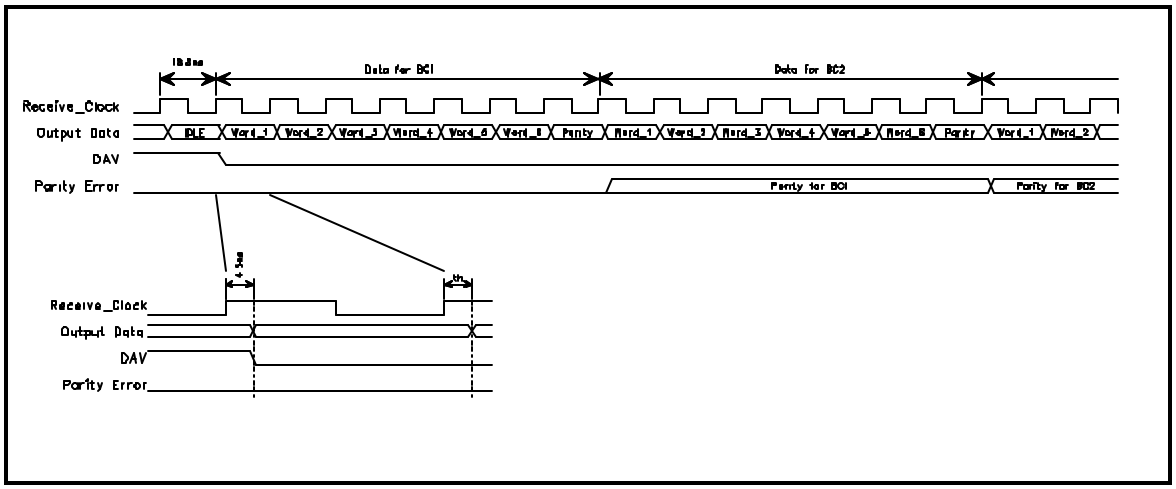

Figure 1 - Receive Timing

4.0 Mechanical Layout

The Serial Transmitter Daughter Board is 1.5" x 2.2" and has 4 mounting holes as well as the connectors that attach to the daughter board. Figure 2 shows the mechanical arrangement of the board.

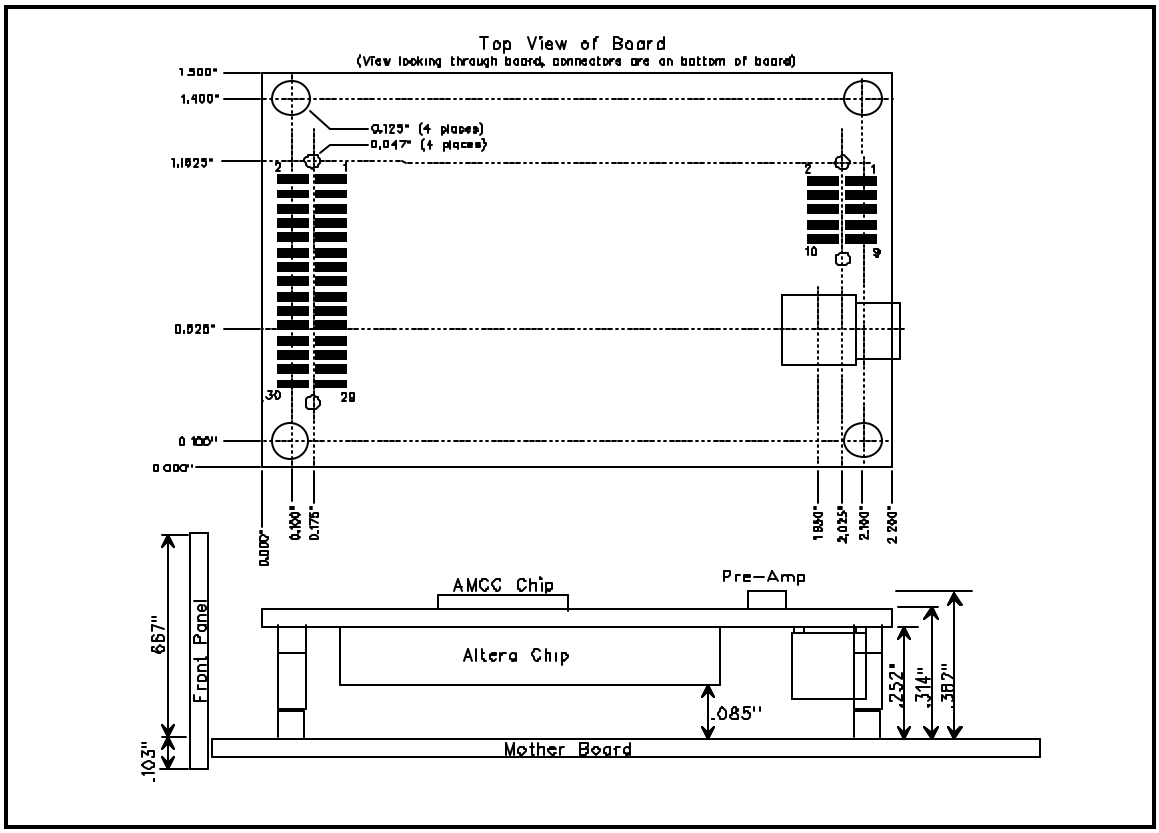

Figure 2 - Mechanical Dimensions

Appendix A - Board Schematic