Towards an ADC for the Liquid Argon Electronics Upgrade

Gustaaf Brooijmans

COLUMBIA UNIVERSITY
IN THE CITY OF NEW YORK

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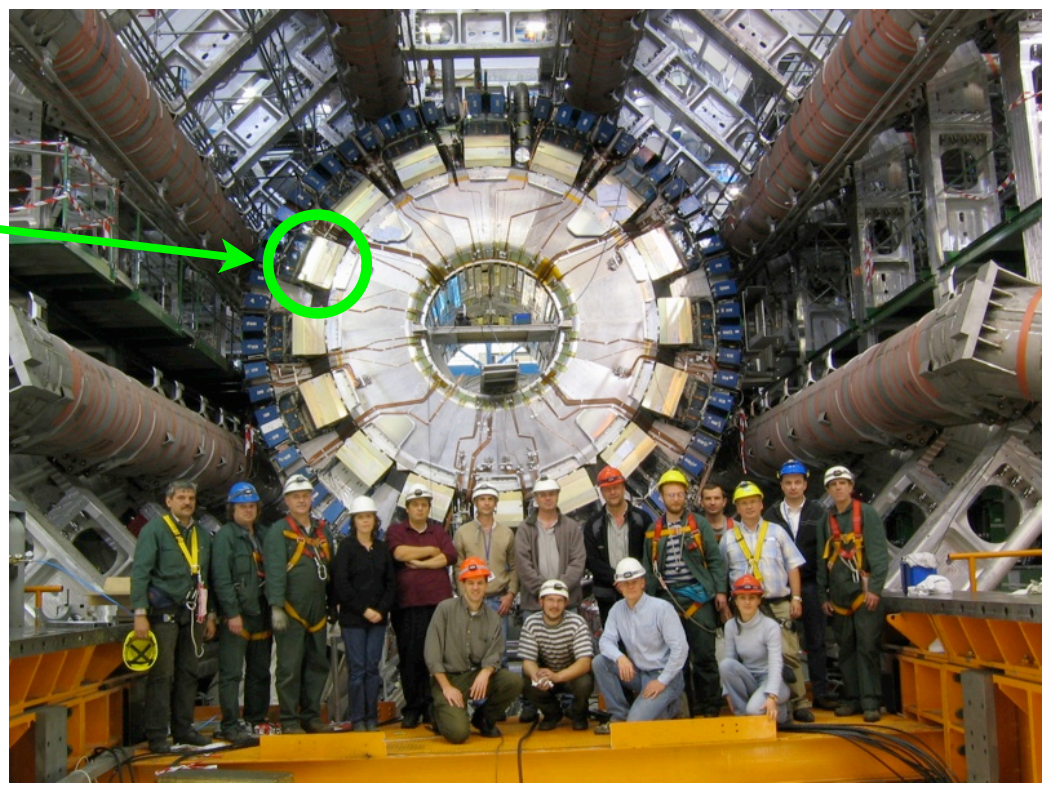
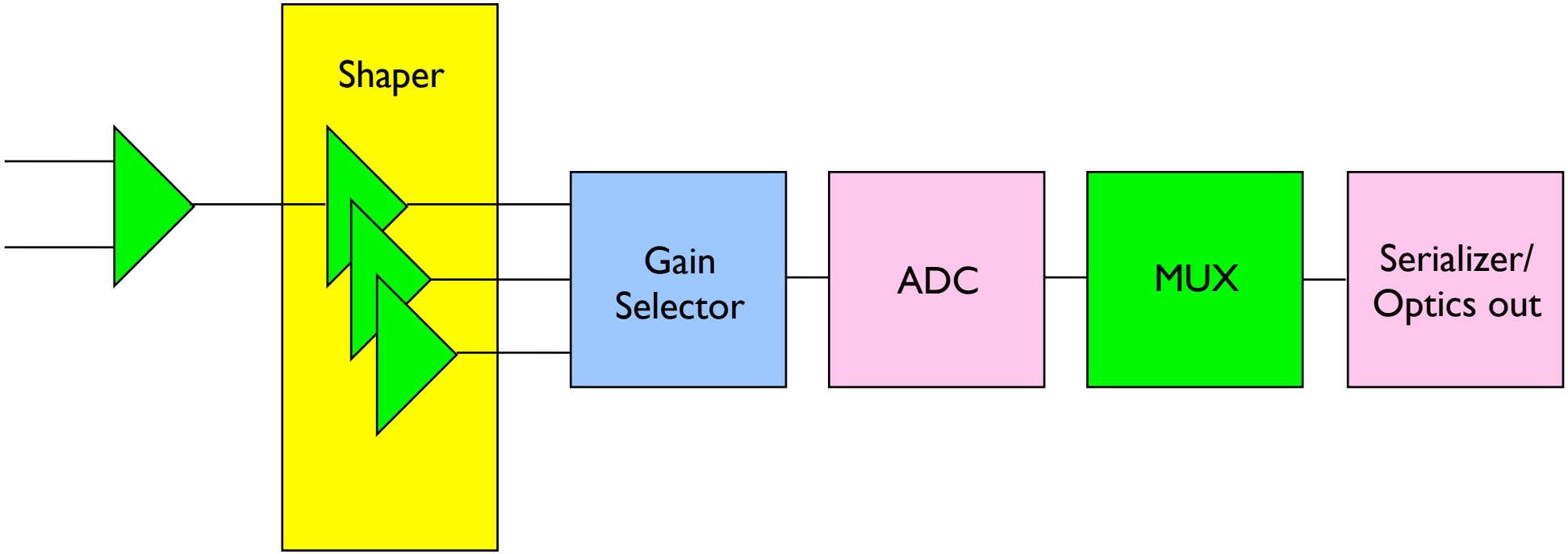
Current LAr FEB

- Existing FEB (radiation tolerant for LHC, but sLHC?)
  - Limits L1 latency to ~2.5 μs
  - Designed for L1 bandwidth up to ~100 kHz
  - Trigger sums on FEB → limits granularity available to L1Calo

Front-end crate location: radiation environment, limits on space, power consumption (cooling)



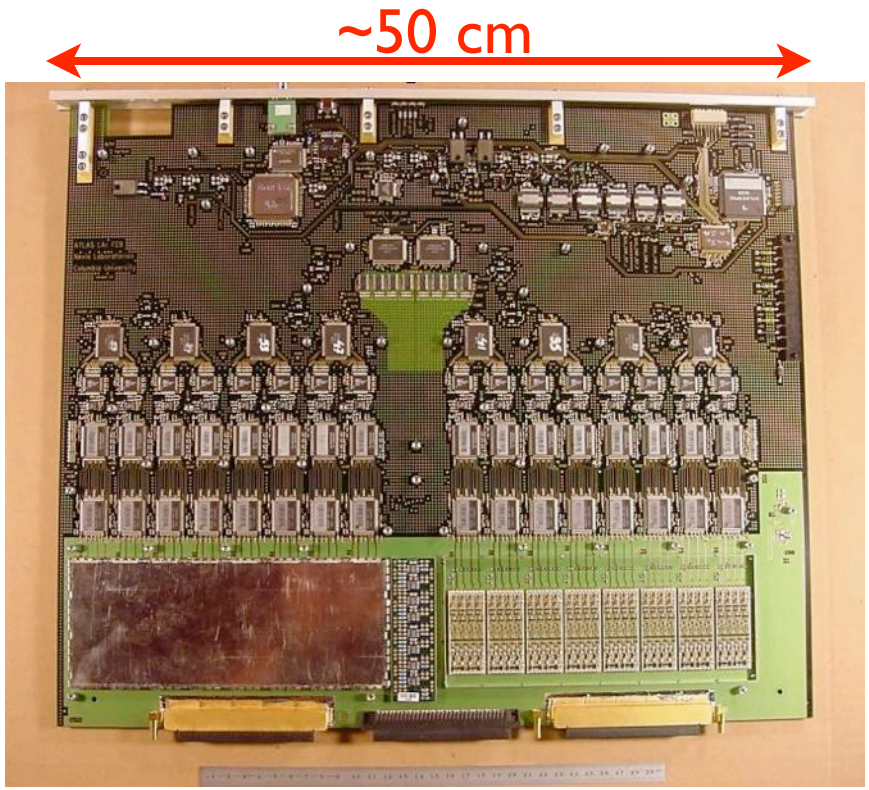
Tentative FEB2 Architecture



- Digitize at 40 MHz (no analog pipeline)
  - Doesn't change if bunch-crossing rate goes to 50 ns
- Move pipeline off-detector → 100+ Gbps/board
  - Implies upgrading back-end
  - (Fall-back has digital pipeline on-detector)

Main ADC Requirements

- Dynamic range:
  - Currently 16 bits (achieved by 3x12), not likely to change
- Power:
  - 80 W per board (128 channels), not likely to change by much
- Geometry:
  - ~50 cm "high" → ~8 mm/channel
  - Small ADC, serialized outputs

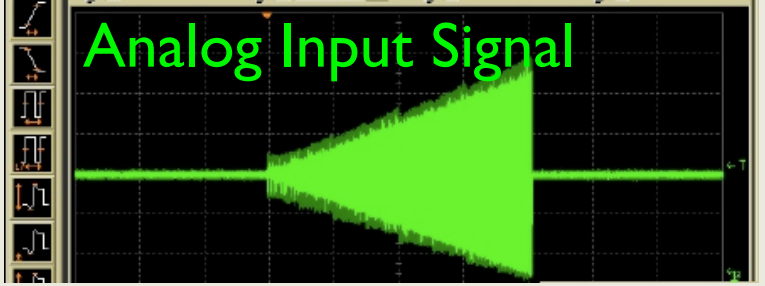


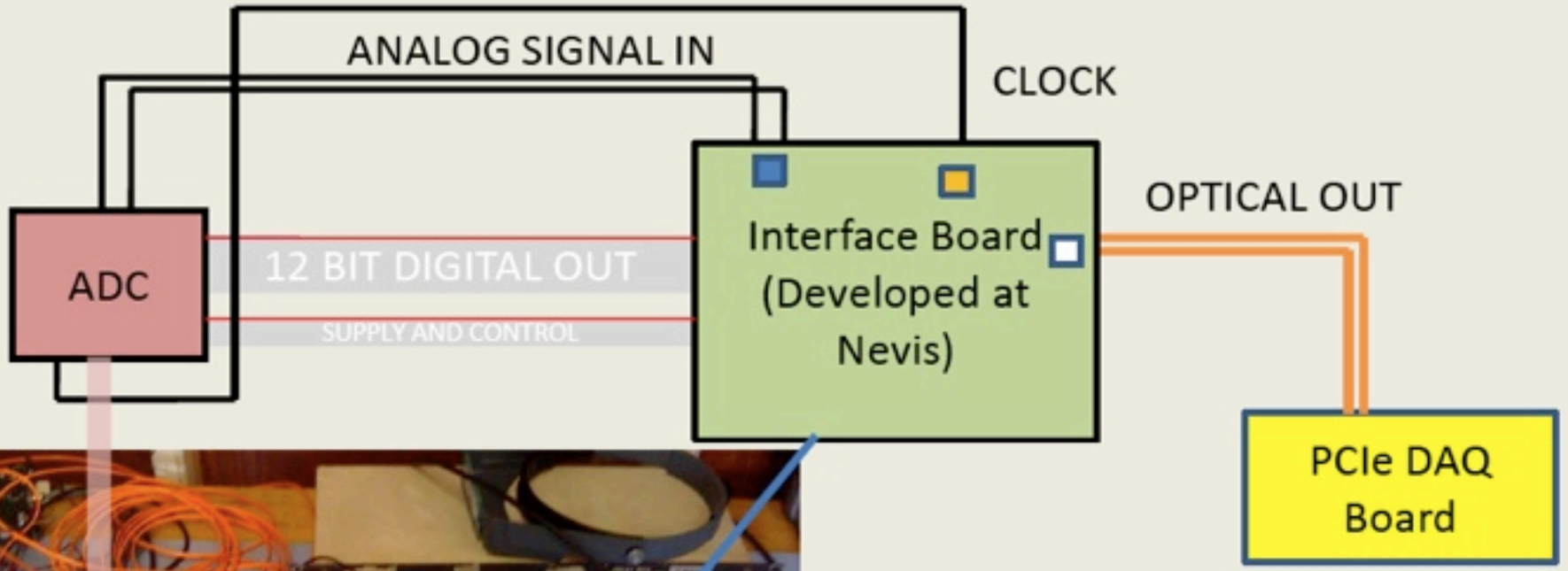
Commercial ADCs

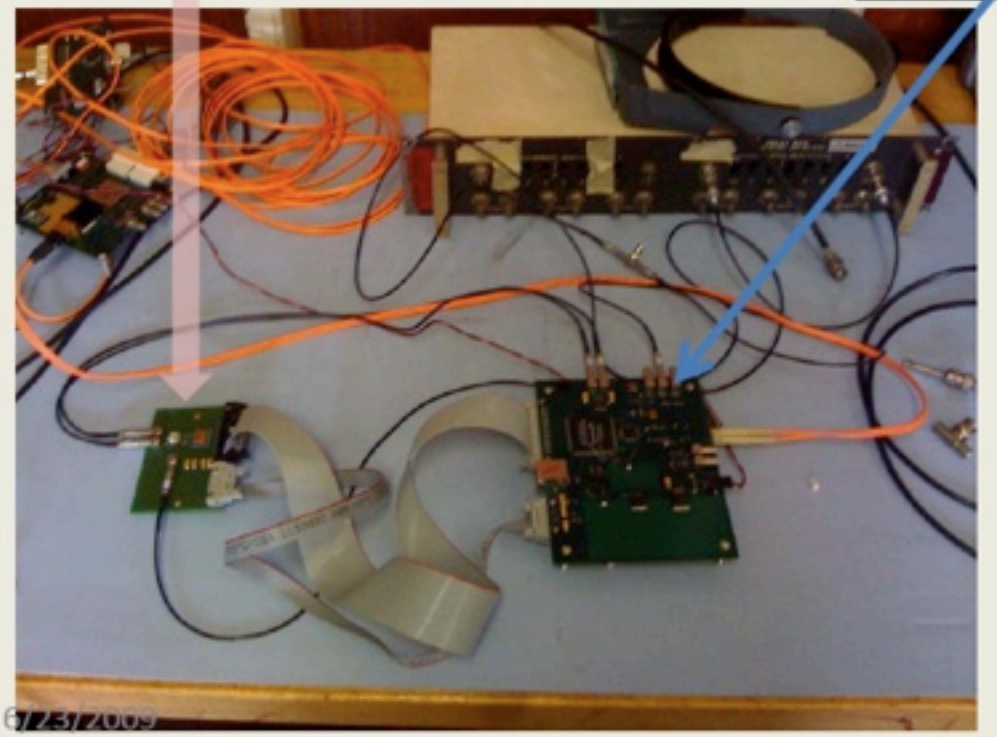
- Most are unlikely to be sufficiently rad hard given flexible features (registers for mode setting etc.)
  - Irradiate to verify
- Developed new setup:
  - ADC board with minimal number of added components
    - Send output data over LVDS (max 50 cm)
    - Tested **ST-RHF1201,** designed for military applications ($$)
    - Interface board with: DAC to inject signals to ADC, LVDS receivers, optical link to DAQ in PC (~7m away)
  - New PCI express DAQ board with optical receiver

Nikiforos Nikiforou

Test setup



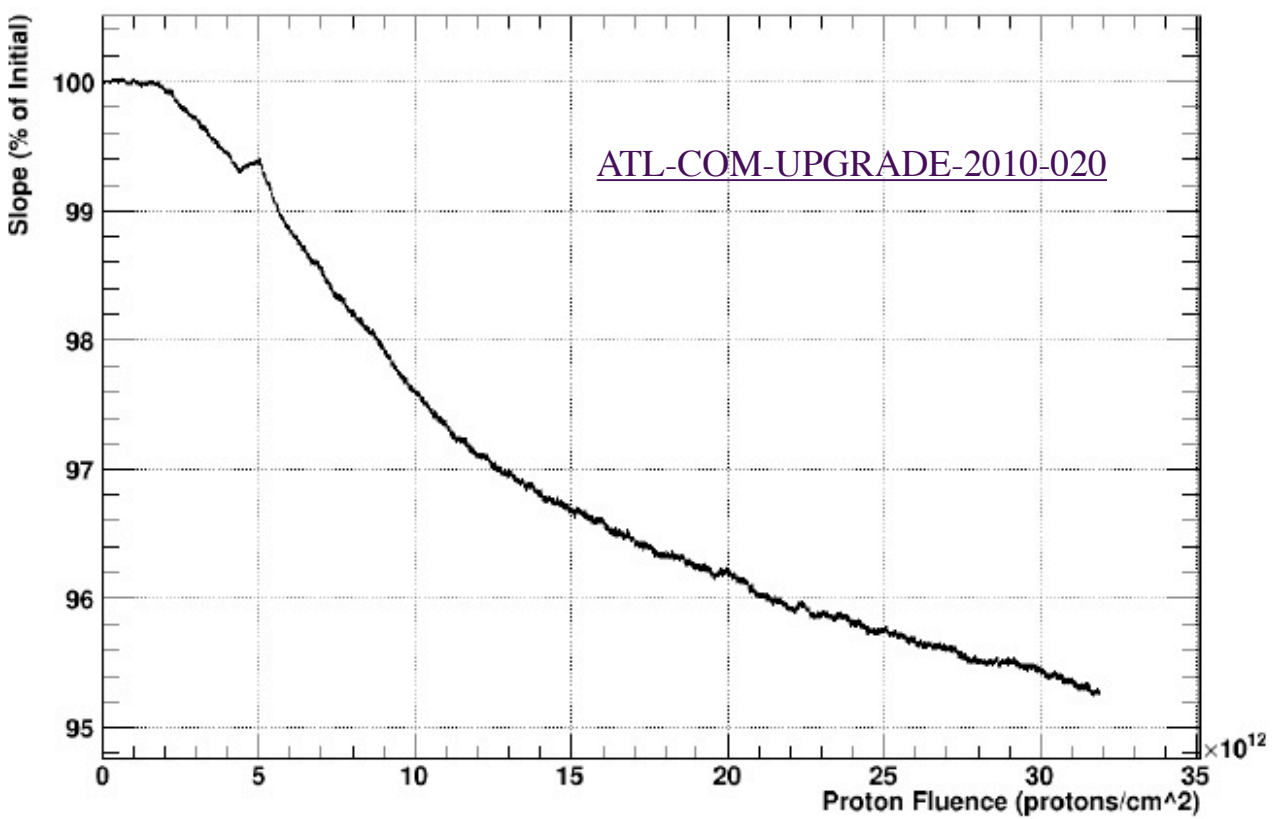




The interface board does everything:
-Produces the analog test signal
-Controls the ADC
-Receives, serializes and transmits the Digital signal over optical connection

ST Irradiation Results

- We irradiated the ST (spec: rad tolerant to 300 kRad) ADC at Mass. General Hospital (protons) in early October 2009
  - ST: degradation in ramp slope: 5% at 300 kRad

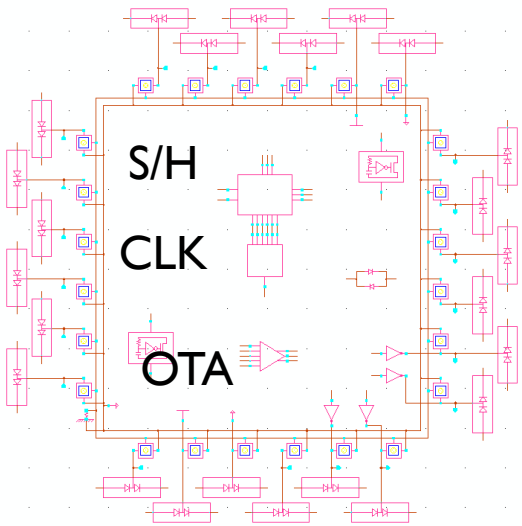


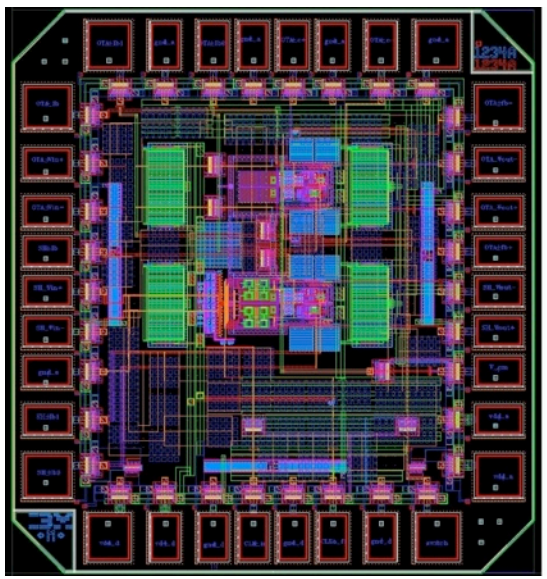
ADC Development Work

- Scaling LHC radiation tolerance requirements, we need 1-2 MRad (but it may be less)
- Have started development of custom ADC
- Given the power, dynamic range, speed & geometrical constraints:
  - Pipelined ADC (1.5 bits/stage) with digital error correction
  - Incorporated gain selector
  - Serialized digital outputs
- Collaboration with Columbia EE group specializing in low voltage analog designs: Peter Kinget et al.

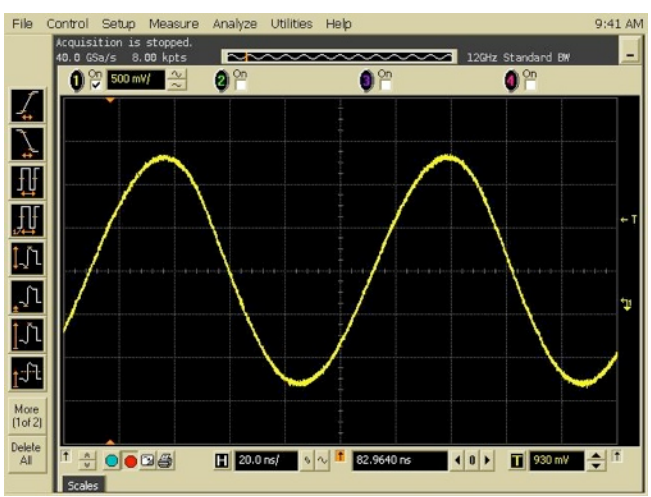
Nevis09 Chip

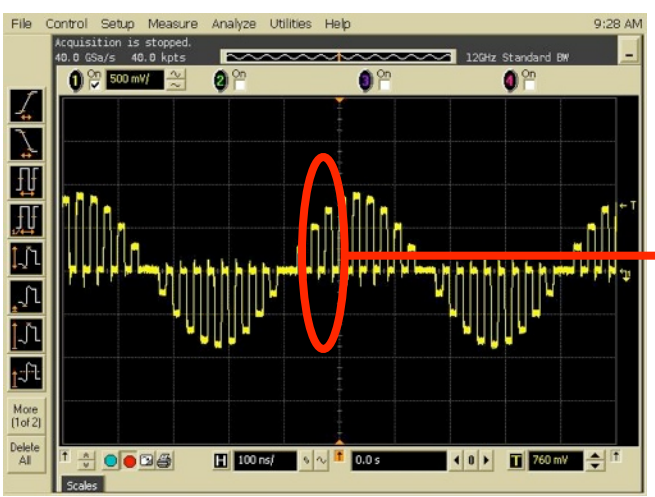
- First test-chip: OTA + S/H, crucial components of an ADC stage

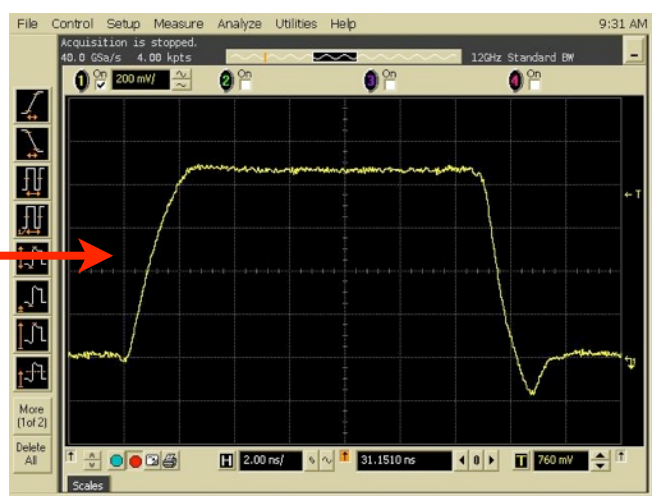




- Inject sinusoidal curve, check OTA & S/H outputs

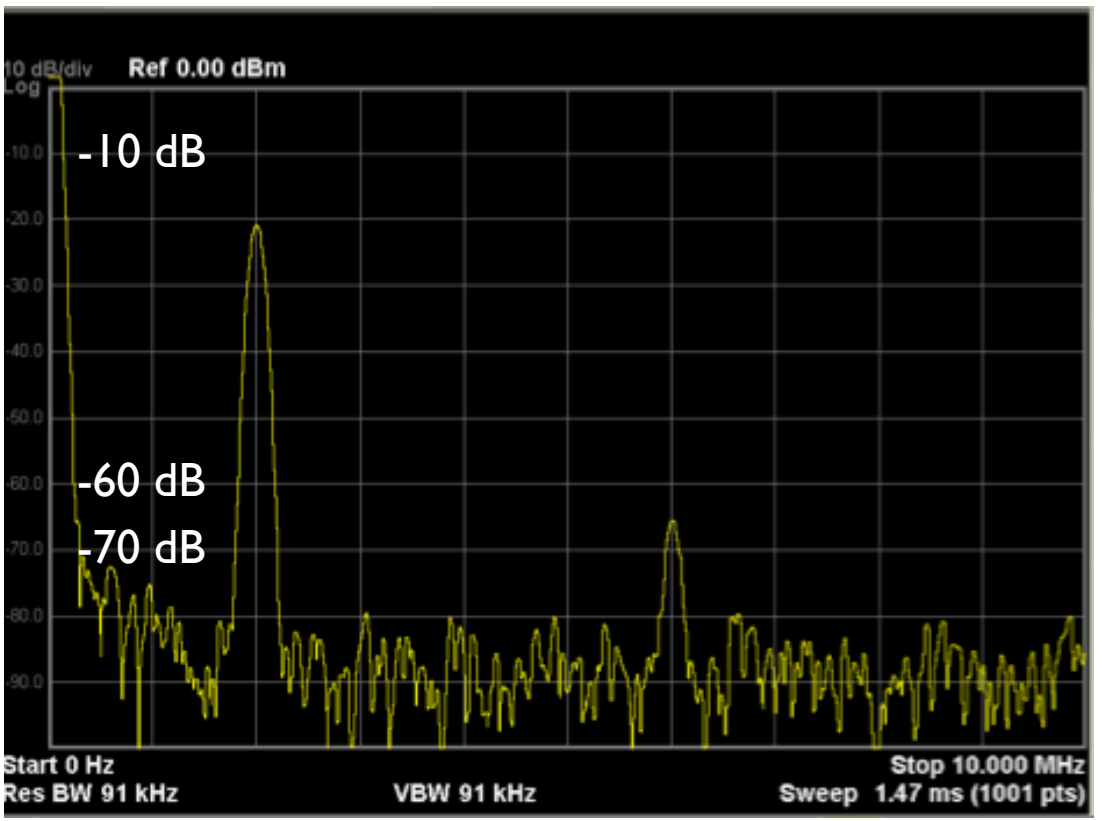






Nevis09 Tests

- Test, irradiate and retest
  - Irradiations to 3, 5, 10 and 20 10^{13} p/cm^2
  - This is approx. 1.5, 2.5, 5 and 10 MRad
- Spectral analysis
- S/H output analysis:
  - Amplitude
  - Rise/Fall time
- No change after irradiation



- Tests only accurate to ~11 bits...

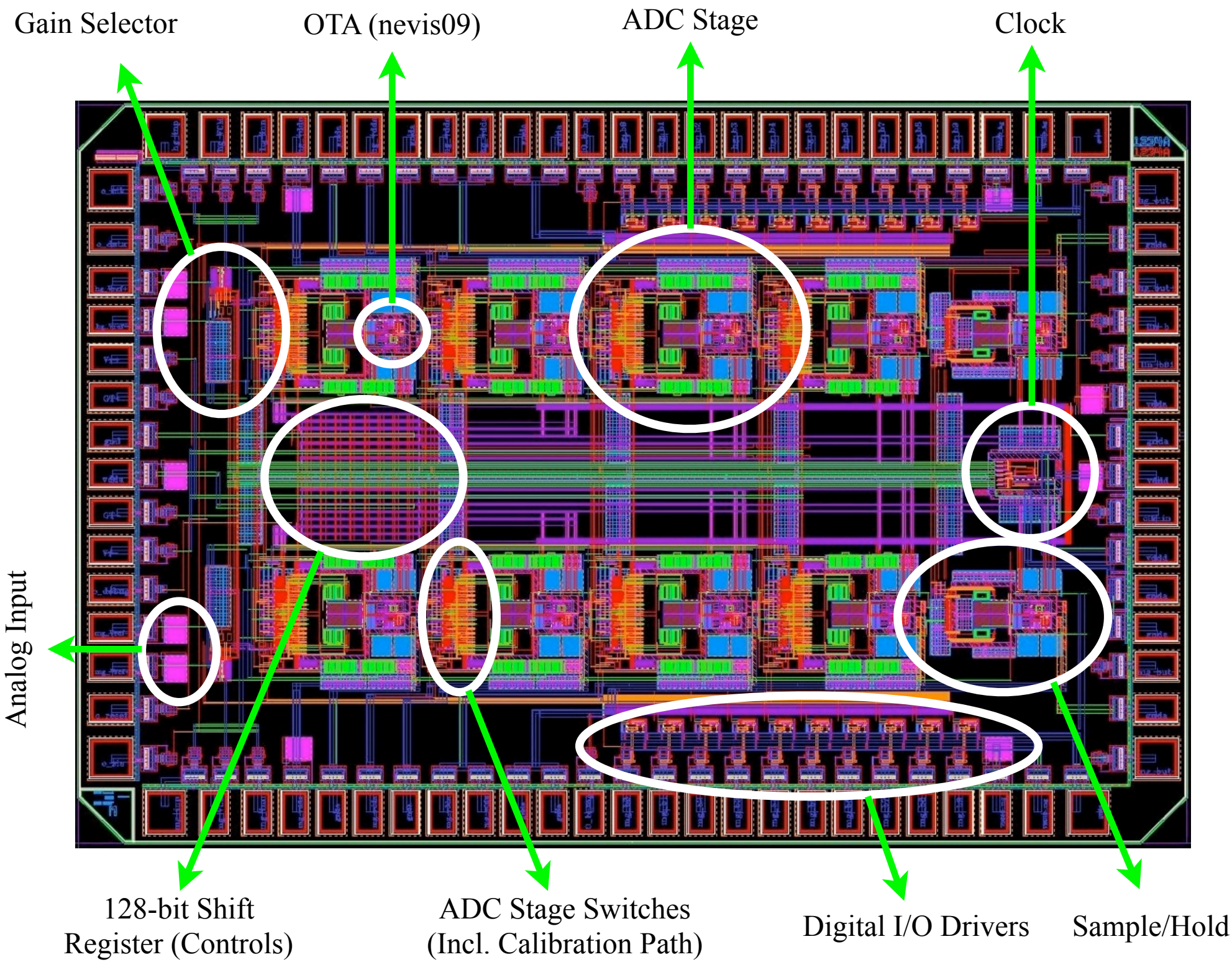
Nevis10 Chip

Submitted for fabrication in August

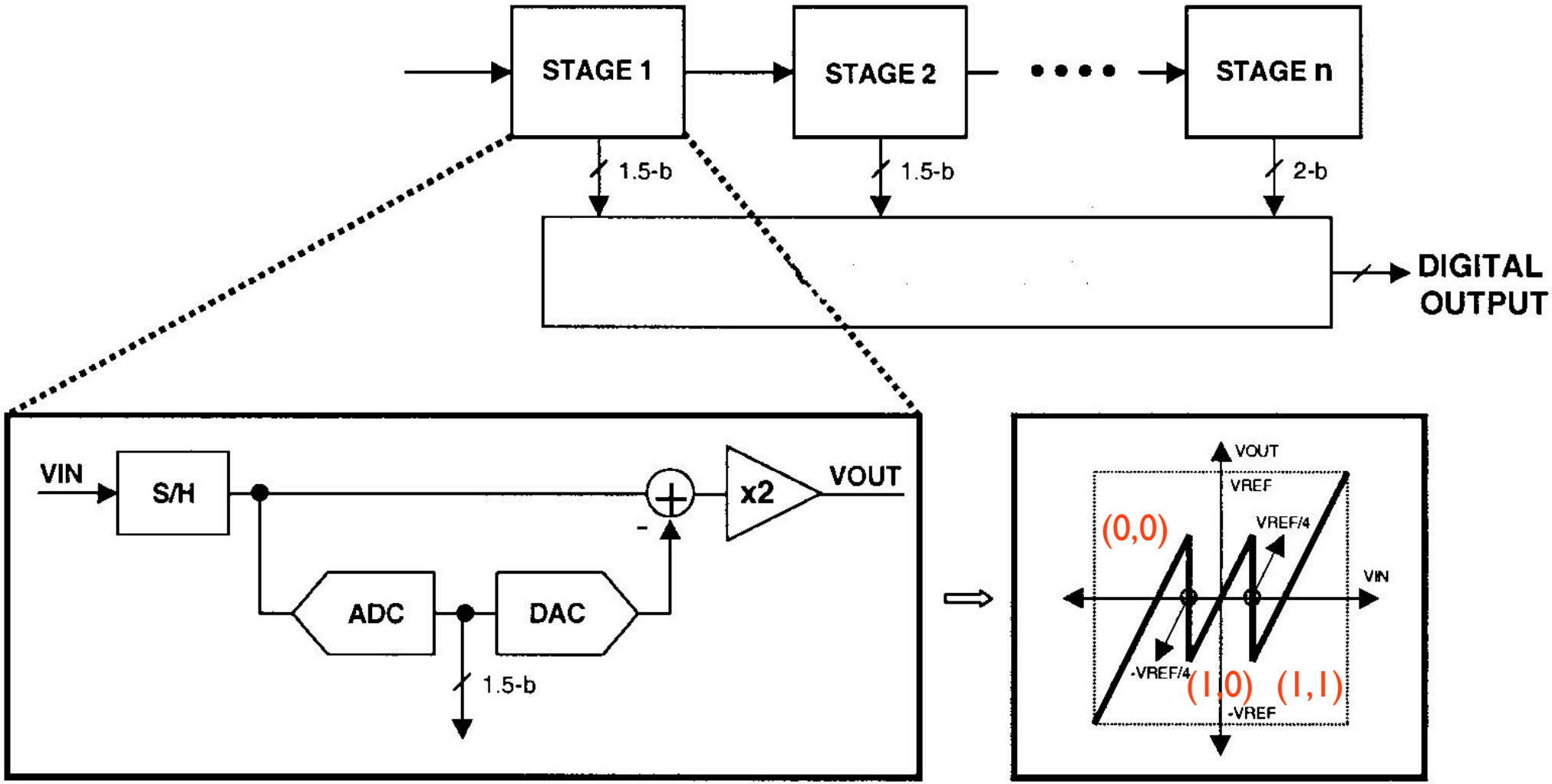
- First chip with true ADC functionality:
  - Two 4-stage ADC pipelines, 1.5 bits/stage (no size scaling)
  - Gain selector structures for each pipeline
  - S/H for analog residue, to be measured by external ADC
  - Support structures:
    - 128-bit control register to set ADC working mode
    - I/O drivers for digital signals
    - Clock unit, bias circuitry
- Implemented in IBM CMOS 8RF (130 nm), 2.5 V transistors, 2x3mm chip (dominated by pads)

Nevis10 Goals

- Demonstrate 12-bit precision
- Measure power consumption
- Verify calibration strategy
- Determine sensitivity to bias voltage
- Check cross-talk
- Verify radiation tolerance
- Test gain selection architectures
- Learn!

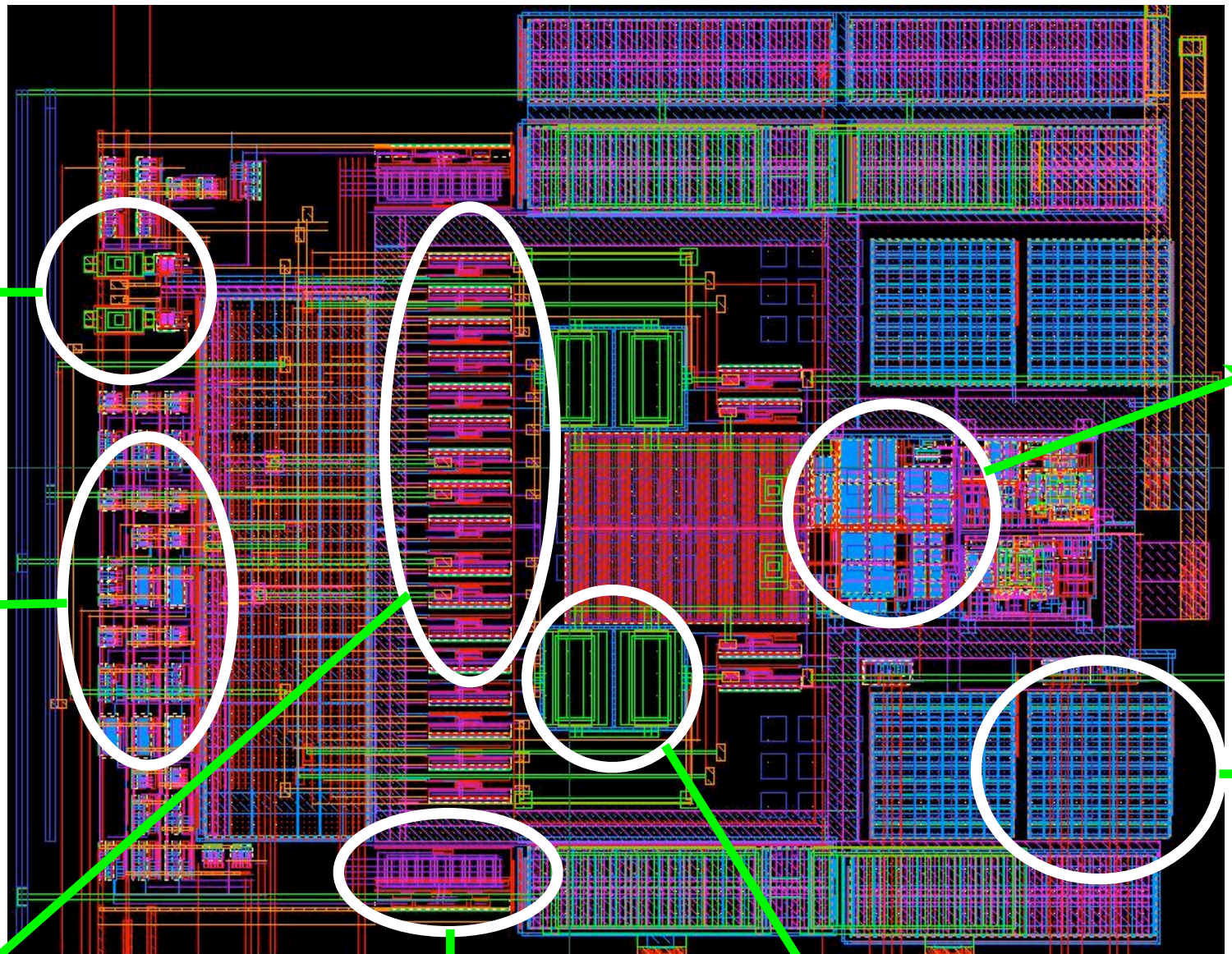

Gain Selector
OTA (nevis09)
ADC Stage
Clock
Analog Input
128-bit Shift Register (Controls)
ADC Stage Switches (Incl. Calibration Path)
Digital I/O Drivers
Sample/Hold

Principle of Operation



- Residue is multiplied ×2, i.e. 1 bit/stage
  - But measure 1.5 bits...

ADC Stage

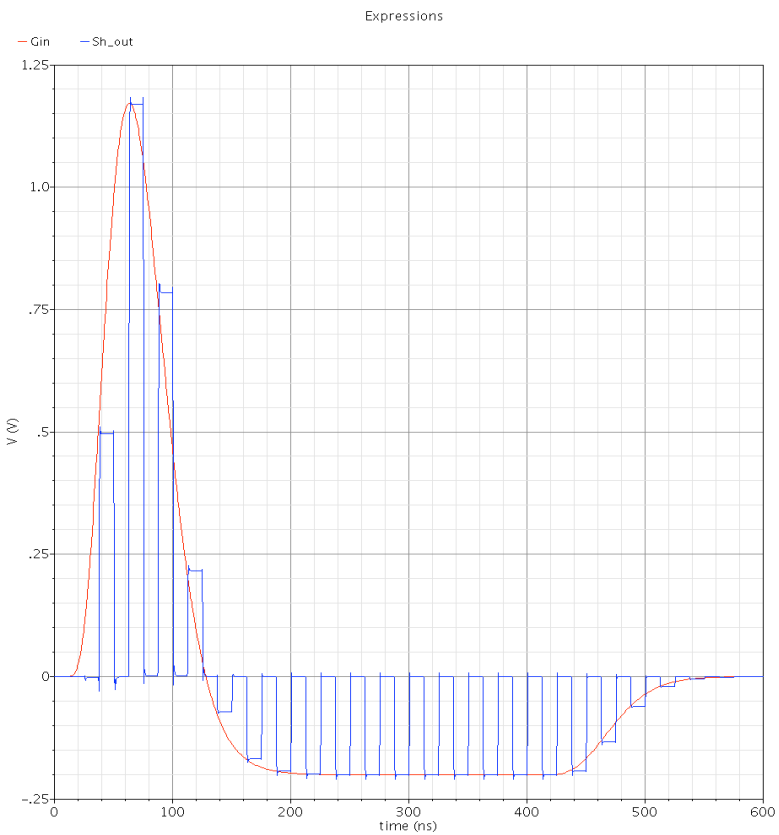

Presampler
Logic
Switches
Comparators
Sampling Caps
Filters
OTA
(Nevis09
chip)

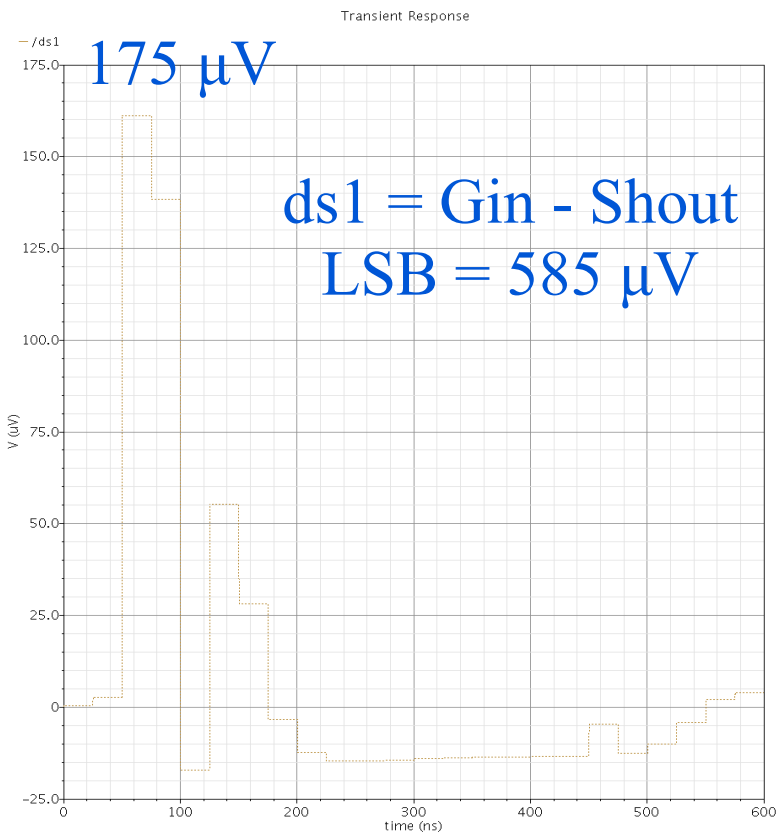
Digital Error Correction

- For each stage, two comparators, three possible codes
  - "1.5 bits"
  - Redundancy allows measurement of comparator offsets and gain calibration
- Inject signal close to comparator threshold, and force decision
  - Measure result of both possibilities using downstream ADC stages (previously calibrated) & compare
- Final output code based on calibration results
  - In nevis10 chip, just output everything

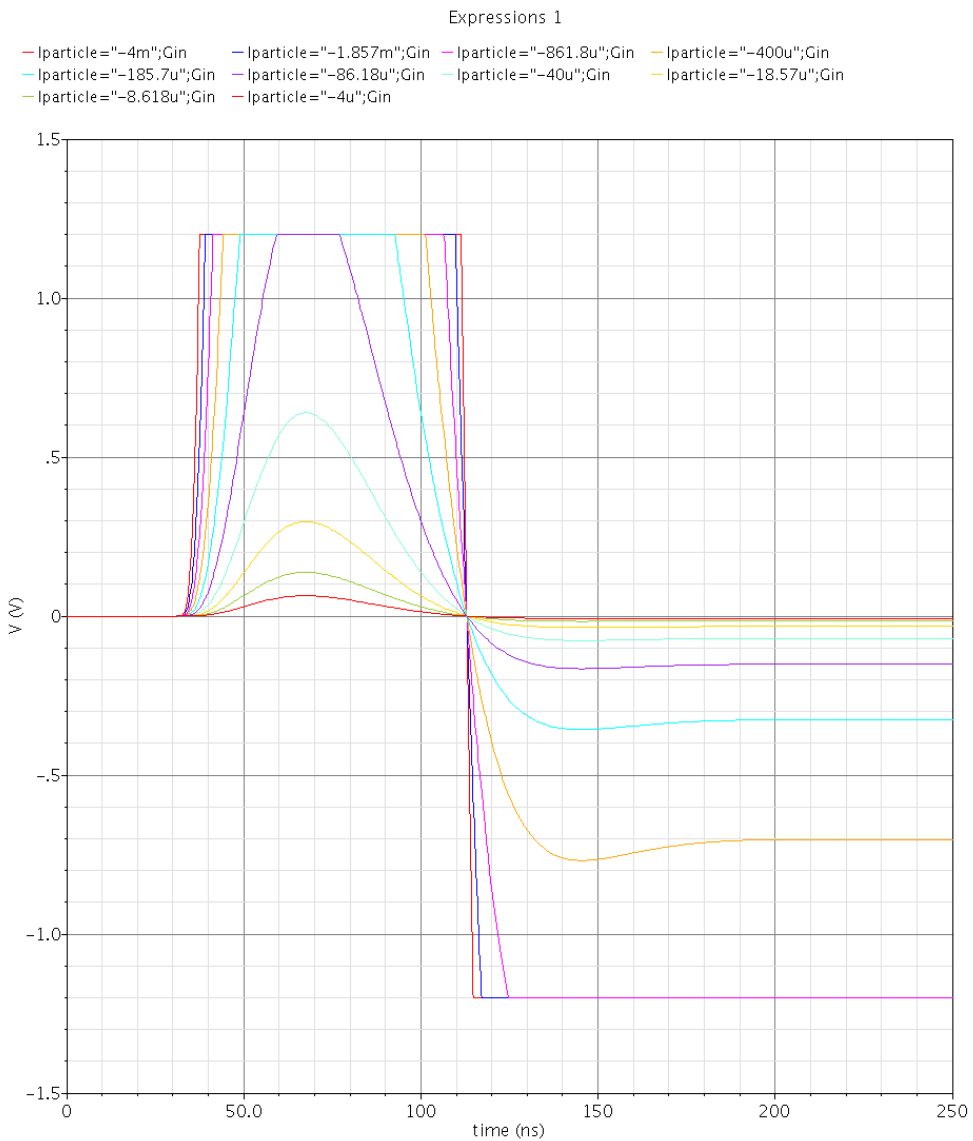
Gain Selection

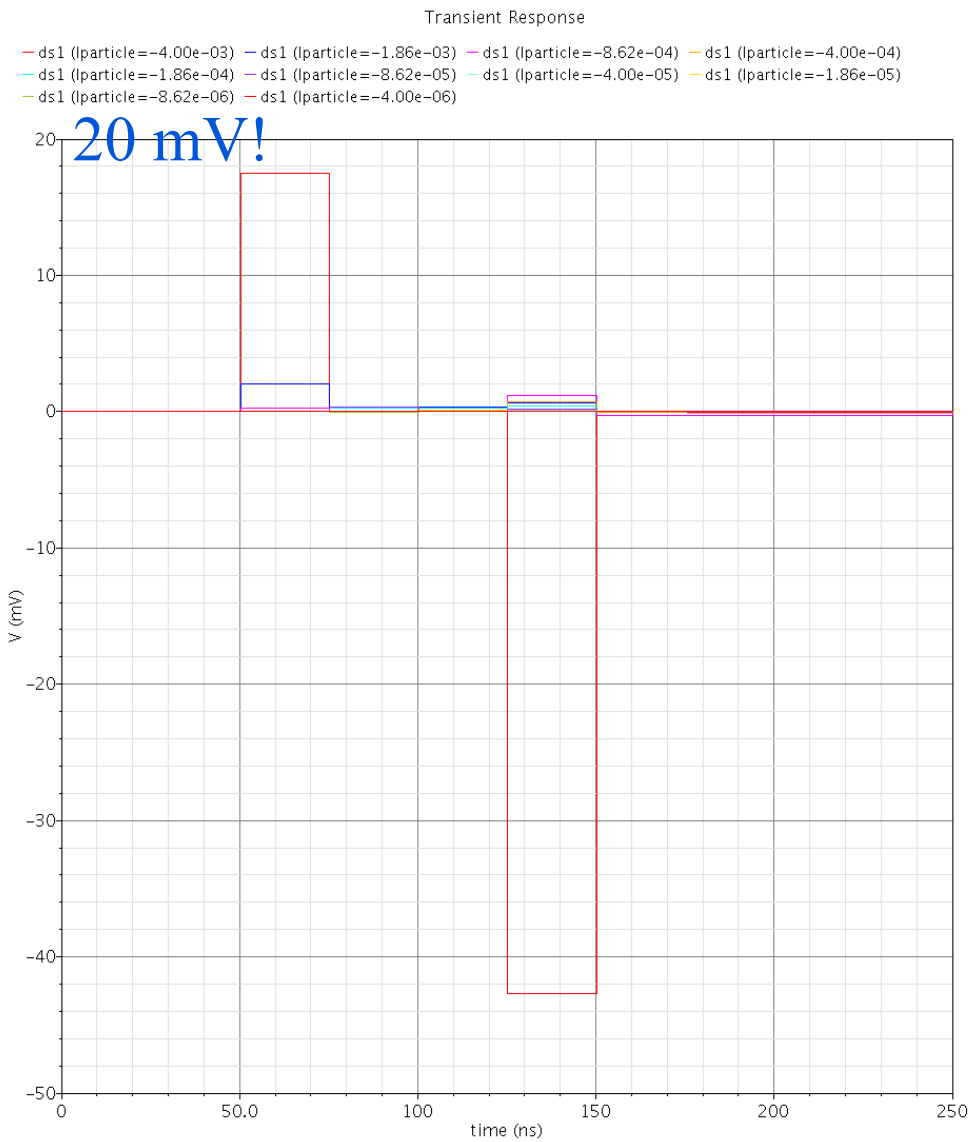
- Would like to do this in analog domain: save power!
- Can use same comparators as in ADC stages, do analog gain selection





- However, for large signals not enough bandwidth!

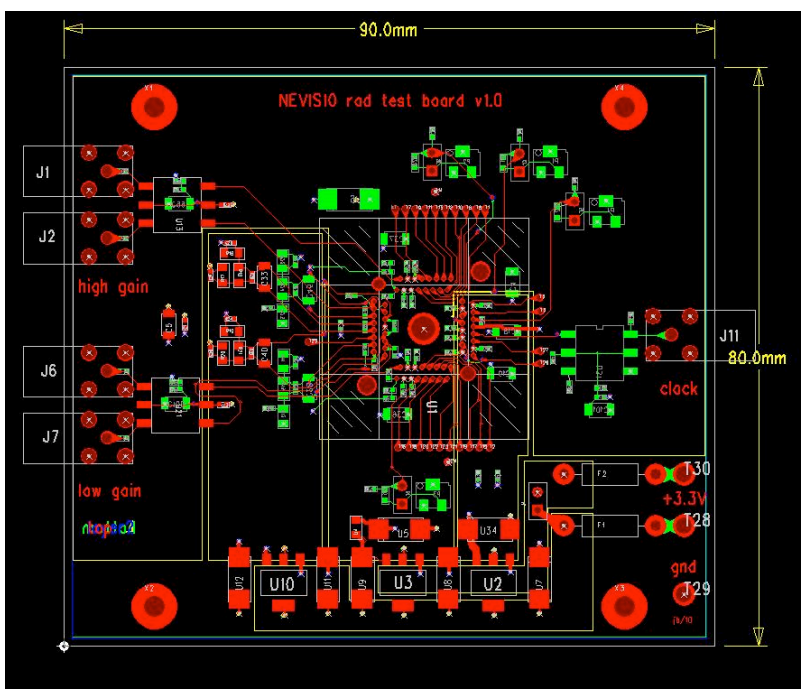


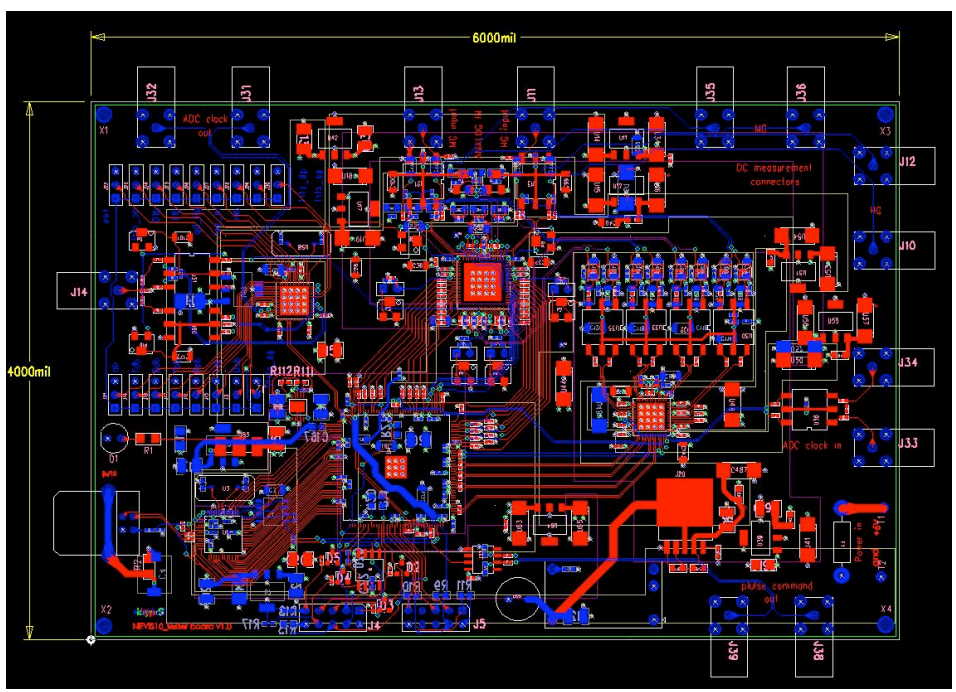


- Options:
  - Analog gain selection with simple thresholds, but remembering previous two samples
    - Go to lower gain if steep slope
  - Digitize all gains for first 2 (3?) stages, then choose
    - Requires multiplexing signal into "lower" part of ADC
  - Fully digital approach: digitize all gains all the way, then do digital gain selection
    - Based on the fact that lower ADC stages are smaller anyway, so very small cost in power & space (in Nevis10, no size scaling yet)
- All three options will be tested with Nevis10 chip

Nevis10 Testing

- Board with socket for basic functionality tests, incl. yield, and irradiations
- Board with FPGA and 4-channel 12-bit ADC for detailed testing
  - Boards are being manufactured





Conclusions & Next Steps

- Nevis10 chip designed to test all analog aspects of FEB2 ADC development
  - Precision, gain selection, calibration, etc.
- Future:
  - Reference voltage circuitry
  - Calibration circuitry/engine
  - Gain selector
  - Output serializer
- Next chip possibly first full prototype (2012?)