RPC
Electrical System
Review
Cern 18 September 2000

This documentation can be found at:
http://pccms5.ba.infn.it:90


We would like to acknowledge the technical staff:
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Overview

ESR RPC Documentation
CERN 18 September 2000

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Chapter 2. VLSI Design
Chapter 3. Front-End Board
Chapter 4. RPC services

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• **Overview, VLSI Design and Front End Board:** F. Loddo

• **Irradiation Tests:** P. Vitulo

• **RPC services:** A. Ranieri
Developments on the RPC system: electronics & services
One barrel sector …………………60 sectors

- RB4 …… 120 chambers
- RB3 …… 120 chambers
- RB2 …… 120 chambers
- RB1 …… 120 chambers

Total number of FE Channels:
180 x 192 = 34,560 (RB1_i, RB1_e, RB2_e)
60 x 288 = 17,280 (RB2_i)
240 x 96 = 23,040 (RB3, RB4)
--------------------------
Total = 74,880/16 Ch. = 4,680 FE board x 1.2 (+ spare) ≈ 5,600 FE board
Shape of the signal

\[ I(t) = I_0 \exp(t/\tau) \quad (0 \leq t \leq 15 \text{ ns}) \]

\[ \tau \sim 1 \text{ ns is the gas time constant} \]

Strip line (Barrel) 1.3 m long and 2 - 4 cm wide: 15 \( \Omega \) \( \leq \) \( R_0 \) \( \leq \) 25 \( \Omega \)
Strip line (Endcap) 0.7 m long and 0.7 - 1.5 cm wide: \( R_0 \sim 40 \Omega \)

160 pF \( \leq C_{\text{strip}} \leq 350 \text{ pF} \)

Input dynamic range for RPC in avalanche operation 20 fC \( \leq \) \( Q_{\text{in}} \) \( < \) 10 pC
Streamer probability \( < \) 5 \%
Expected rate \( < \) 400 kHz/strip

Overview: Design constraints
Strip termination

Rise time (1 ns) is shorter than propagation delay: the strip behaves like a transmission line and must be properly terminated at both ends

- Reflected charge is lost (higher effective threshold)
- Reflected signals increase the strip occupancy

Which termination?

- active termination on the Front End side
- passive termination on the far end

Timing

Accurate timing information from the RPC is crucial for unambiguous assignment of the event to the related bunch crossing
After-pulse

- The avalanche pulse is often followed by an after-pulse with a delay 
  \[ 0 \leq \delta t \leq 100 \text{ ns} \text{ (or more)} \]
- The after-pulse must be masked in order to prevent wrong triggering

**A One-shot must follow the discriminator**

Choice of pulse length as compromise between possible second trigger and dead time (< 4%)

Dead time

- The maximum expected rate in CMS: 400 kHz per strip (T = 2.5 µs)
- Maximum dead time: 4% (T = 100 ns)
Barrel RPCs: 11 different strip geometries (see “Study of detailed Geometry of Barrel RPC strips” CMS Note 2000/xxx) with different strip impedance

Endcap RPCs: xx different strip geometries with different strip impedance

Advantages:

• The same, minimum sized FEBs for the barrel (and the endcap)
• The impedance matching will be done on the kapton with
  • strip impedance control
  • if necessary, termination resistor
• Compensation of the delays
• Easy to be soldered
## Overview: Radiation Environment

<table>
<thead>
<tr>
<th>Component</th>
<th>Total</th>
<th>Neutron $\Phi$</th>
<th>Ch. Had. $\Phi$</th>
<th>Max. TID</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>E&gt;100keV</td>
<td>2-20MeV</td>
<td>E&gt;20MeV</td>
</tr>
<tr>
<td><strong>HCAL:</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Barrel FEE box</td>
<td>$3.1 \times 10^{11}$</td>
<td>$1.3 \times 10^{11}$</td>
<td>$4.3 \times 10^{10}$</td>
<td>$2.4 \times 10^{10}$</td>
</tr>
<tr>
<td>Endcap FEE box</td>
<td>$6.5 \times 10^{10}$</td>
<td>$2.8 \times 10^{10}$</td>
<td>$5.2 \times 10^{9}$</td>
<td>$2.8 \times 10^{9}$</td>
</tr>
<tr>
<td><strong>Muon chambers:</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Barrel MB1</td>
<td>$2.3 \times 10^{10}$</td>
<td>$6.4 \times 10^{9}$</td>
<td>$8.0 \times 10^{8}$</td>
<td>$1.2 \times 10^{9}$</td>
</tr>
<tr>
<td>MB1, Z=0-400</td>
<td></td>
<td>$2.9 \times 10^{9}$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MB1, Z=400-660</td>
<td></td>
<td>$1.1 \times 10^{10}$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Barrel MB4</td>
<td>$2.9 \times 10^{10}$</td>
<td>$6.3 \times 10^{9}$</td>
<td>$1.0 \times 10^{9}$</td>
<td>$3.4 \times 10^{8}$</td>
</tr>
<tr>
<td>Endcap ME1/1</td>
<td>$8.7 \times 10^{11}$</td>
<td>$2.2 \times 10^{11}$</td>
<td>$3.6 \times 10^{10}$</td>
<td>$5.4 \times 10^{10}$</td>
</tr>
<tr>
<td>ME1/1, R=100-150</td>
<td></td>
<td>$6.2 \times 10^{11}$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>ME1/1, R=170-270</td>
<td></td>
<td>$1.1 \times 10^{11}$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Endcap ME1/2</td>
<td>$3.0 \times 10^{10}$</td>
<td>$5.6 \times 10^{9}$</td>
<td>$6.9 \times 10^{8}$</td>
<td>$7.3 \times 10^{8}$</td>
</tr>
<tr>
<td>Endcap ME1/3</td>
<td>$1.2 \times 10^{10}$</td>
<td>$2.3 \times 10^{9}$</td>
<td>$3.4 \times 10^{8}$</td>
<td>$1.7 \times 10^{8}$</td>
</tr>
<tr>
<td>Endcap ME2/1</td>
<td>$2.2 \times 10^{11}$</td>
<td>$6.0 \times 10^{10}$</td>
<td>$9.8 \times 10^{9}$</td>
<td>$1.7 \times 10^{10}$</td>
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• Front End Chip Specifications
• Tools for automatic tests
• Test of low volume production

• Front End Board Layout
• Board components
• Latch-up protection
• Slow control interface
• Kapton design
• Irradiation test
• Production plans
RPC Electronics
Front-End specifications
Technology: 0.8 \( \mu \)m BiCMOS of AMS
8 channels
Power supplies: +5 V; GND
Power consumption: ~ 50 mW/channel

Dimensions: 2.9 mm X 2.6 mm
64 I/O pads
Package: PQFP 80
It must preserve the fast slope of the input signal for fast timing

- **Current-sensitive preamplifier**: low input impedance for matching at the signal frequency (~ 100 MHz)

- **Dummy preamplifier**: required to balance the DC output variations of preamplifier

- **Gain stage**: non linear amplifier for dynamic compression

- **Power consumption**: ~ 15 mW

- **ENC (strip connected and terminated)**: < 2 fC
• Common emitter transimpedance stage

• Low input impedance: $R_{in} \sim 15 \Omega$

• Preserve the shape of input signal

• Bandwidth: 116 MHz

• $I_{in} = 700 \mu A$

• $g_m \sim 25 \text{ mA/V}$

• $R_{feed} \sim 1 \text{ K\Omega}$

• $C_{feed} \sim 1 \text{ pF}$

• Charge sensitivity: 0.5 mV/fC
Input impedance vs. frequency

Typical preamplifier response
\(Q_{in} = 20 \text{ fC}\)
• Dynamic compression: “peaked pulse” in the dynamic range
• Two-step piecewise-linear function fitting:
  sum of the output currents of 2 gain segments

\[ V_{\text{gain1}} = 7 \quad (Q_{\text{in}} < 200 \text{ fC}) \]
\[ V_{\text{gain2}} = 0.25 \quad (Q_{\text{in}} > 200 \text{ fC}) \]

• Charge sensitivity (Preamp-Gain Stage) \sim 2 \text{ mV/fC} \quad (up to 80 \text{ fC})
• Bandwidth: 90 MHz
Transfer characteristics of Preamplifier+ Gain Stage

Gain stage output

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Accurate timing information from the RPC is crucial for **unambiguous assignment** of the event to the related bunch crossing.

1. **Leading-edge triggering**: simple, but **amplitude and rise time dependent**
   In the case of RPC signals, with a 1000:1 dynamic range (20 fC to 10 pC), the time walk is ~ 10 ns

2. **Zero-crossing triggering**: a good approximation of **amplitude-independent timing response**
   - C-R differentiation of the input signal produces a bipolar pulse crossing the zero in correspondence of the peak of the input signal
   - If input signals have same peaking time, the zero-crossing time is independent of signal amplitude and can be used as time reference
   - Easy integration into ICs
Zero-Crossing Discriminator

• Threshold Discriminator (Charge selection)
• Zero-Crossing Discriminator (Time reference)
• One-shot
• Coincidence gate

- Threshold range: $5 \text{ fC} < Q_{th} < 500 \text{ fC}$
- Threshold uniformity: 1.5 fC rms
- Shaped Arming pulse width: 20 ns
- Power: 8 mW
Discriminator Response in the dynamic range: simulation results

$Q_{th} = 20 \text{ fC}$ \hspace{1cm} $1 \text{ fC} < Q_{ov} < 10 \text{ pC}$

**One-Shot response**

- $\Delta T \sim 10 \text{ ns}$

**Zero-crossing Discriminator response**

- $\Delta t < 1 \text{ ns}$

**Discriminator Response in the dynamic range:**

- Simulation results

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\[ \tau (V_{\text{mon}} = 5 \, \text{V}) = R_{\text{mon}} C_{\text{mon}} \sim 300 \, \text{ns} \]
\[ \tau (V_{\text{mon}} = 0 \, \text{V}) = R_{\text{ds}} C_{\text{mon}} \sim 15 \, \text{ns} \]

\{ 50 \, \text{ns} < T_w < 250 \, \text{ns} \}

Diodes are for fast recovery: \( T_{\text{dead}} = 10 \, \text{ns} \)

Power consumption = 2 mW
- 100 \Omega \text{ twisted pair cable}
- LVDS receiver, 250 mV minimum signal
- Typical power consumption: \(~18\text{ mW}
- Tuneable output current to compensate process variations

**Output Driver**

**measure**
- OFF Cursors
- Parameters
- node
- Std Voltage
- Std Time
- Custom
- Pass
- Fail

**Statistics**
- OFF

**On Time**
- 340

**From**
- 0.000 div
- Track 180

**To**
- 10,000 div
- 650 pts

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**Double Pulse Resolution: simulation results**

\[ Q_{th} = 20 \text{ fC}, \quad T_w = 50 \text{ ns} \]

Dead time (typical case) \(~ 70 \text{ ns}\)

Dead time (worst case) \(~ 100 \text{ ns}\)

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\[ Q_{in} = 2 \text{ pC}, \ T_w = 50 \text{ ns}, \ f_{in} = 14 \text{ MHz} \]
Typical timing response vs. Charge Overdrive

$Q_{th} = 30$ fC

<Time (ns) [Arbitrary zero]

$Q_{ov}$ (fC)

Typical timing response vs. Charge Overdrive

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RPC Electronics
Tools for automatic test
The Front-End CHIP Testing system

Chip characterization
- Threshold uniformity
- Find $V_{gain}$
- Measure propagation time
- Measure dispersion among 8 channels
- Store informations

Chip acceptance
- Threshold dispersion < ± 5 fC
- Time dispersion < 0.5 ns

PC
- Interface boards (PCI BUS)

GPIB

PULSE GEN.

TRIGGER AND SIGNAL

ANALOG AND DIGITAL I/O

FEC/FEB TESTING BENCH

SCOPE

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- PC : Pentium 350 MHz, Win95/NT
- Software : developed with LabView 5.0.1
- Interface boards : I/O Analog/Digital National Instr. 6024E Multifunction Board
- Pulse generator : LeCroy 9210
- Scope : LeCroy 9374
- Testing bench : FEC or FEB
The Front-End CHIP Testing system

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The front-end chip test bench
The front-end chip test bench
RPC Electronics
Test of low volume production
Test of low volume production (1000 chips)

AVERAGE DELAY TIME
\( Q = 1 \text{ pC} ; T = 22^\circ \text{C} \)

IN-CHIP DELAY DISPERSION
\( Q = 1 \text{ pC} \ T = 22^\circ \text{C} \)
CHIP DELAY TIME DISTRIBUTION
Q = 1 pC  T = 22 °C

Colour coded time distribution

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RPC FE board

• Front end board layout
• Board components
• Latch-up protection
• Kapton connectors design
• Slow control
• Irradiation tests
• Tests on massive production
• Time schedule
RPC Front-End board
Front-End board layout
RPC FE board & Service board architecture

From strip

8

FEC

DAC

FEC

ADC + Temperature Sensor

LVDS output + Test Input from LB (50 pins)

Service board

LV Cable

I2C Channel

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Dimensions: 230x105 mm²
16 channels (2 FE Chips)
4 Layers (1 for both AGround and DGround)
2 FPC connectors for RPC strip connection (through Kapton foils)
50 pin socket connector for flat cable → Link Board (outputs, test inputs)
20 pin socket connector for power & control flat cable (Power, I²C Lines)

AVP = 5V
DVP = 5V
I_a = 70 mA
I_d = 130 mA
Dimensions: 255x140 mm²
32 channels (4 FE Chips)
4 Layers (1 for both AGround and DGround)
4 FPC connectors for RPC strip connection (through Kapton foils)
Two 50 pin socket connector for flat cable → Link Board (outputs, test inputs)
20 pin socket connector for power & control flat cable (Power, I²C Lines)

AVP = 5V
DVP = 5V
I_a = 140 mA
I_d = 260 mA
RPC Front-End board
Front-End board components
One (Two in the Forward FEB) Voltage Output 10-Bit DAC with I\(^2\)C Interface (Analog Device AD5311 BRM) for threshold setting

- Resistor string DAC fabricated on CMOS process
- Reference derived from Power Supply (5V) → Resolution = 4.88 mV (~2.44 fC)
- Power-on reset function
- Max. Zero Code Error = 20 mV
- Power consumption = 0.75 mW

One 10-Bit ADC and Digital Temperature Sensor with I\(^2\)C Interface (Analog Device AD7417 AR) for threshold check and local Temperature monitoring

- On-chip Reference = 2.5V (± 25 mV max) → Resolution = 2.44 mV
- Offset Error = ± 4 LSB max
- T Measurement Error = ± 2 °C max
- T resolution = 1/4 °C /LSB
- Power consumption = 3 mW max
Two 400 mA Low-Dropout Voltage Regulator MICREL MIC29201-5.0 V

- Dropout (100 mA) = 250 mV
- Shutdown input
- Error flag
- Foldback current limiting ($I_{\text{limit}} = 425$ mA Typical)

One (Two in the FW) LVDS Quad CMOS Differential Line Receiver DS90C032

- Chip Test pulsing

Two-Three potentiometers/Chip to set (during the test procedure in the Company):

- $V_{\text{gain}} \approx 2.5$ V, according to automatic test results
- $0 < V_{\text{mon}} < 5$ V, to set ONCE the output pulse width between 50 ns and 250 ns
- $V_{\text{drive}} \approx 2.5$ V, to tune the driver current. Probably it is not necessary!!

One (Two in the FW) potentiometer to set (once) the start-up value of $V_{\text{Threshold}}$
RPC Front-End board
Latch-up protection
Polyswitch

• Error Flag warns of output dropout > 250 mV due to current limiting after few μs
• AC coupling with Shutdown input (after an inversion) switches off the MIC29201 for 100 ms
• Positive feedback through Q2 avoids oscillations of Error_Flag
• If the failure persists, Polyswitch intervenes

Current limit: 425 mA (Typ)
1 A (Max)
Latch-up protection and de-latching technique (II)

Induced short-circuit on VDD

Micrel disabled after 4.5 µs
RPC Front-End board
Slow control interface
Parameters to be controlled:

- Set Thresholds (10-bit word into the DAC)
- Check Thresholds (10-bit word from the ADC)
- Monitor Temperature (10-bit word from the ADC)

Interface (Barrel):

- I²C serial bus (2-wire)
- One Line will be provided by DT
- Clock rate: 100 kHz
- Communications with Control Room will be set-up by DT

Advantages:

- Easy to be used
- Many commercial chips with this interface
- Clock activity only during operations
RPC Front-End board
Kapton design
Barrel RPCs: 11 different strip geometries (see “Study of detailed Geometry of Barrel RPC strips” CMS Note 2000/xxx)

<table>
<thead>
<tr>
<th>Chamber</th>
<th>Pitch (mm)</th>
<th># strips</th>
<th>Kapton Type</th>
<th>Strip impedance (Ω)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>RB1_in</td>
<td>22.7</td>
<td>15</td>
<td>1</td>
</tr>
<tr>
<td>2</td>
<td>RB1_out</td>
<td>24.3</td>
<td>14</td>
<td>2</td>
</tr>
<tr>
<td>3</td>
<td>RB2_in</td>
<td>27.3</td>
<td>15</td>
<td>3</td>
</tr>
<tr>
<td>4</td>
<td>RB2_out</td>
<td>29.3</td>
<td>14</td>
<td>4</td>
</tr>
<tr>
<td>5</td>
<td>RB3</td>
<td>34.8</td>
<td>14</td>
<td>5</td>
</tr>
<tr>
<td>6</td>
<td>RB4/1-</td>
<td>40.8</td>
<td>16</td>
<td>6,7</td>
</tr>
<tr>
<td>7</td>
<td>RB4/1+</td>
<td>40.8</td>
<td>16</td>
<td>6,7</td>
</tr>
<tr>
<td>8</td>
<td>RB4/11</td>
<td>40.8</td>
<td>16</td>
<td>6,7</td>
</tr>
<tr>
<td>9</td>
<td>RB4/4--</td>
<td>40.6</td>
<td>12</td>
<td>8</td>
</tr>
<tr>
<td>10</td>
<td>RB4/4-</td>
<td>40.6</td>
<td>12</td>
<td>8</td>
</tr>
<tr>
<td>11</td>
<td>RB4/10</td>
<td>41.0</td>
<td>12</td>
<td>9</td>
</tr>
</tbody>
</table>

Barrel RPCs: 9 different Kapton Shapes

<table>
<thead>
<tr>
<th>Chamber</th>
<th>Base (mm)</th>
<th>Height (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>RB1_in</td>
<td>321.95</td>
</tr>
<tr>
<td>2</td>
<td>RB1_out</td>
<td>324.10</td>
</tr>
<tr>
<td>3</td>
<td>RB2_in</td>
<td>398.20</td>
</tr>
<tr>
<td>4</td>
<td>RB2_out</td>
<td>395.00</td>
</tr>
<tr>
<td>5</td>
<td>RB3</td>
<td>471.60</td>
</tr>
<tr>
<td>6</td>
<td>RB4_1X_L</td>
<td>312.72</td>
</tr>
<tr>
<td>7</td>
<td>RB4_1X_R</td>
<td>312.70</td>
</tr>
<tr>
<td>8</td>
<td>RB4/4</td>
<td>472.62</td>
</tr>
<tr>
<td>9</td>
<td>RB4/10</td>
<td>477.98</td>
</tr>
</tbody>
</table>
• Strip width $> 350 \, \mu m$

• Strip width depends on RPC strip impedance to be matched

• Strips have EXACTLY same lengths $\Rightarrow$ No skew

• In the Barrel, only in RB1_in and RB1_out: 10 $\Omega$ SMD Resistor in series to improve impedance matching (Amplifier input impedance $\approx 15 \, \Omega$)
KAPTON Example 1: RB1_in

SMD Resistors
10 Ω

Stiffener to improve mechanical stability (0.3 ± 0.05 mm)

Ground connections
KAPTON Example 2: RB4_1X

Left

Right

RPC-ESR CERN September 2000
The tests of the FEBs will consist of:

• In-Circuit test
• Functional test
• Check of timing performance
• Burn-in
RPC Front End irradiation tests

• Bari $\gamma$ irradiation tests (~ 1 Gy)
• Cern (Gamma Irradiation Facility) $\gamma$ irradiation tests (~ 20 Gy)
• Pavia (Lena Reactor) fast neutrons irradiation test (~ 1 Gy)
  (high $\gamma$ background: 440 keV - ~ 100 Gy)
• UCL (Louvain-la-Neuve) high energy n irradiation test ~ 70 Gy
  (low $\gamma$ background)
Two front-end boards have been irradiated with 11 mCi of $\gamma$ source ($^{60}$Co). The performance has been monitored after the exposition time to spot possibly aging effects.

**Bari irradiation tests**

- MCNP 4b code
  - source activity ($3.5 \times 10^8$ Bq) $\Rightarrow \gamma$ flux
  - $\phi = 1.5 \times 10^5 \, \gamma/cm^2s$
  - $D_{rate} = 1.5 \, \mu$Gy/s
  - $D_{tot} = 1.3 \, Gy$

- Board with FE chip (vetronite + Si)

- Concrete wall

- Collimator & $^{60}$Co source
- One RPC-RB2 like has been irradiated integrating a dose of ~20 Gy over several months.
- No sensible variations in performance was observed both in the FE alone and in the chamber.

20 Ci $^{137}$Cs source

$\gamma$ Beam

$\mu$ Beam

Estimated Flux

$\varphi = 1.9 \times 10^6 \pm 0.5\% \ (cm^2 s^{-1})$

ABS 1

$\varphi = 3.6 \times 10^5 \pm 1.2\% \ (cm^2 s^{-1})$

ABS 5

$\varphi = 2.9 \times 10^4 \pm 0.7\% \ (cm^2 s^{-1})$

ABS 100
Two FE boards were put in the Thermal Column of the Reactor just in front of a boral window (to deplete thermal component)
Neutron spectrum before and after the boral window

<table>
<thead>
<tr>
<th>Neutron Energy</th>
<th>$\Phi_n$ (n/cm$^2$ sec)</th>
<th>Total (n/cm$^2$ sec)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$E_n &lt; 0.4$ eV</td>
<td>$1.6 \times 10^3$</td>
<td></td>
</tr>
<tr>
<td>$0.4$ eV $&lt; E_n &lt; 10$ KeV</td>
<td>$3.4 \times 10^5$</td>
<td>$5.9 \times 10^5$</td>
</tr>
<tr>
<td>$10$ KeV $&lt; E_n &lt; 10$ MeV</td>
<td>$2.5 \times 10^5$</td>
<td></td>
</tr>
</tbody>
</table>
Each OR of 8 channels (1 chip) was counted (with open input) at Reactor ON and OFF to measure spurious neutron induced events (Single Event Upset)

Average CHIP SEU RATE

10 years LHC in the Muon Barrel

Φ ~ 6 x 10^5 cm^-2 s^-1

17.0 Hz
15.5 Hz
17.2 Hz
15.8 Hz
@ Φ ~ 2 x 10^9
Thermal (no γ)
15’ irradiation
~ 1.8 x 10^{12} cm^-2

We have directly measured the flux with activated Au/Ni targets (6x10^5 cm^-2 s^-1)
The accidental rate induced by Fast Neutrons (0.4 eV - 10 MeV) on each channel of the tested FE chips has been measured to be $2.5 \times 10^{-3}$ Hz ($\Phi \sim 6 \times 10^5 \text{ cm}^{-2} \text{ s}^{-1}$) and constant as a function of the fluence up to a value of about $1.6 \times 10^{11} \text{ cm}^{-2}$.
• Testing condition:
  – Neutrons (3 to 65 MeV) from p(65Mev) on a Be target
  – Max proton current (15 μA): yield 3.3x10^7 n/cm^2/s @ 2m on 25x25 cm^2
  – Neutron fluence of 10^{12} cm^{-2} equivalent to a proton charge of 367.647 μC
  – Neutron yield: 2.72x10^6 n/cm^2/s/μA

• Four beam periods:
  – 25 min @ 0.82 μA
  – 10 min @ 1.3 μA
  – 22 min @ 3.0 μA
  – 300 min @ 15.0 μA

• Integrated neutron flux: 1x10^{12} n/cm^2 (RE1/1 conditions)
UCL Irradiation Measurements: Test set up (I)

Collimator output

RPC Front-End boards
• Each OR of 8 channels (1 chip) was counted (with open input) at Cyclotron ON and OFF to measure spurious neutron induced events (Single Event Upset).

• Monitoring of the latch-up protection circuits to detect SEL events (by counting the error flag of the latch-up circuit)

• Monitoring (every 30 s) of the preset threshold voltage value to check SEU on DACs (by checking the DAC bits contents and its analog output)

• Monitoring of the local temperature value from ADCs to check right functioning

• DACs and ADCs monitoring by means of I²C circuit
Average Chip SEU rate

Neutron Fluence (x 10^10 cm^-2)

Average Chip Rate (Hz)

Φ ~ 5 x 10^7 cm^-2 s^-1

Chip 1
Chip 2
Chip 3
Chip 4
Average SEU cross section

\[ \sigma = \frac{N_{ev}}{\Phi \Delta t} \]

Pavia reactor results
(0.4 eV - 10 MeV)

Setting Up

Fast Neutron Fluence (x 10 \(^{10}\) cm\(^{-2}\))

Neutron fluence (x 10 \(^{10}\) cm\(^{-2}\))

Average SEU Cross Section
(Pavia Results)

Average SEU
\( (x 10^{-10} \text{ cm}^2) \)

Chip 1
Chip 2
Chip 3
Chip 4
• no SEL events detected
• no SEU on DACs
• right behaviour of ADC-T sensor
• front-end chip charge sensitivity unchanged
• no significative degradation of timing performance
The gamma irradiation tests made in Bari and at Cern have shown no degradations on the performance of both front-end chip and control electronics.

The accidental rate induced by Fast Neutrons (0.4 eV -10 MeV at Pavia reactor) on 32 channels of the RPC FE chip (AMS 0.8 μm BiCMOS) has been measured to be $2.5 \times 10^{-3}$ Hz/channel ($\Phi \sim 6 \times 10^5 \text{ cm}^{-2} \text{ s}^{-1}$) in average and constant as a function of the fluence up to a value of about $1.6 \times 10^{11} \text{ cm}^{-2}$ (> 10 years of LHC operation in the CMS barrel region).

Other measurements with more energetic neutrons (65 MeV at UCL-Belgium) have shown an accidental rate of about 0.2 Hz/channel ($\Phi \sim 5 \times 10^7 \text{ cm}^{-2} \text{ s}^{-1}$) as a function of the fluence up to a value of about $1.0 \times 10^{12} \text{ cm}^{-2}$ (> 10 years of LHC operation in the CMS muon end-cap region).

The results show a good behaviour of the developed front-end chip and the related control electronics in the expected CMS experimental conditions.
Irradiation test results are satisfactory

A pre-production of 1000 chips have been tested with the developed automatic test bench

The yield of the chip resulted to be better than 95%

Integration with detector have shown good results during the past test beams
Time schedule

- VLSI pre-production (1000 pieces): done
- Test of pre-production: done
- Gamma and Neutron irradiation tests: done
- Tender of VLSI: ready to start
- Tender of FE boards: ready to start
- Tender of Kapton: ready to start
RPC Services

• Requirements
• Cabling
• Power requirements
• HV & LV distribution
• Cooling distribution
• Gas distribution
• Parameters to be controlled
• Grounding scheme
• State of the art
One barrel sector ......................60 sectors

- RB4 ...... 120 chambers
- RB3 ...... 120 chambers
- RB2 ...... 120 chambers
- RB1 ...... 120 chambers

Total number of FE Channels:

- $180 \times 192 = 34,560$ (RB1i, RB1e, RB2e)
- $60 \times 288 = 17,280$ (RB2i)
- $240 \times 96 = 23,040$ (RB3, RB4)

--------------------------

Total = 74,880/16 Ch. = 4,680 FE board x 1.2 (+ spare) ≈ 5,600 FE board
Signals

Three types of connections are foreseen:

- Kapton connection between strips and Front End (at RPC level)
- Twisted flat 25 pairs cable between FEBs (at RPC level, ≤ 1.5 mt)
- On wheel connection between Front End Boards and Link Boards through round twisted 25 pairs, common shield and skewclear cable (< .5 ns/100 m and very low cost 2.3 CHF/m on 50 Km quantity)
Kapton Strip connection

- F-E board
- F-E board insulator support
- RPC higher gap
- Copper foil (ground)
- soldering points
- RPC lower gap
- KAPTON PC foil
- strip
Front-End Signal cables

Z axis

2455 mm

3000 mm/4000 mm (RB3, RB4)

12 twisted flat cables with 25 pairs conductors / 192 FE channels inside RPC

Kapton connecting strips to FE

12 round twisted pairs skewclear cables

78 round cables / sector
22542 mm² / sector (17x17 mm² / cable)

To Link Board around the detector
**FE board & Link Board connection**

**RPC Chamber**

<table>
<thead>
<tr>
<th></th>
<th>barrel</th>
<th>endcap</th>
<th>Total</th>
</tr>
</thead>
<tbody>
<tr>
<td>MLBs (fibre optical links)</td>
<td>300</td>
<td>432</td>
<td>732</td>
</tr>
<tr>
<td>SLBs</td>
<td>500</td>
<td>432</td>
<td>932</td>
</tr>
</tbody>
</table>

25 twisted pairs lines: 16 data lines plus 4 test input lines/FEB

Optical cable

LV & I2C connection
Barrel signal cable position (I)
Barrel signal cable position (II)
Cabling Cross Sections

- **Signal cable (on the detector):**
  - 17x17 mm²/cable = (289 mm²/cable)
  - (78 cables/sector) x 12 sectors = 936 cables /wheel ≈ 1,000 ⇒289,000 mm²/wheel
- **Signal cable (towards counting room):**
  - 6 optic fibers/sector x 4 mm² = 24 mm²/sector x 12 = 288 mm²
  - (6 optical fibers + 6 fibers TTC) = 288 x 2 = 576 mm² /wheel
- **HV cable (on the detector):**
  - 9 cables/sector x 12 = 108 cables/wheel
  - 17x17 mm²/cable = (289 mm²/cable)
  - 2,601 mm²/sector ⇒31,212 mm²/wheel
- **HV cable (towards counting room):**
  - 1 pair/floating channel ⇒4 mm² /floating channel
  - 4 mm² x 34 floating chan/sector = 136 mm²/sector ⇒1,632 mm²/wheel
  - LV for HV: 36 mm²/sector ⇒ 432 mm²/wheel (3 cable x 3 mm² = 9mm²)
- **LV cable (on the detector):**
  - 8 cables/sector x 12 = 96/wheel
  - 100 mm²/cable ⇒9,600 mm² /wheel
- **LV cable (towards counting room):**
  - same as before
The RPC electronics will consist of the 12 FE board/Chamber with a total of 192 channels. Total Front-end power consumption/Chamber considering analog plus digital is ~80 mW per channel (~15 W for the whole chamber).

**Analog absorption**

- 30 mA/FEC * 7V = 210 mW/FEC

**Digital absorption**

- 55 mA/FEC * 7V = 385 mW/FEC
- 595 mW * 2(FEC/FEB) * 78 FEB/sector = 92.8 W/sector
- 92.8 W * 60(sectors) = 5.6 kW/barrel
RPC Services
HV & LV distribution
HV and LV architecture for one barrel sector

26 LV channels/sector  34 HV channels/sector

RB4

96 channels  96 channels
4 LV Ch.

RB3

96 channels  96 channels
4 LV Ch.

RB2

96 channels + 96 channels + 96 channels
10 LV Ch.

RB1

96 channels + 96 channels
8 LV Ch.

1560 LV channel
2040 HV channel

LV analog
LV digital
8 HV Ch.
10 HV Ch.

LVA Channel
LVD Channel
HV Channel

RPC-ESR CERN September 2000
• **2040 HV channels**

  Maximum Rated Voltage = 12 kV  
  (Working Voltage = 9 kV)

  Maximum Rated Current = 0.5 mA/channel  
  (Working Current = 0.1 mA/channel)

  Maximum Power = 6W/channel  
  (Working Power = 0.9 W/channel)

  Maximum Power = 204 W/sector  
  (Working Power = 31 W/sector)

  Maximum Power = 2.5 kW/ring  
  (Working Power = 370 W/ring)

  Maximum Power = 12.5 kW/Barrel  
  (Working Power = 2 kW/Barrel)

• **1560 LV channels**

  **Analog**: Rated Voltage = 7 V  
  Working Cur. = 0.36 A/ ALV channel

  **Digital**: Rated Voltage = 7 V  
  Working Cur. = 0.66 A/ DLV channel

  Total power consumption/LV channel: 1.02 A * 7 V = 7.14 W

  Expected Power consumption = 92.8 W/sector 1.1 kW/ring 5.57 kW/Barrel
Architecture for HV & LV distribution

Main Frames (in Control room)
- SY1527
- (n PBHV + m PBLV)/sector

Remote Distribution Board (on the Balcony)
- HV or LV RDB

1 Barrel sector Detector
- RPC1
- 9 kV
- 7 V
- 9 kV

- RPC2
- 7 V
- 9 kV

- RPC3
- 7 V
- 9 kV

- RPC4
- 7 V

Number of RDBH: 16 HV Ch/RDBH (6U/8TE) ≤ 3 RDBH/sector ⇒ 180 RDBH / Barrel ⇒ 22 VME crate
Number of RDBL: (100W/sector) / (48W/RDBL) = 2 RDBL/sector ⇒ 120 RDBL / Barrel ⇒ 6 VME crate

RPC-ESR CERN September 2000
HV & LV: Power Supply System Crate

16 slots housing:
- High/Low Voltage boards
- Generic I/O boards (temperature, pressure monitors, ecc.)

Ethernet interface to control all parameters
CAENnet or CAN-Bus connectivity
Possibility to monitor/set:
- HV, including reading back actual individual voltages
- LV, same as HV
- Temperature sensors on detector
- Gas flux & composition
- Pressure (In/Out, once per sector & RPC gap)
• **2040** HV channels (one for each RPC gap) (number for barrel only)
• 12 kV, 500 μA supply per HV channel (request)
• Magnetic field in the detector region (2 kGauss)
• System components must be rad-hard tested (gamma and neutrons up to 10 MeV)
• Modularity
• **Local board:**
  – form factor: SY1527 board, 2 units wide
  – generation of a Power Medium Voltage
  – generation of a Service Low Voltage
  – management of the remote boards
  – each Local Board serves 2 Remote boards

• **Remote board:**
  – form factor: 6U x 8TE x ? (H x W x L)
  – two independent *floating* groups of 8 HV per board
RPC-ESR CERN September 2000

HV: System Layout (II)

COUNTING ROOM

SY1527 Board

COMM. LINK

POWER_MV
SERVICE_LV

Remote Board

GND1
HV1
HV2
HV8
GND2
HV8
HV1
HV2
HV8
GND1
GND2
HV8
HV1
HV2
HV8

DETECTOR
• The number of local and remote boards depends on the required power on the individual HV channels

• Constraints:
  – the SY1527 can provide totally 2.25 kW to the boards
  – each remote board can provide 16 HV channels
  – conversion efficiency (local and remote boards)
### HV: System Modularity (II)

<table>
<thead>
<tr>
<th>HV Channel Current (@ 12kV)</th>
<th>Power req'd for Single Channel</th>
<th>Corrected Power per HV Ch. (( \eta = 0.7 ))</th>
<th>Power req'd to drive 8 remote Ch</th>
<th>Total req'd Power (remote bd.)</th>
<th>Total n. local boards per SY1527</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 mA</td>
<td>12 W</td>
<td>17.15 W</td>
<td>10 W</td>
<td>294.4 W</td>
<td>3.8</td>
</tr>
<tr>
<td>500 ( \mu \text{A} )</td>
<td>6 W</td>
<td>8.75 W</td>
<td>10 W</td>
<td>160 W</td>
<td>7</td>
</tr>
<tr>
<td>440 ( \mu \text{A} )</td>
<td>5.3 W</td>
<td>7.6 W</td>
<td>10 W</td>
<td>141.6 W</td>
<td>8</td>
</tr>
</tbody>
</table>
• **2040** (1560) HV (LV) channels
  ⇒ **128** (98) Remote Boards;
  assuming 8 boards per crate:
  ⇒ **16** (13) Remote Crates (passive)

• **128** (98) Remote Boards ⇒ **64** (49) Local Boards (system crate in control room)
  ⇒ **8** (7) Local Crates (SY1527)
Suitable to sustain up to 15 kV

Cable characteristics:

- According CERN safety instruction IS 23
- Single conductor-\( \varnothing = 0.16 \text{ mm} \)
- Conductor resistance @ 20\(^\circ\)C = 147 \(\Omega/\text{Km}\)
- Core-\( \varnothing = 3 \text{ mm} \)
- Screen wire-\( \varnothing = 0.2 \text{ mm} \) (for 10 conductors)
- Overall diameter = 16.6 mm (for 12 conductors)
- Price: 4,370 DM/Km (for 10 conductors)

9 (8+1) cavi HV/sector \(\Rightarrow\) 2601 mm\(^2\)/sector
A 52 poles HV connector from RADIALL, is under evaluation by CERN to sustain 15 kV as RPC HV connector

- 8 high voltage conductors to supply four –12 kV values and the related ground connection
- 2 conductors for interlock function
- 1 conductor for shielding
The LV connector should have at least 19 contact pins to include:

- **RB1in/out, RB2in, RB3, RB4 case**
  - 8 LV conductors to supply four +7V values and the related ground connections
  - 8 conductors for sensing (4 conductors for each FEB row: one couple for digital and one couple for analog)
  - 2 conductors for interlock
  - One conductor for shielding

- **RB2out case**
  - Use 2 connectors of the same type as before
- one 9 pins DB connector to support I2C signal for slow control connection

**Used to connect LV cable**

**Used to connect I2C cable**

**For slow control**
Barrel LV/I²C connection scheme

Cooling bar  Flat connector

Front End board

LV/I²C flat cable

Metal box containing the service board
- Distributes LV to one chamber
- Provides I²C signals to two chambers
- Conceptual design ready (PCB under development)
RPC Services
Cooling distribution
RPC Cooling system (present design)

- hollow “L” shaped profile to cool and to support FE Board
- round cavity for water circulation
- Water flow
- FE Board
- strip
- RPC lower gap
- RPC higher gap
- RPC higher gap
- RPC lower gap
Water will be flowed into the pipe to maintain the temperature inside the electronic box at a constant and allowed value around 17°C.

- 100W/sector

- Cooling in common with DT cooling
RPC Services
Gas distribution
### Service type
- **Cooling pipe**: 6
- **Gas pipe**: 6

### Right side services
- **Water**
- **Gas in**
- **HV cables**
RPC Services
Parameters to be controlled
• **Monitor/Set:**
  – HV, including reading back actual individual voltages
  – LV (same as HV)
  – Temperature sensors on electronics
  – Analog threshold settings, including reading back actual values
  – Dead analog channels (monitor with/without test patterns)

• **Calibrate:**
  – HV value and current absorption vs. HV (rate dependent)
• **Threshold values** (one value/6 boards) \(\Rightarrow 780\) digital words

• **Temperature values** (2/RPC layer)(monitoring) \(\Rightarrow 780\) digital words

• **LV** (26 Ch./sector) (monitoring + set) \(\Rightarrow 1560\) values

• **HV** (34 Ch./sector) U & I (1/ RPC gap) \(\Rightarrow 2040 \times 2\) values

• 16 HV floating Ch./RDB (monitoring + set)

• **RDB** dimensions: 6U, 8TE (4cm width = two VME slots)

• 8 RDB/crate \(\Rightarrow 128\) HV floating Ch/crate
RPC Grounding Scheme (Preliminary)

1) Common Signal Ground
2) Shield Ground
3) Connection between Grounds (to be studied)
• Things already done

HV System crate available (SY1527)
Construction of a prototype of HV/LV Board with floating grounds for SY1527 (delivering in September)
Test of first prototype of Radiall connector (we are waiting for second one)
Signal cable Skewclear type: chosen

Things still to do

- Construction of 1’st prototype of HV Remote Distribution Board
- Test and validation of grounding scheme
- Test and validation of cooling system on a few chambers (tower of 10)
- Construction of the electronics service board