Calorimeter Digitizer Electronics

Cheng-Yi Chi

Columbia University

Off-Detector Calorimeter Digitizer electronics

- Function
- Past experience
- System block diagram
- ADC board block diagram, differential receivers, ADC choice. Comments on trigger primitives
- Progress on the Prototype
  - Some measurement results
- Production Flow
- System cost
- Status/Outlook

Calorimeter Digitizer electronics function

- Digitizing the signal after the on-detector electronics with single scale 14 bit ADC.
  - Try to maintain the best dynamic range as good we can do with single scale ADC. We are looking for 12 bits dynamic range.
- Interface with SPHENIX DAQ system
  - Receive beam clock, L0 timing and L1 trigger.
  - Provide 40 beam crossing L1 delay.
  - Provide the 4 L1 trigger events buffer.
  - Provide the functionality to generate L1 trigger primitives.

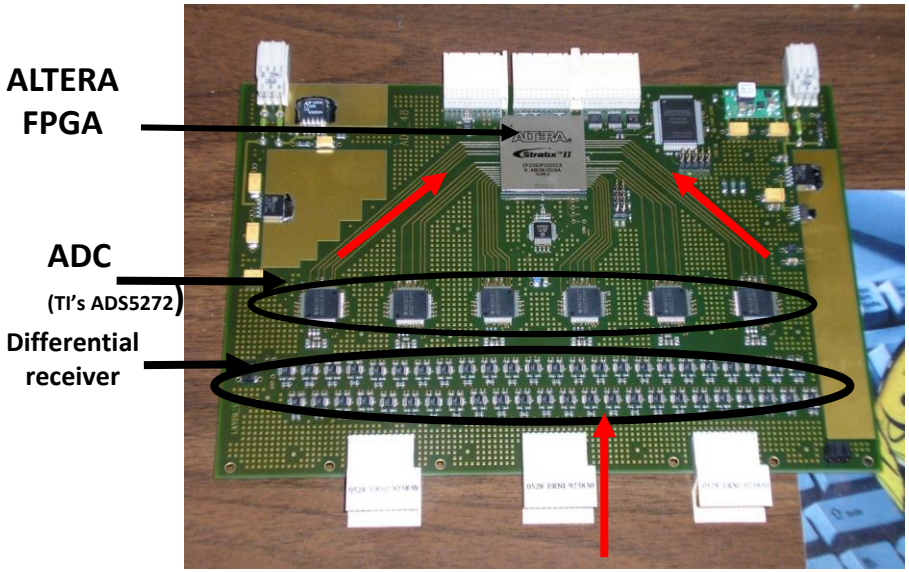
Past Experience

Built

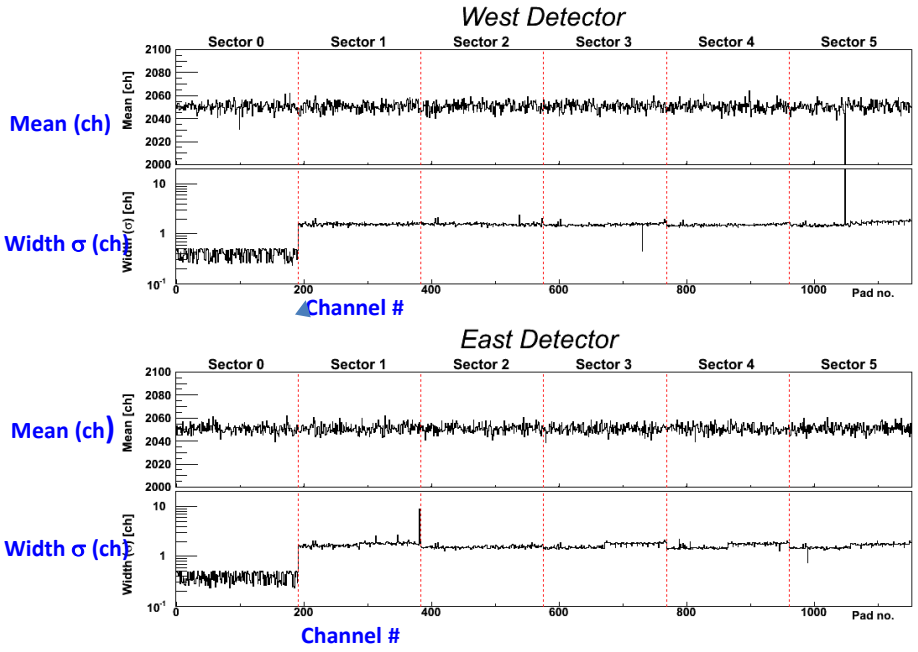
PHENIX Hadron Blind Detector (HBD) off-detector digitizer (12 bits, ~60 MHz)
also been use for the MPC readout electronics and SPHENIX test beam readout

MicroBoone TPC readout (BNL+Nevis) and PMT readout (similar shaper+ADC like HBD, 64 MHz)

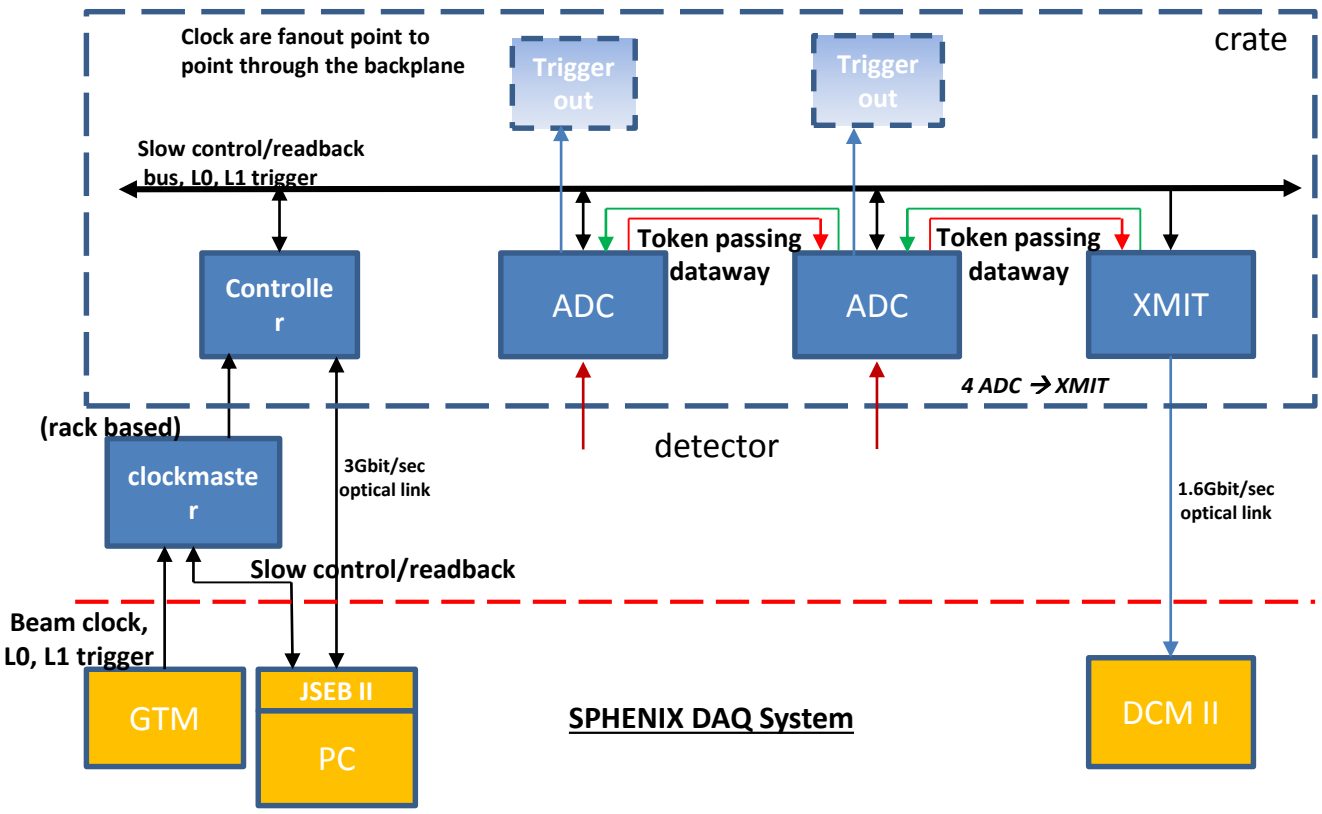
HBD ADC module



HBD Pedestal Run



ADC System Block Diagram



Crate based system.

Signals are cable from the on-detector electronics.

Digitized with 14 bit ADC.

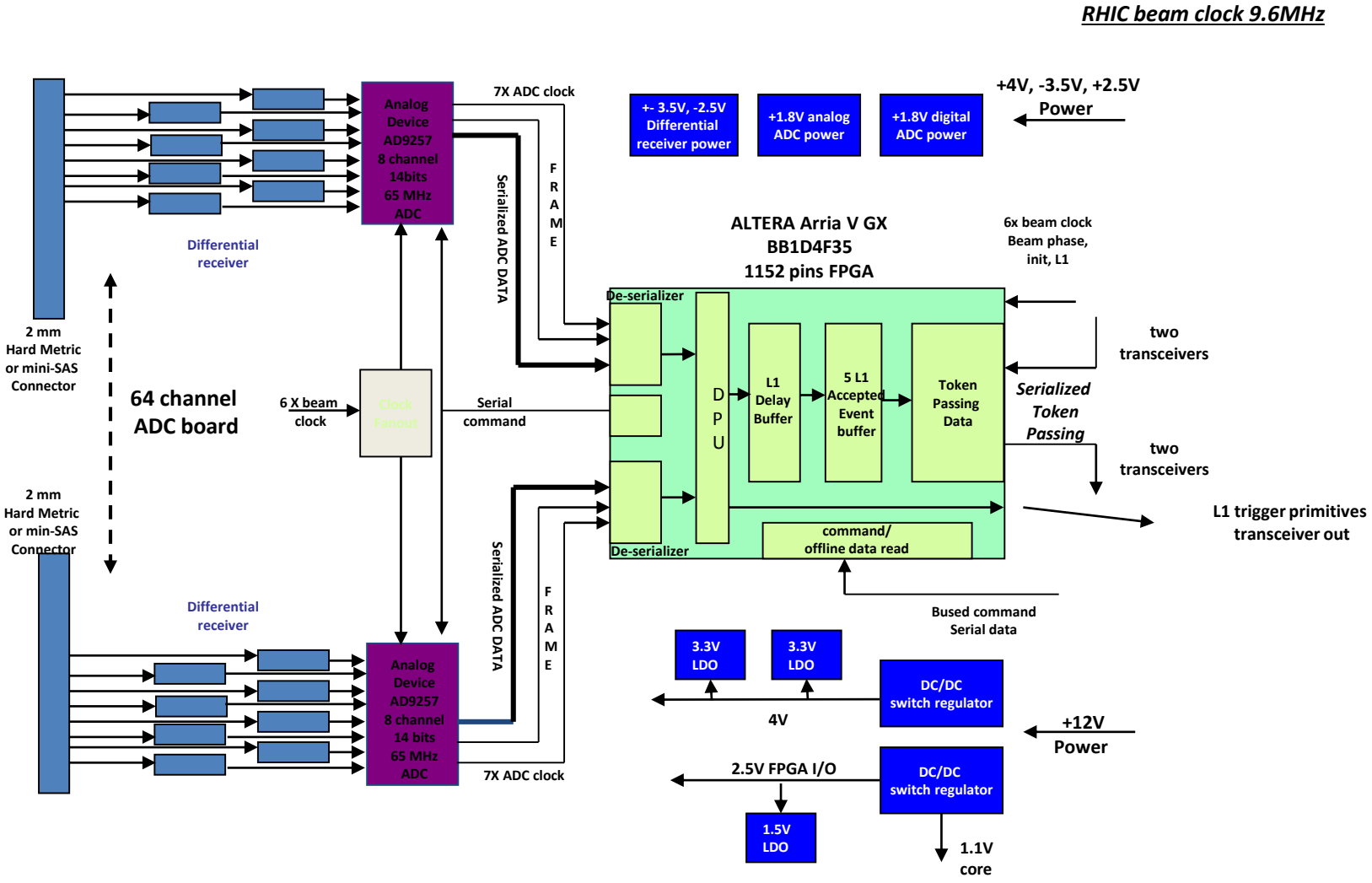
Receive timing information the PHENIX Granule Timing Module (GTM)

Generate L1 trigger primitives (not in the reference design)

Receive L1 trigger and send out L1 triggered event data to Data Collection Module II (DCMII).

Provide buffer for both the 40 beam crossing L1 delay buffer and 4 L1 triggered events

sPHENIX ADC Module Block Diagram

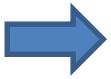


The Choice of ADC

The limit of ADC LVDS serializer seems to be less than 1Gbits/sec
→ 65 MHZ ADC

The FPGA does not have 128 LVDS De-serializer → 1 LVDS output per ADC channel

JSED204B's ADC need the transceiver to receive data
→ Limits number of ADC can be connected to the reasonable price FPGA



Analog device AD9249
- 16 channel 14 bits ADC. Maximum sampling rate 65 MHz SNR 75db
- 1.8v technology. 58mw per channel at 65 MHz -> 1 W per chip.
- 144 pins package. 1cm X 1cm BGA
- *pipeline latency 16 clocks.*

Analog Device **AD9257**
- 8 channel 14 bits ADC Maximum sampling rate 65 MHz SNR 75.5 db
- 1.8v technology. 55mw per channel at 65 MHz
- 65 pins LFCSP package. 0.9mm by 0.9mm.
- *pipeline latency 16 clocks.*

Texas instrument ADS5294
- 8 channel 14 bits ADC. Maximum sampling rate 80 MHz SNR 75.5db
- 1.8v technology. Per channel 58mw at 50 MHz, 77mw at 80 MHz.
- 1-wire only interface only for below 50 MHz sampling
- 80 pins QFP package. 12mm by 12mm
- included digital processing block (only after digitization)
- *pipeline latency 11 clocks for 1 wire interface.*

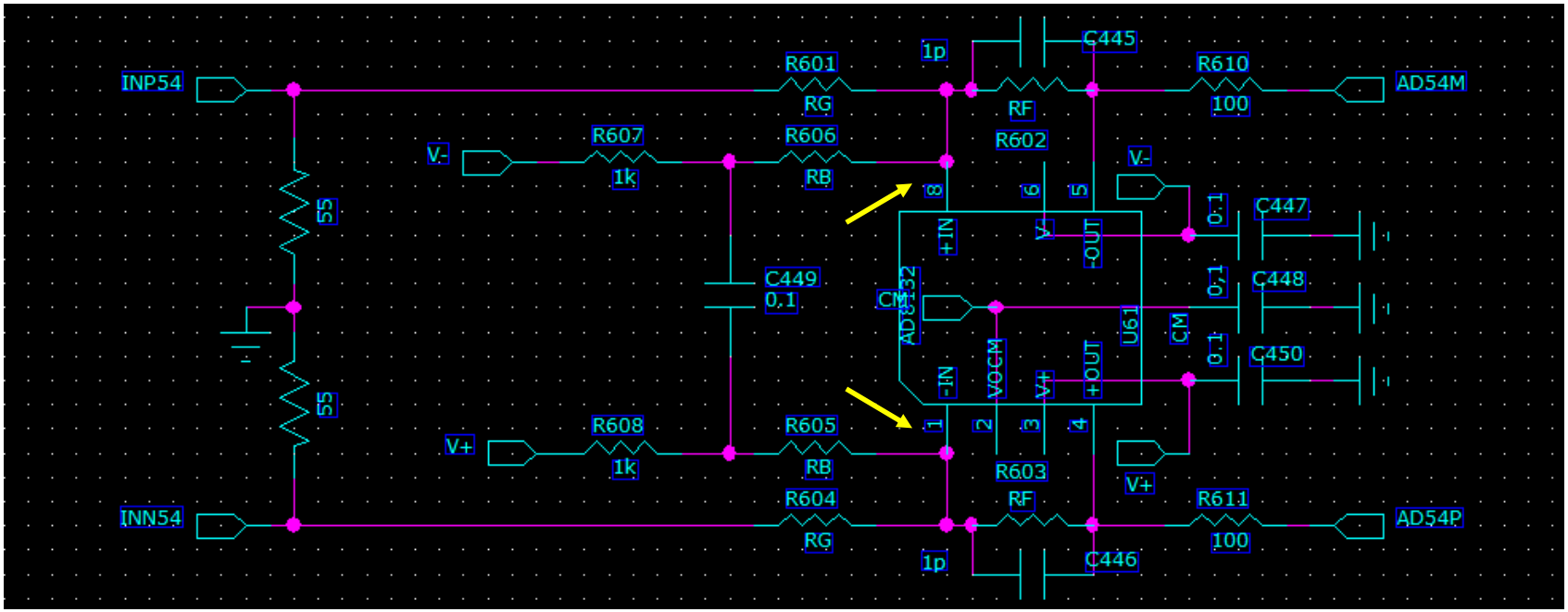
Linear Technology LTM9008-14
- 8 channel 14 bits ADC. Maximum sampling rate 65MHz SNR 73 db
- 1.8v technology. Per channel 88mw at 65 MHz.
- 140 pins BGA. 11.25mm X 9mm
- pipeline latency 6 clocks.

The ADC system has 14 bits output (0- 16383 ADC counts)

The ADC input is differential, need to supply both + and – inputs (peak-peak range is 2V)

(122 μV per ADC counts)
+1V on the positive side and –1V on the negative side
8192 ADC count happened when V+, V- difference is zero
Our signal only swing one side

To get full range we need to offset the signals. → (the point to introduce the noise)

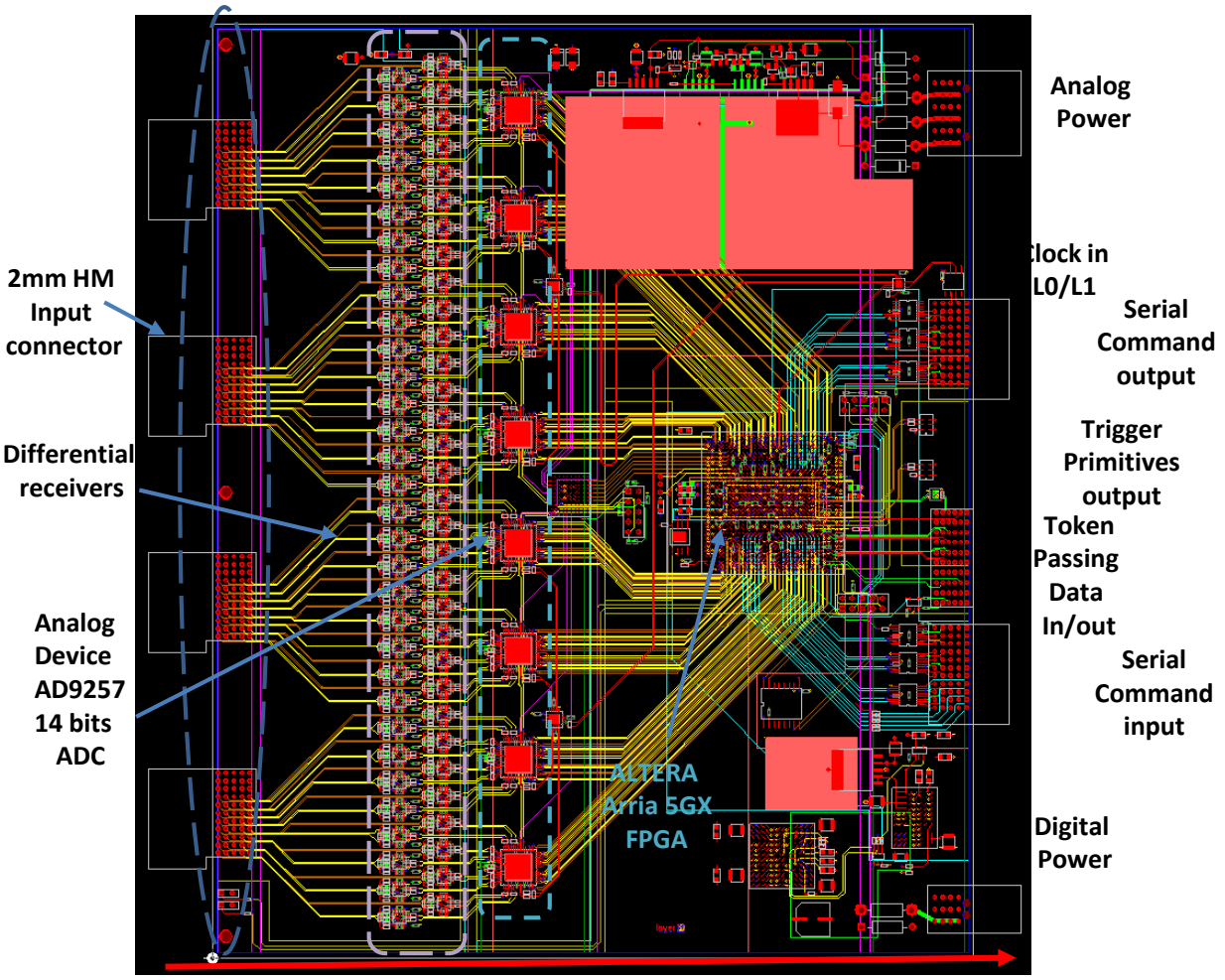


SPHENIX ADC board

64 channel inputs
2mm HM connectors
160mm by 190mm (6U board)

The 8 channel 14 bits ADC will be running at 6x beam crossing rate ~ 60 MHz

Altera Arria 5GX FPGA de-serialize data, provide 4 events buffer, 40 beam crossing L1 delay, token passing data, L1 trigger primitives output



Thoughts on the Trigger Primitives.

FEM can do rough gain correction → We will do on board 2x2 sum first
If trigger primitive output will be 8 bits, for 40 Gev top scale, the least count will be ~156 Mev if the scale is linear.

If we output 8 bits per channels, the optical bandwidth will be 10 (8b/10b encoding) *64 * 10 MHz = 6.4 Gbits/sec. if one only output 2X2 sum, we will only have 1.6 Gbits/sec. With formatting, the output will be 2 Gbits/sec. (1 frame marker + 1 header + 8* (2* 8) data words.)

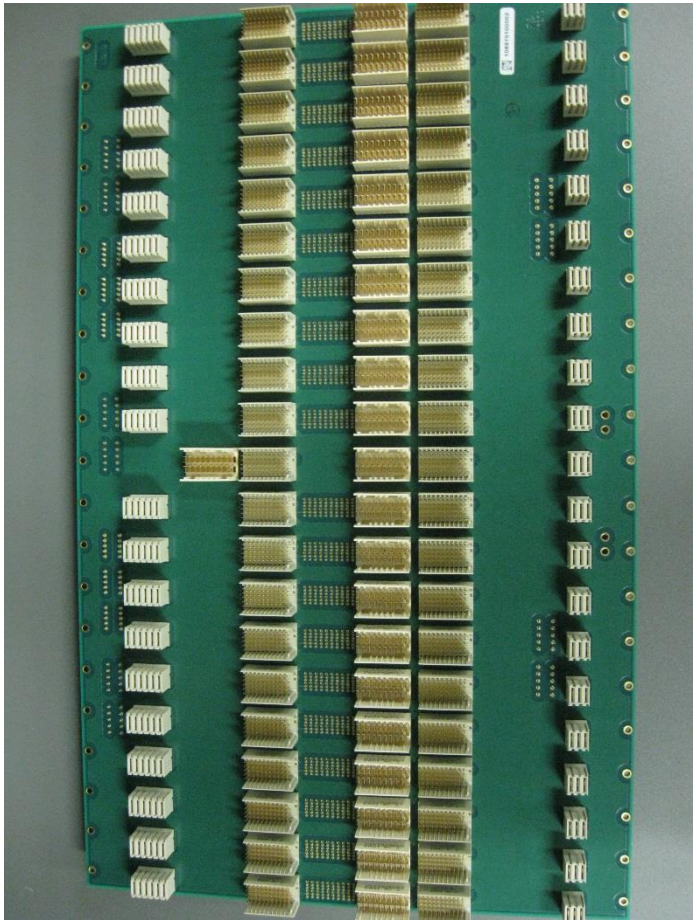
if trigger sum is 10 bits, we will have (1 frame marker + 1 header + 10 16 bits data words.), The optical
Bandwidth will be 20 (bits)*12 words* 10 MHz = 2.4 Gbits/sec

The FPGA has a high speed transceiver port to the backplane with high speed LVDS repeater. A rear mounted optical transceiver could be used to send out L1 trigger primitives.

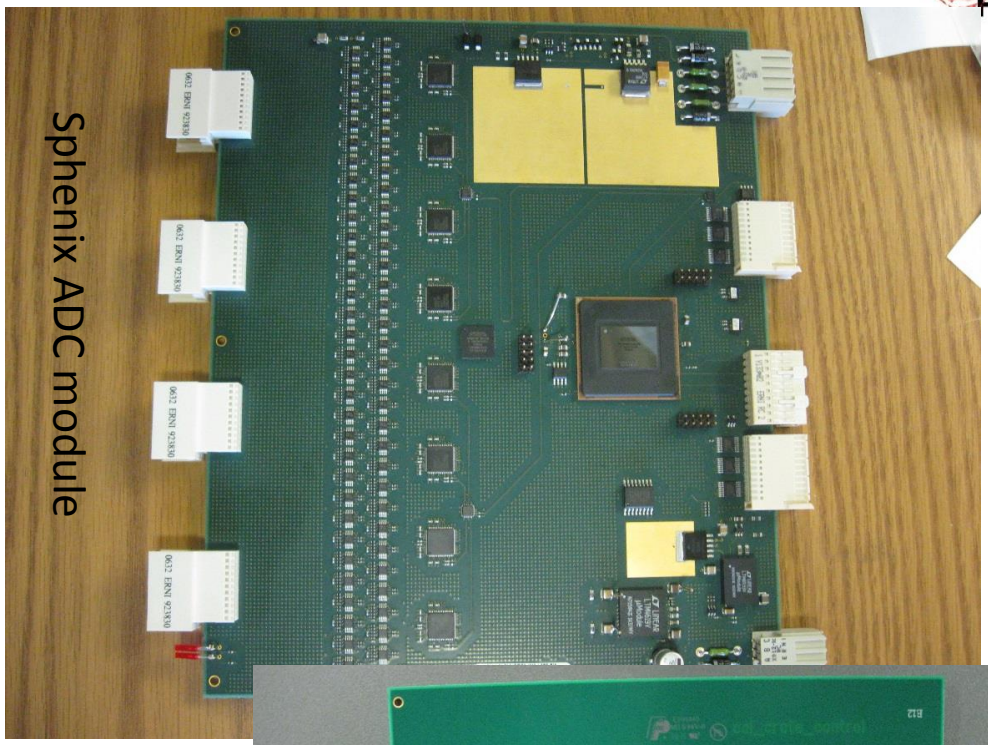
FPGA code is being developed to study the memory usage if correction table are used to correct the data.

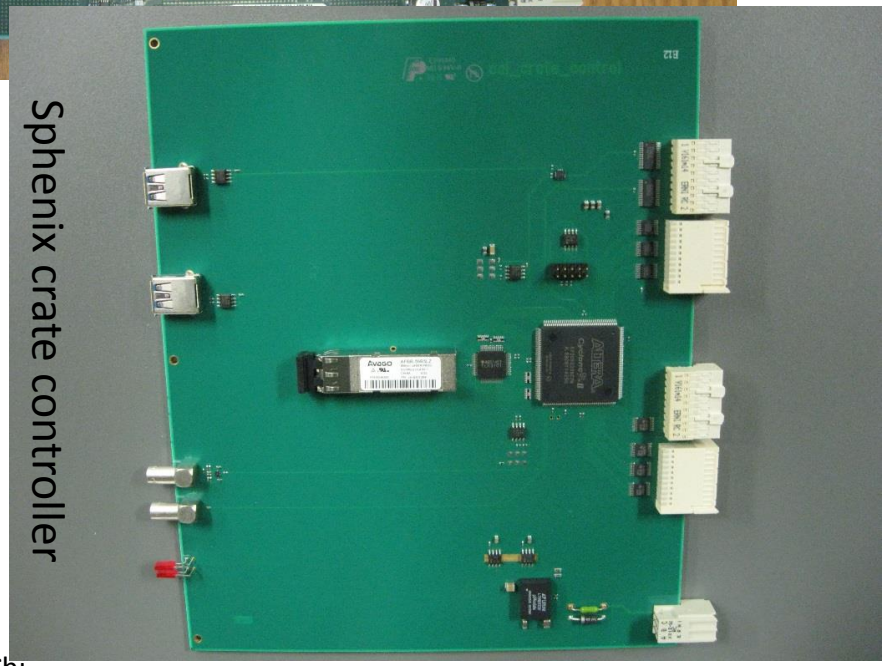
Prototype Progress

- ADC Module, Crate Controller and Backplane prototype modules have be build.
  - This is enough for us to test analog function.
    - Can we safely built 64 channel ADC module with reasonable performance?
    - Will offset circuit introduce more noise into the system?
  - The XMIT module is on the way



Sphenix ADC backplane

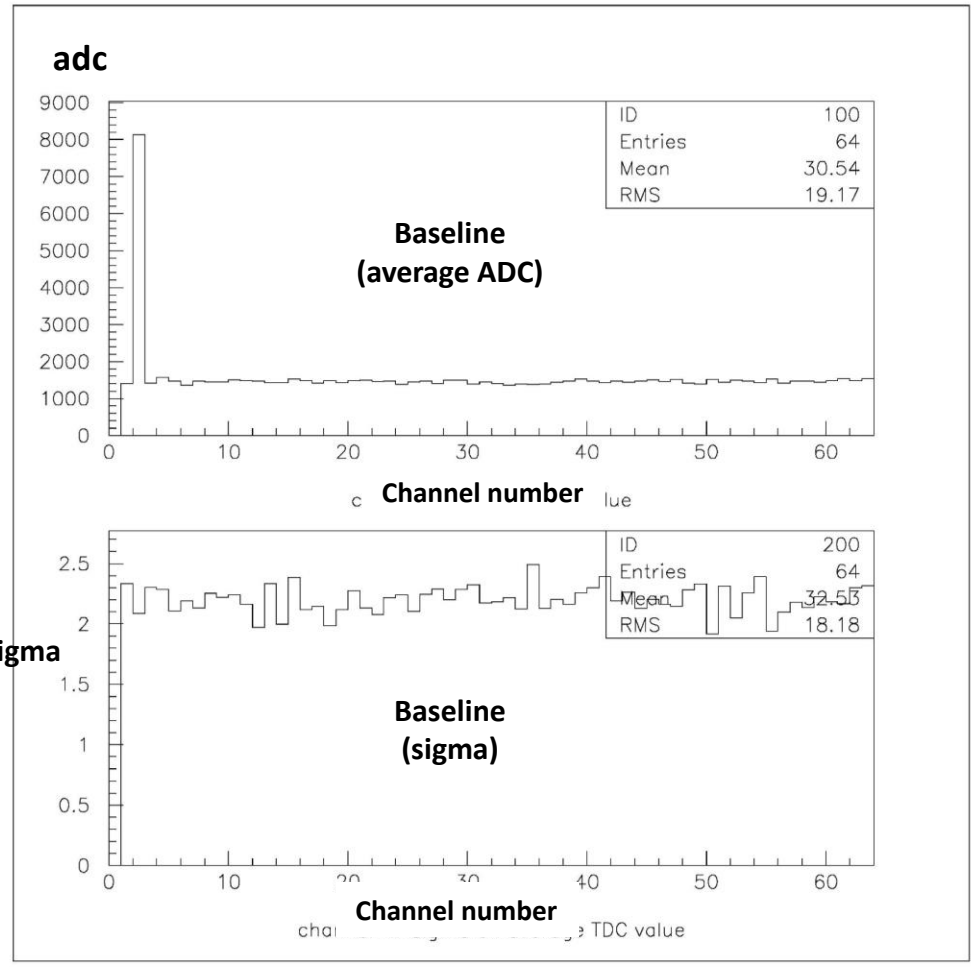


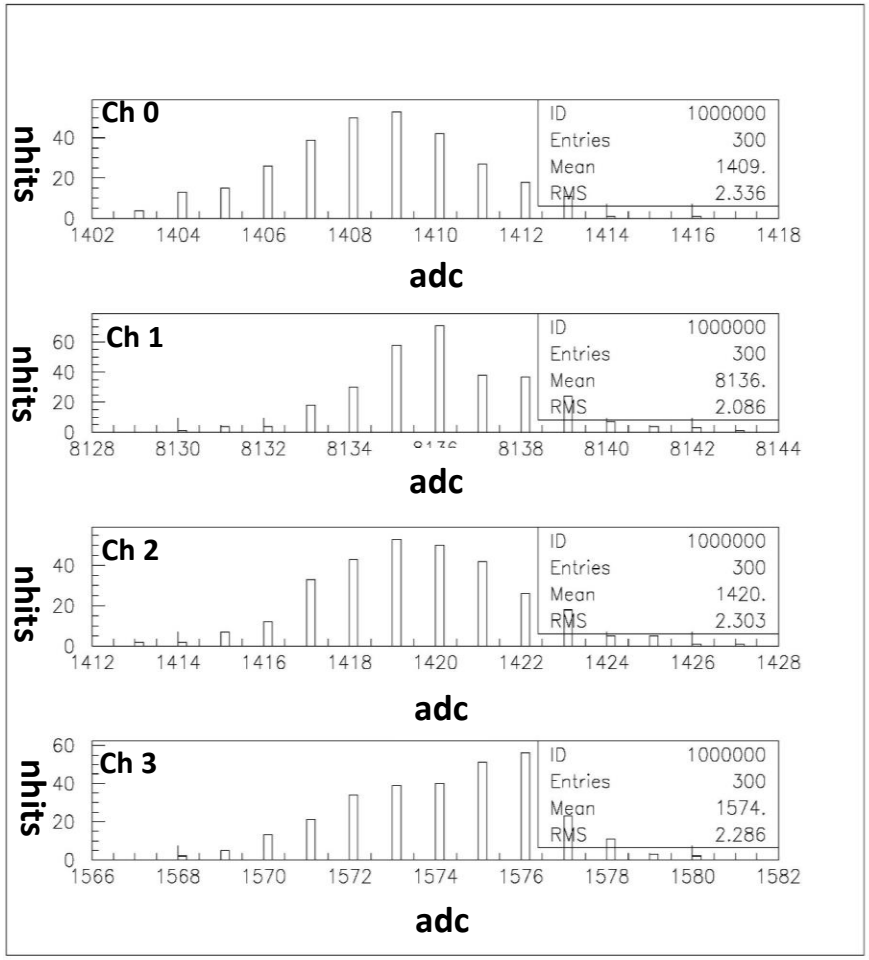


ADC Board Performance

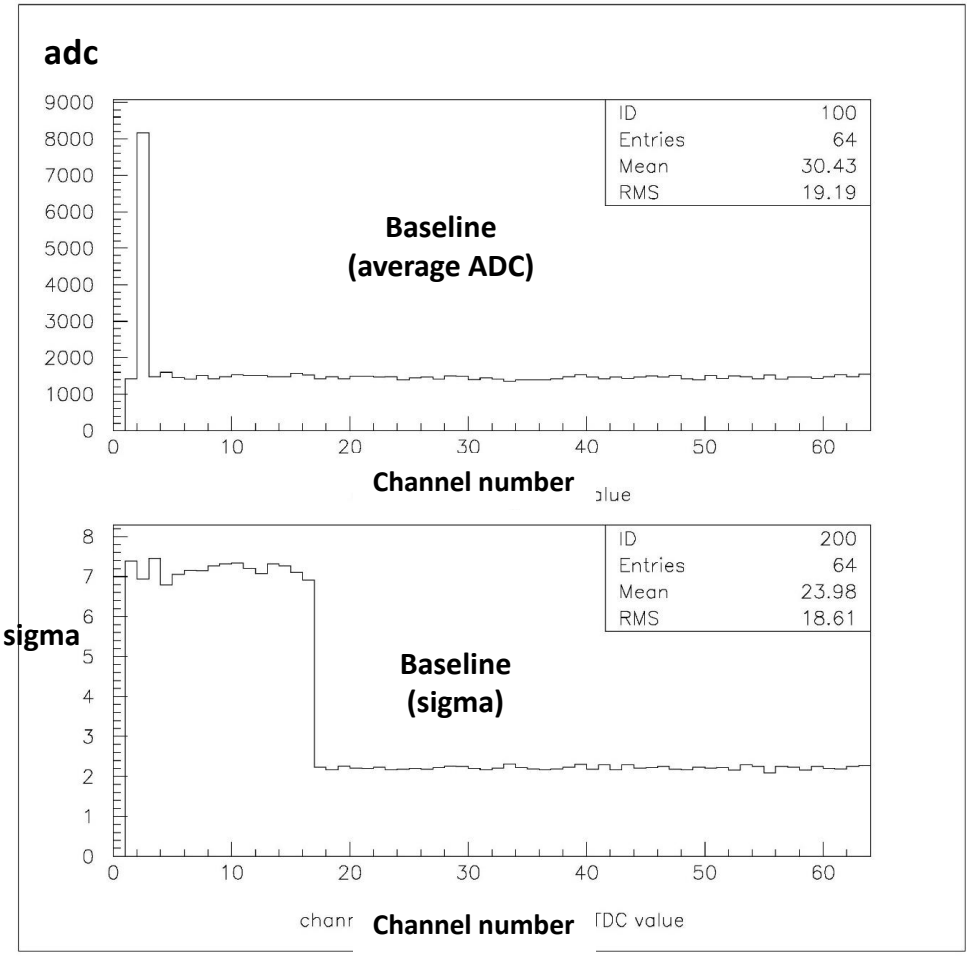
(*baseline, no signal*)

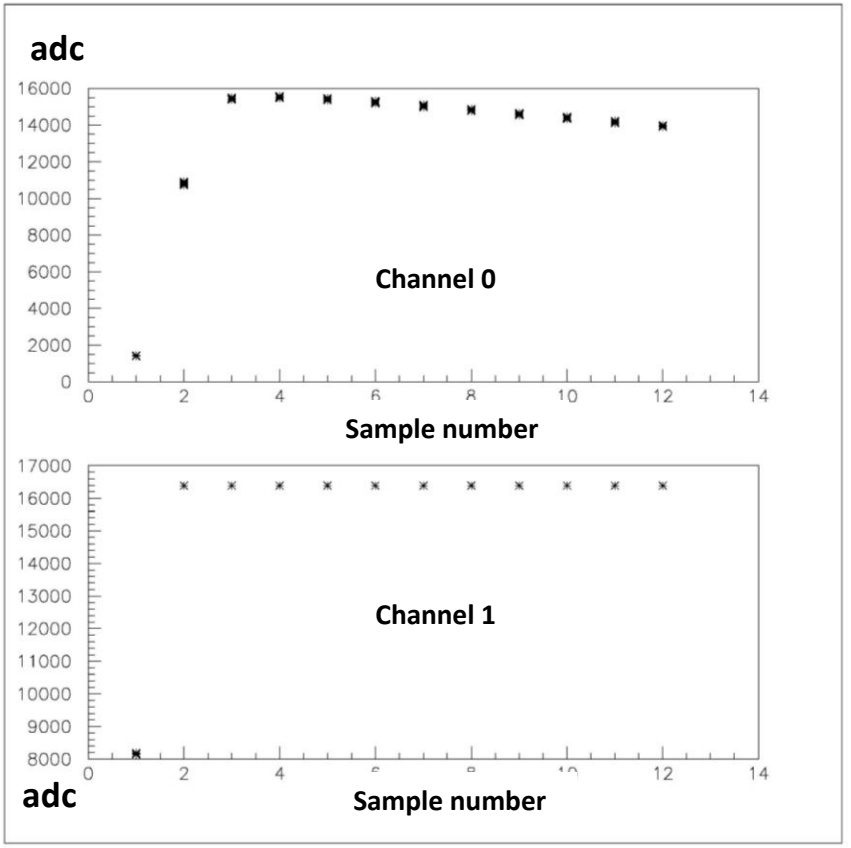
Channel 1 without offset





ADC noise test with existing HBD preamp

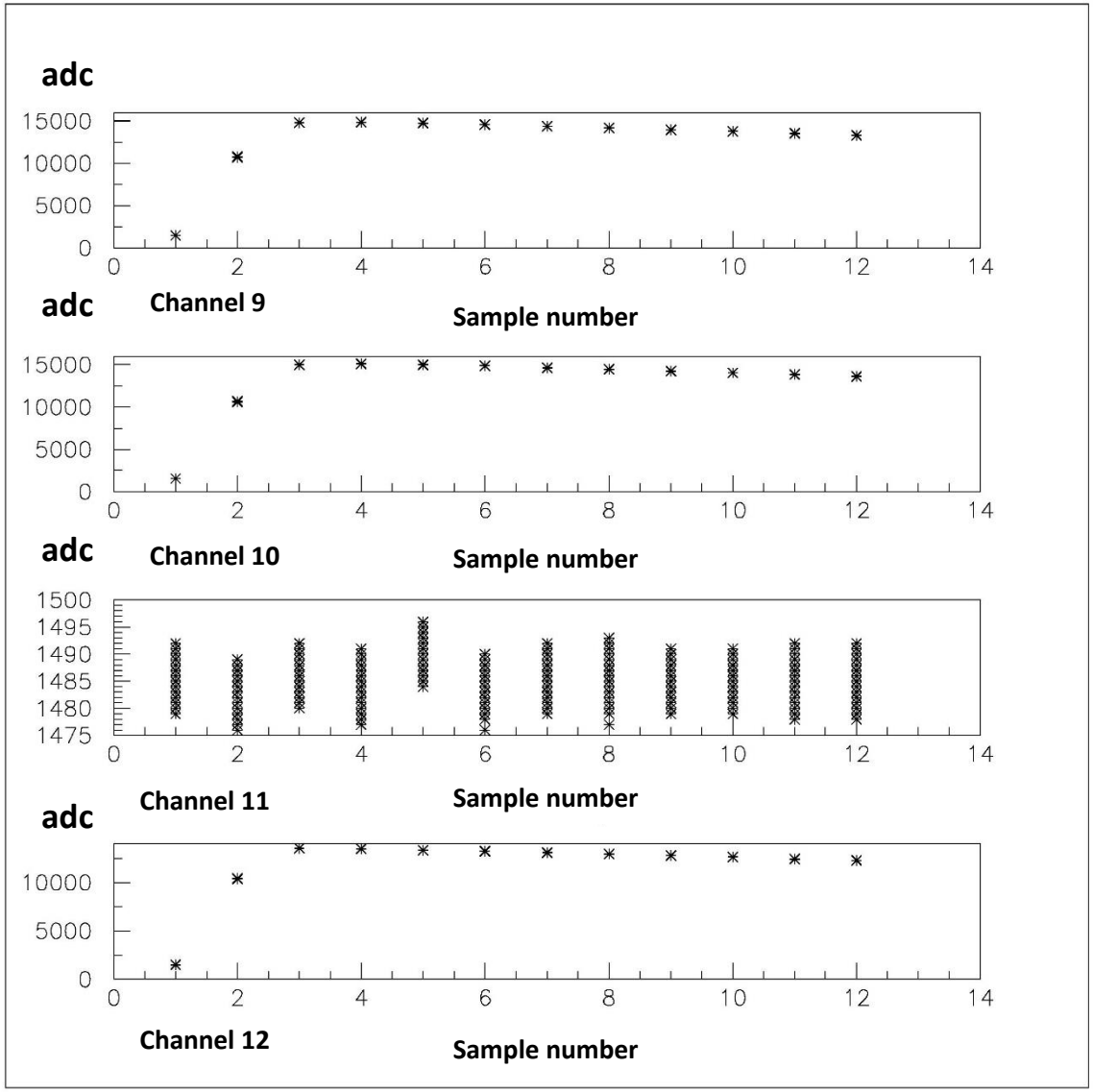




Cross Talk Study

Cross talk with existing HBD preamp (similar rise time)

6 meters of 2mm HM cable



Production Flow

- Last prototype cycle of the electronics should dress production needs.
  - Testing, yield etc.
- Parts and Printed Circuit Boards (PCB) procurements.
  - Work with distributors on getting the parts.
  - Work with prototype PCB vendors.
- Board assembly.
  - Have a preproduction run.
  - Work with prototype board assembler.
  - Schedule the board delivery to match with testing flow.
    - Feedback to assembler.
- Testing
  - Set up at least 2 test stands.
    - One for testing. The other one for debugging.
  - Probably can do at least 10 boards a day.

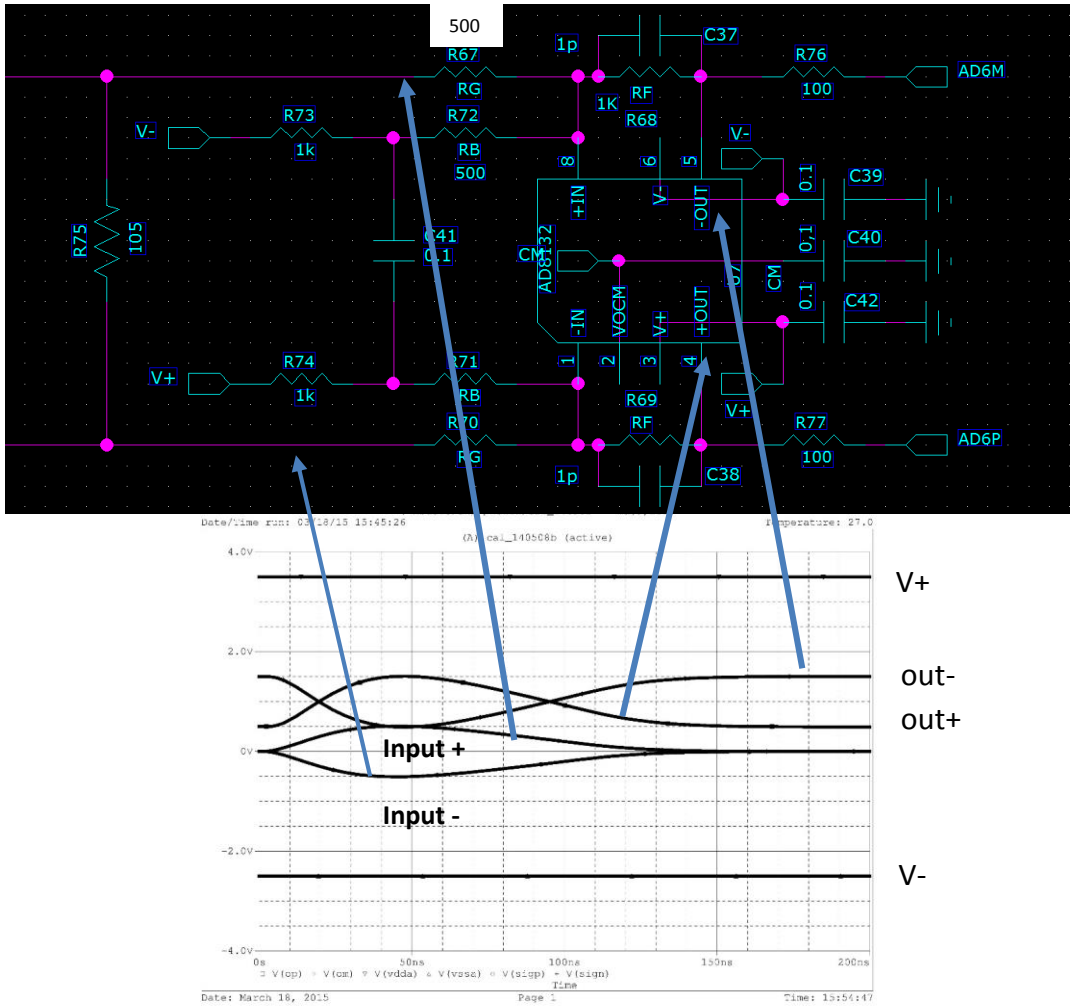
Cost of the system

- The design of the digitizer is to minimize the cost of the system.
  - Compact 6U design.
    - Save space reduce the PCB cost. Saving the rack space. Easy handling.
  - Use low cost FPGA to handle all ADC data, event data flow and Level 1 trigger primitives.
- Except for the clock master module to interface with GTM system, we have design reset of the system excluding the trigger portion.
  - We have asked our vendors for budgetary quotes.

Status and Outlook

- Prototype modules of ADC, Controller and Backplanes have been build.
  - Testing ongoing. So far it is O.K.
  - XMIT module will be complete before end of the year.
- Prepare to use the new system for upcoming testing beam
  - readout system with 2 ADC modules, 128 channels.
- Need to test trigger primitives output.
- Need to address the test system for the ADC analog inputs.
- Some modification to the design/layout may be necessary for the 2nd round prototype
  - Enhance testing features.

Backup Slides



Differential Receiver

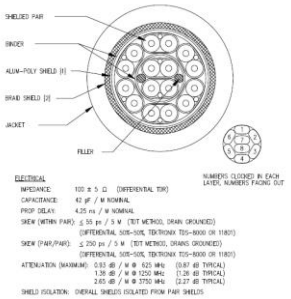
The ADC module will receive the signal from the On detector module.

The signal will be AC coupled. The blocking capacitor will be on the frontend.

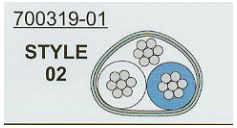
The ADC's Vcommon is at 1V. With the signal swing +-0.5v among Vcommon. To get full range of the ADC, the signal need to swing in both direction. The signal from the detector only swing in one direction.

We offset the differential receiver to push the baseline to the lower ADC range.

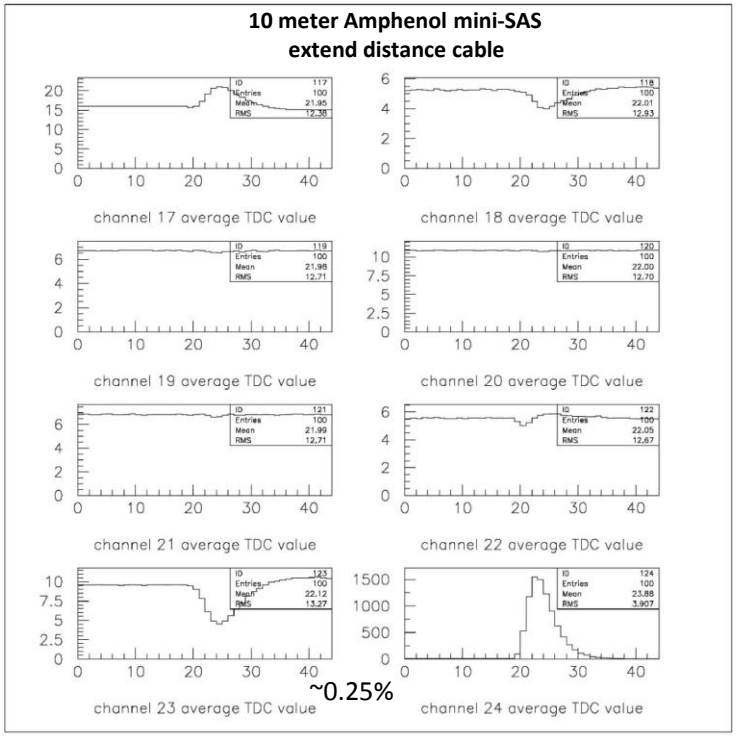
The resistors are discrete components. Supply voltages are adjustable through resistors.



SPHENIX cable cross talk study

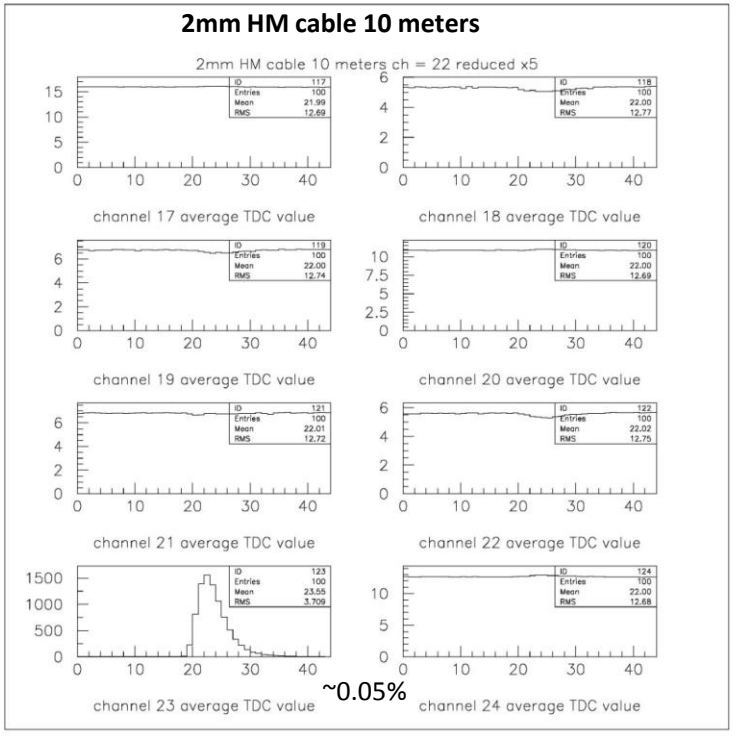


10 meter Amphenol mini-SAS extend distance cable



~0.25%

2mm HM cable 10 meters



~0.05%

Crate Controller

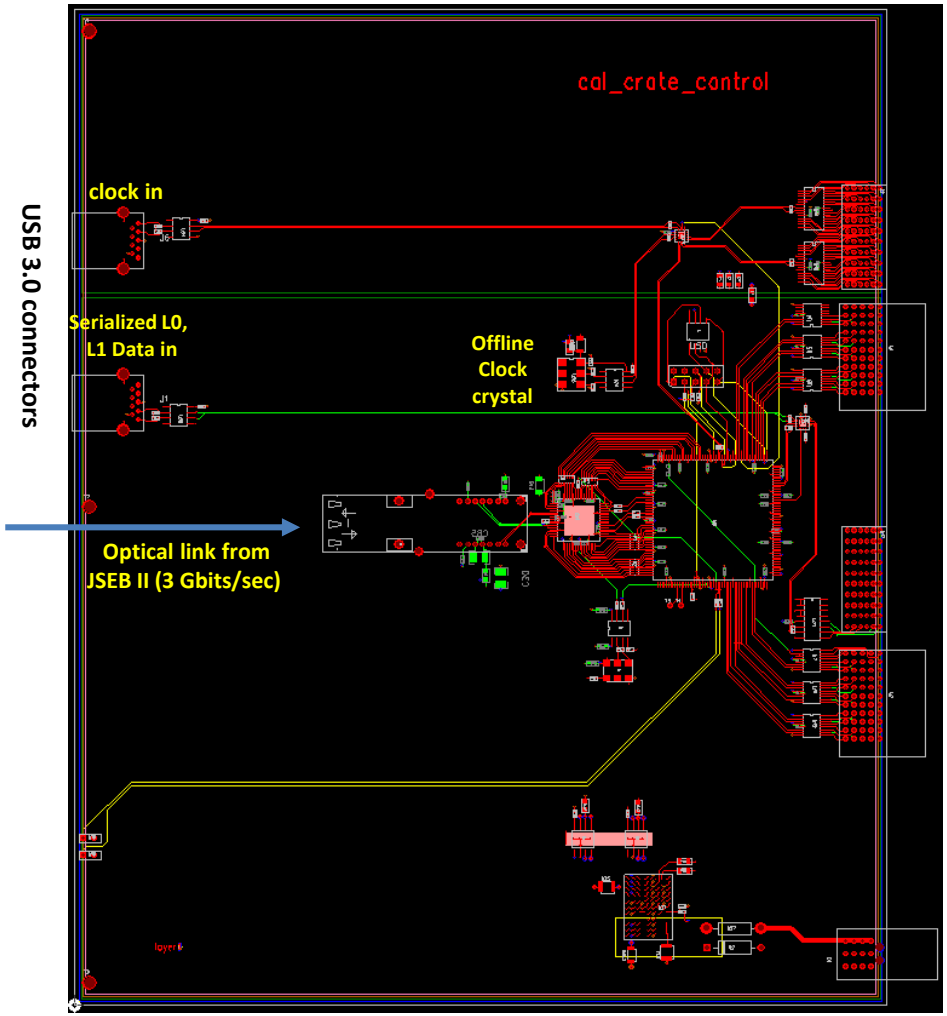
Receive clock and L0 (init, test etc), L1 trigger.

Receive slowdown load from DAQ system.

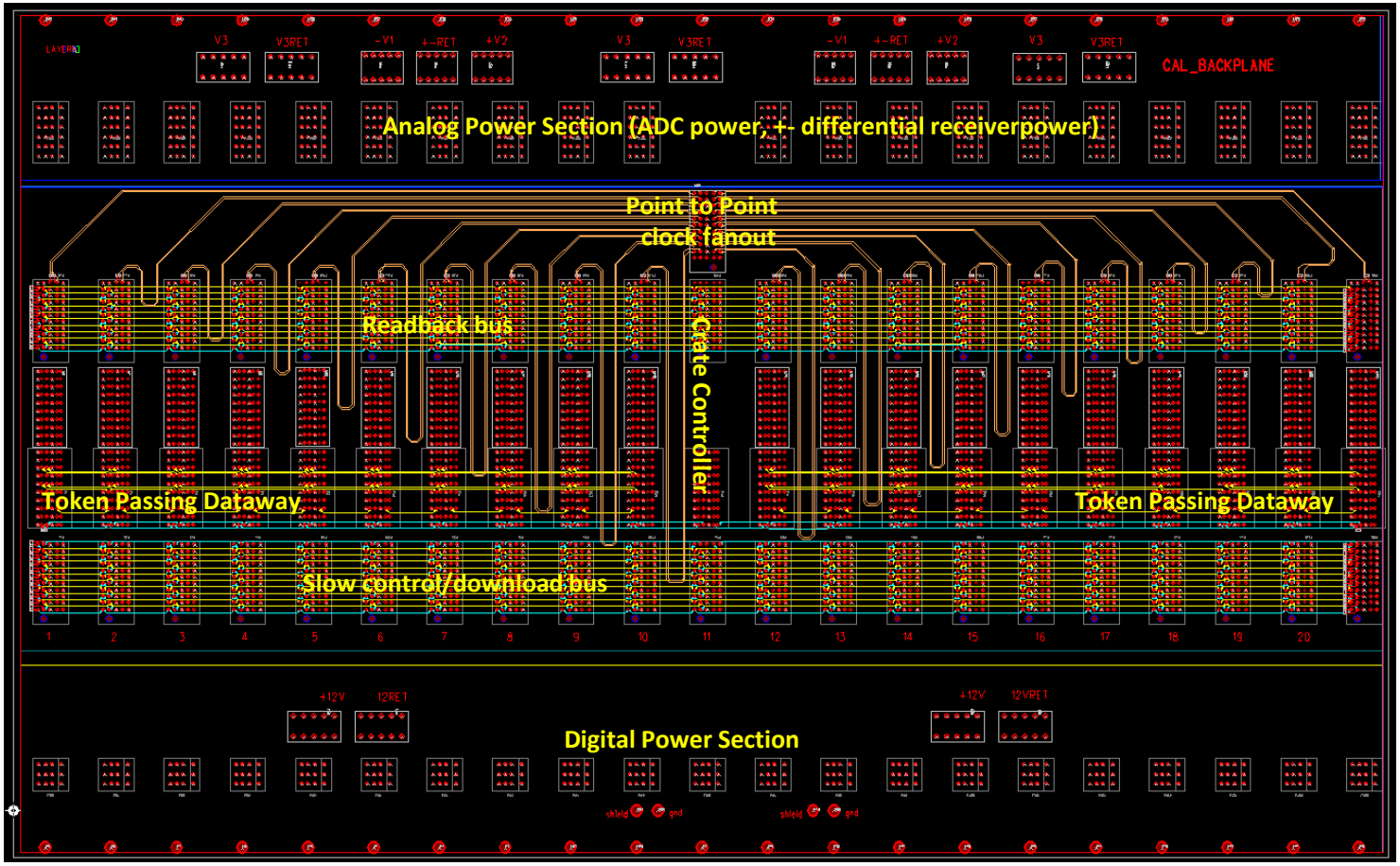
- Write ADC's module FPGA boot code to the EPROM.
- Write ADC, XMIT & Controller modules running parameters.
- Download varies table.
- Download fake data
- Initialize system. Set online/offline system

Provide offline clock/L0 data, L1 trigger. (standalone crate running)

Provide readback from ADC module to computer.



Crate Backplane



XMIT Module

. Receive data from FEM
. Issue token after receive all data transfer
. Format FEM data (header and checksum)
. Error handling