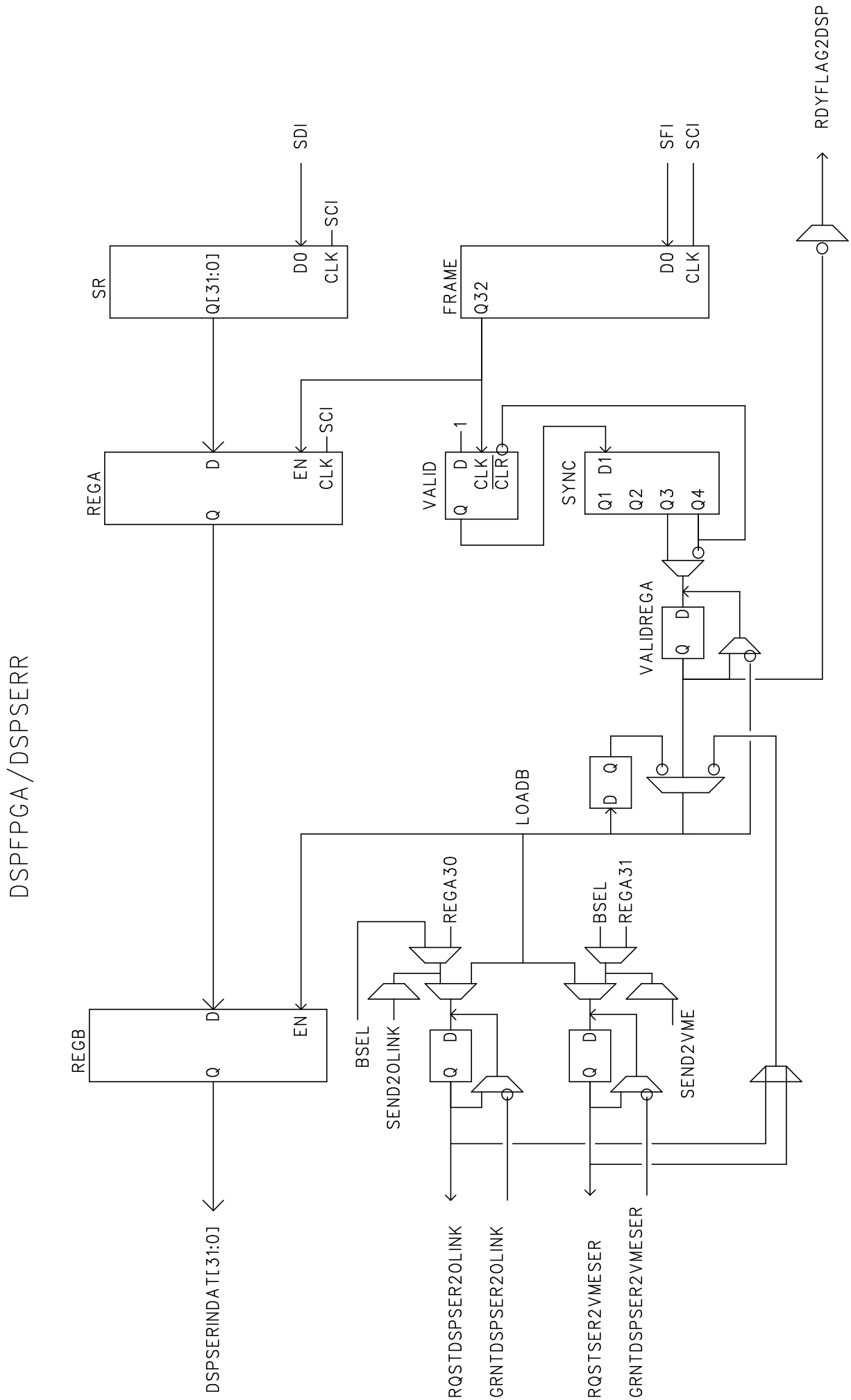
DSPFPGA/DSPSERR
SDI
SCI
SR
Q[31:0]
DO
CLK
SFI
SCI
FRAME
Q32
DO
CLK
RDYFLAG2DSP
REGA
D
Q
EN
CLK
SCI
VALID
1
D
Q
CLK
CLR
SYNC
D1
Q1
Q2
Q3
Q4
VALIDREGA
D
Q
LOADB
D
Q
REGB
D
Q
EN
BSEL
REGA30
SEND2OLINK
BSEL
REGA31
SEND2VME
DSPSERINDATI[31:0]
RQSTDSPSER2OLINK
GRNTDSPSER2OLINK
RQSTSER2VMESER
GRNTDSPSER2VMESER