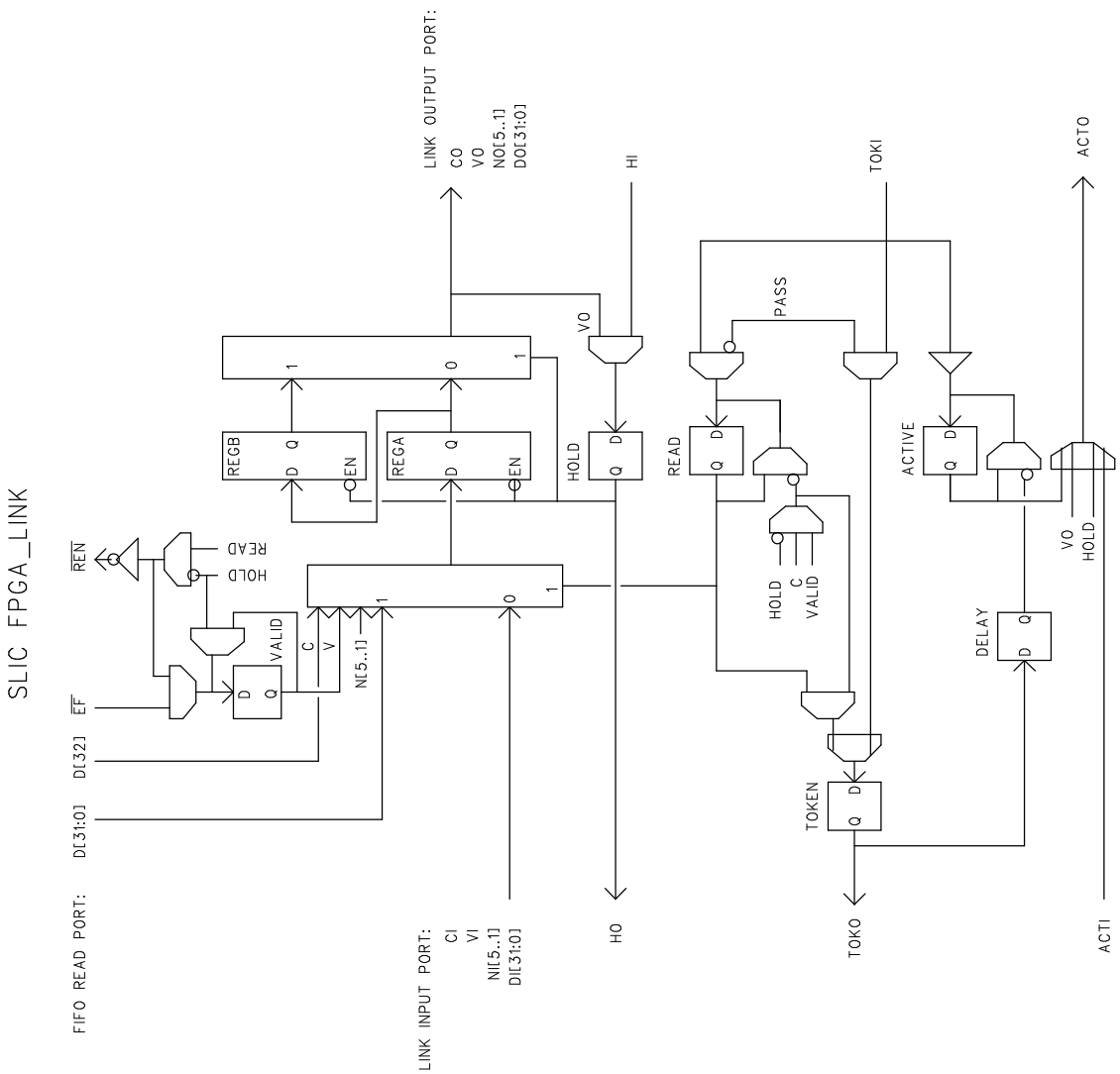
SLIC FPGA_LINK
FIFO READ PORT:
REN
EF
D[32]
D[31:0]
READ
HOLD
VALID
C
V
N[5..1]
REGB
REGA
EN
HOLD
VO
HI
HO
LINK OUTPUT PORT:
CO
VO
NO[5..1]
DO[31:0]
LINK INPUT PORT:
CI
VI
NI[5..1]
DI[31:0]
READ
PASS
HOLD
C
VALID
TOKEN
TOKI
TOKO
ACTIVE
DELAY
ACTO
ACTI
VO
HOLD