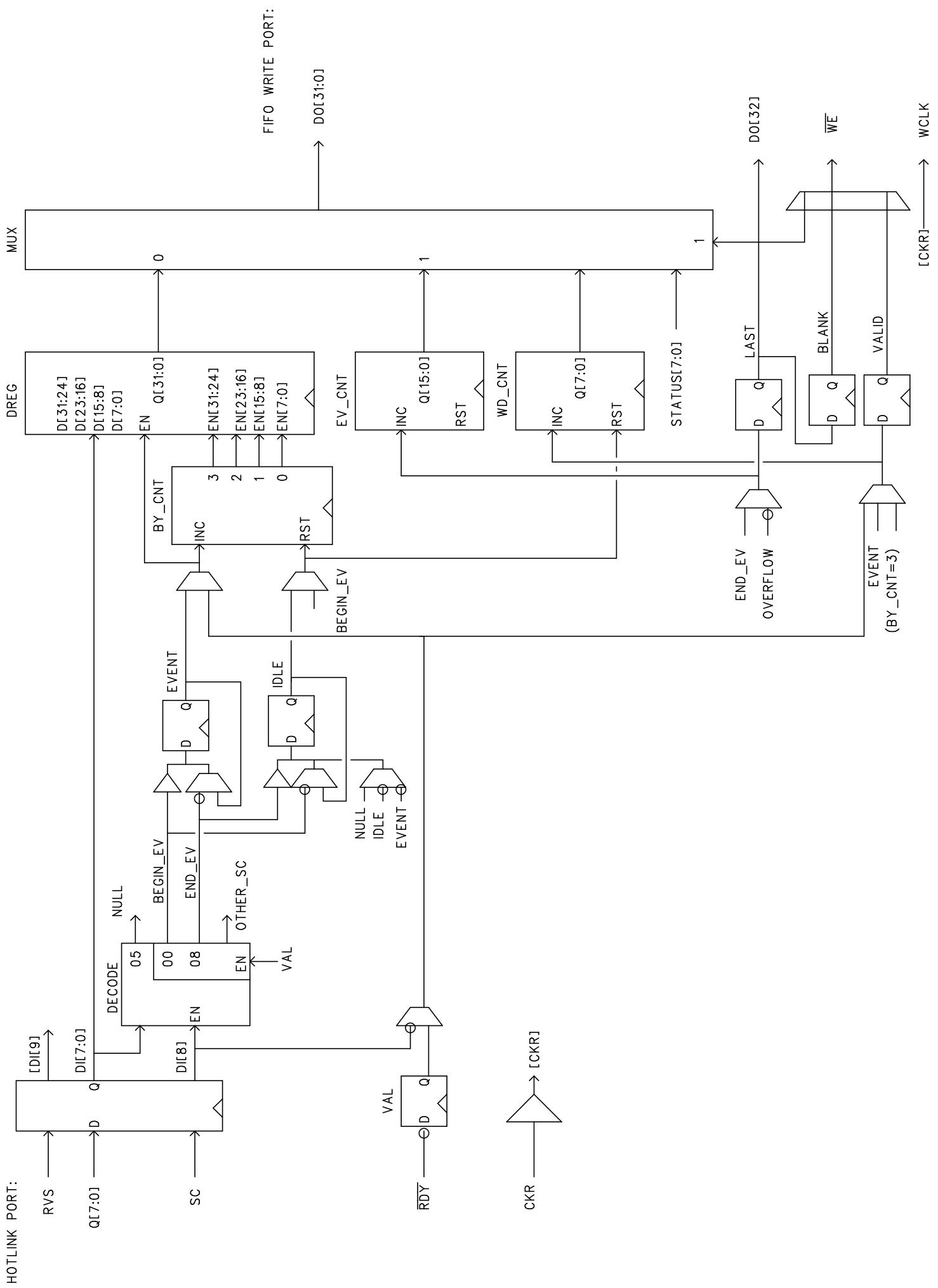
FPGA SLIC_REC
HOTLINK PORT:
RVS
Q[7:0]
SC
RDY
CKR
[CKR]
[DI[9]
DI[7:0]
DI[8]
D
Q
EN
DECODE
05
00
08
NULL
BEGIN_EV
END_EV
OTHER_SC
VAL
EVENT
IDLE
NULL
IDLE
EVENT
BEGIN_EV
BY_CNT
INC
RST
3
2
1
0
DREG
D[31:24]
D[23:16]
D[15:8]
D[7:0]
Q[31:0]
EN[31:24]
EN[23:16]
EN[15:8]
EN[7:0]
EV_CNT
Q[15:0]
WD_CNT
Q[7:0]
STATUS[7:0]
MUX
FIFO WRITE PORT:
DO[31:0]
DO[32]
LAST
BLANK
VALID
WE
WCLK
[CKR]
END_EV
OVERFLOW
EVENT
(BY_CNT=3)