H.Evans
Columbia U.

Phases of L2 Muon Commissioning

<table>
<thead>
<tr>
<th>Phase</th>
<th>Where</th>
<th>When</th>
</tr>
</thead>
<tbody>
<tr>
<td>1) Indiv. Board Tests</td>
<td>Inst's</td>
<td></td>
</tr>
<tr>
<td>Alpha</td>
<td>UIC</td>
<td></td>
</tr>
<tr>
<td>MBT</td>
<td>Umd</td>
<td>03/00</td>
</tr>
<tr>
<td>SLIC</td>
<td>Nevis</td>
<td>01/00</td>
</tr>
<tr>
<td>CIC &amp; SFO</td>
<td>Nebraska</td>
<td>03/00</td>
</tr>
<tr>
<td>2) Board-to-Board comm.</td>
<td>Inst's</td>
<td></td>
</tr>
<tr>
<td>MBT-SLIC</td>
<td>Nevis</td>
<td>10/99</td>
</tr>
<tr>
<td>MBT-Alpha</td>
<td>UIC</td>
<td></td>
</tr>
<tr>
<td>SCL-MBT</td>
<td>FNAL</td>
<td></td>
</tr>
<tr>
<td>3) System Integration</td>
<td>FNAL</td>
<td>07/00</td>
</tr>
<tr>
<td>L2Mu Crate</td>
<td>standalone?</td>
<td></td>
</tr>
<tr>
<td>L2Mu + Data Src</td>
<td></td>
<td></td>
</tr>
<tr>
<td>4) DØ-Style Running</td>
<td>FNAL</td>
<td>09/00</td>
</tr>
<tr>
<td></td>
<td>(MCH)</td>
<td></td>
</tr>
</tbody>
</table>

* my random guesses

Baseline Needs (all Phases)

- Crate (5V & 3.3V), Bit3, PC
- Data Source (*mid-Phase-3*)
Data Source Needs

- **Two Data Types:**
  1) SCL-Like \( \rightarrow \) SLIC Input 0
    - Initiates SLIC Readout
    - Format needs to be very similar to SCL structure
  2) Data-Like \( \rightarrow \) SLIC Inputs 2-15
    - Format not critical

- **Adjustable Event Rate**

- **Adjustable Delay b/w 1) & 2)**

- **Timescale**
  - Data Source only needed late in Phase 3 (late spring 00)
Phase 1: SLIC Goals

• **Data Rate Tests**
  – **The Test:** Circulate data & Count Errors
    * Hotlink Out → Hotlink In0 → Data Link → DSP → Hotlink Out
  – **Results:** Data errors in continuous running
    * limited by DSP Out Rate

• **Processing Tests**
  – **The Test:** Load (<100?) real events to all SLIC input fifos
    * Input → Processing DSP → Formatting DSP → VME
  – **Results:** Verifies Algorithms
    * Processing, Formatting, Monitoring
    * limited rate dependence
Phase 3: Goals

- **SLIC-MBT-Alpha Communication/Processing Tests**
  - **The Tests:** Real events from SLIC inputs through system
    * SLIC inputs → Proc. DSPs → Form. DSP → MBT → Alpha
  - **Results:** Tests communication throughout system for real events + L2Mu Monitoring
    * limited rate capability

- **Data Rate Testing**
  - **The Tests:** Send data from Data Source through system at variable rate
    * Data Source → CIC/SFO → SLIC → MBT → Alpha
  - **Results:** Data Errors in continuous running
    * Event structure limited by complexity of Data Source

- **Note:** all of these test can be done standalone
  - no dependence on L2 Framework
Phase 4: Goals

- **Fully Integrate w/ DØ**
  - SCL: realistic conditions
  - TCC: downloads
  - VBD to L3
  - Monitoring
  - *Possible w/ Pulser Triggers*

- **Cosmic Running**
  - **Advantages (over pulser)**
    * Algorithm test
  - **Disadvantages**
    * Limited rate(?)