

STATUS OF ADF BOARD DESIGN

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PLAN

ANALOG SPLITTER

ADF BOARD AND CRATES

DIGITAL FILTER

SCL INTERFACE

INTERFACE WITH TAB

FUTURE WORK

ANALOG SPLITTER

DESIGN

Schematic captured

PCB design on the way

Board dimensions: ~30 cm x 10 cm because connector spacing matches the pitch of the existing CTFE's

COMPONENTS

Some components being ordered

We will need termination capacitor (CMS 470nF) from D0 in the next few weeks

ISSUES

Where do we get the cables and who does it:

- cables ~10 cm to connect output of splitters to CTFE's**
- cables of ~3 meters to connect to future ADF prototype**

ADF CRATE AND VME INTERFACE

MODEL OF CRATE INVESTIGATED

Wiener 6023 Plenum bin for 6U cards; (12U or 9U crate height?), VME64x backplane

Cost with power supply and fans: 9050 Euros (8000 \$)

ALL I/O PLACED AT THE BACK OF THE CRATE

Can we get 5 rows VME inverse female connectors that do not have right angled pins?

If yes: a pluggable backplane on P2 with 20 connectors 5 rows on one side and 320 BLS cable connectors on the other side

If not: 20 rear side transition cards, each with 1 connector 5 rows and 16 BLS cable connectors

VME INTERFACE / VME INTERCONNECT

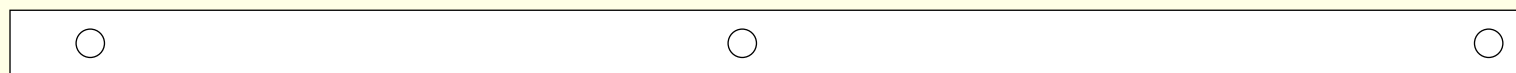
SBS/Bit3 VME PCI Interface model 618: 5000 Euros

-> At present we have decided not to purchase this;

-> Can D0/Fermilab lend us one spare?

-> We might need 2 in the future: 1 at Saclay and 1 at Fermilab

IEEE P1101.11 REAR SIDE I/O TRANSITION CARD



233 mm (6U)

110 I/O available + 16 GND

95 I/O avail.

RJ2/RP2

RJ0/RP0

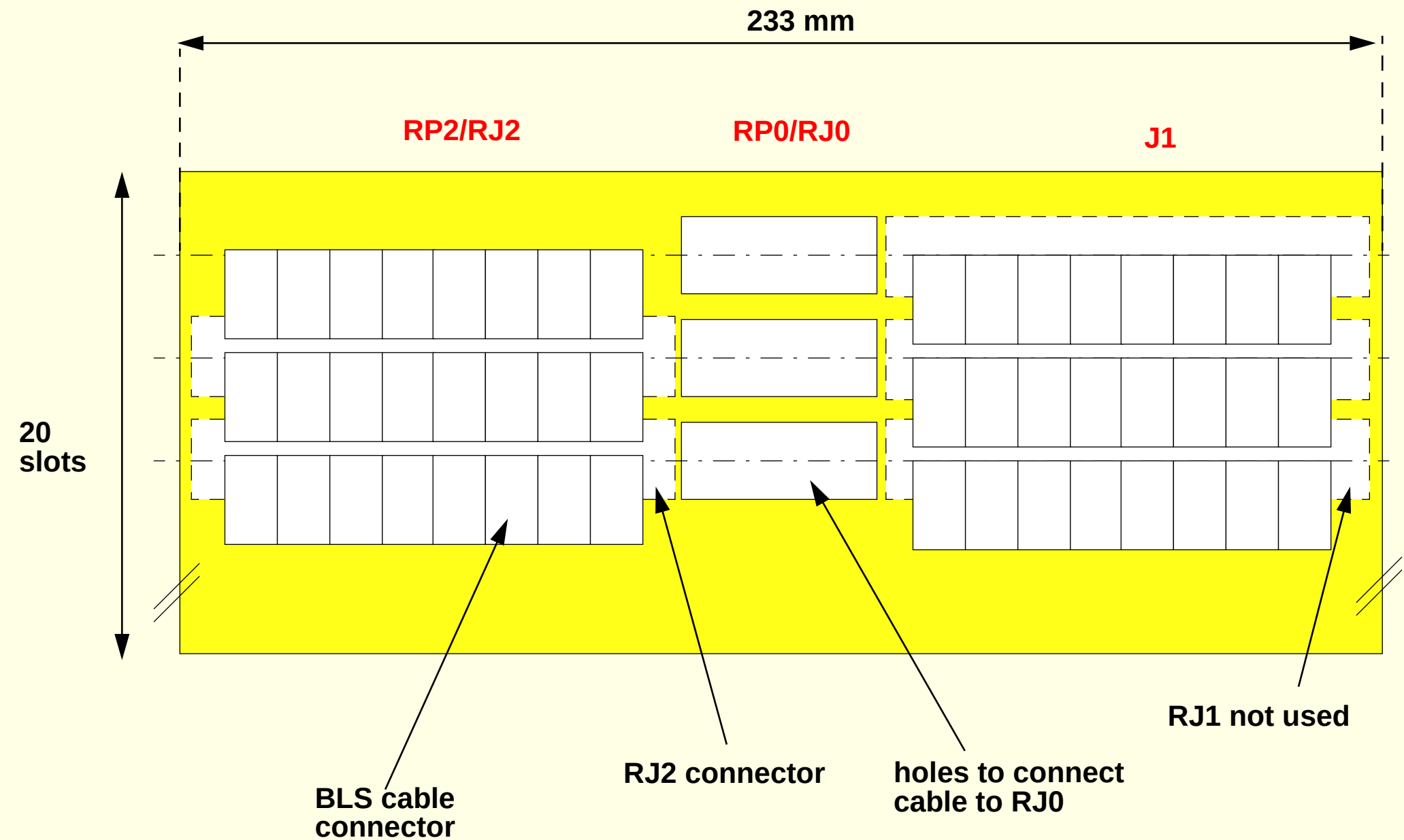
VME P1/J1

80 mm

3 x 10 pairs

16 cables from BLS (32 differential analog channels - 64 signal wires)

REAR-SIDE 6U TRANSITION BACKPLANE



STATUS ON FPGA AND FIRMWARE

VHDL CODING

Logic for one channel almost coded and simulated

Bus interface coded

Missing: interface to SCL signals distribution; FPGA download & bootstrap

FPGA TARGET

Choice almost finalized: 500K gate Xilinx Virtex II FG 456 speed grade: -4 (slowest)

8 channels per device; ~80% of the logic used; 75% I/O used

Post-routing simulation shows device running at 64 MHz (goal is 61 MHz)

Cost per FPGA: 142 Euros (120 \$); 4 chips per ADF card

LATENCY BUDGET

Total from ADC analog input to MSB out of the FPGA serializer: 6.5 BC

(need to add Channel Link SERDES and all cable delays)

