L1CAL & CAL-TRK LATENCY

updated 26-Jun-02

Step	delta-t (clk)	delta-t (ns)	cumul-t (ns)	Notes
Bunch Crossing		0.0	0.0	
Transmit to ADF				
BC to ADF		650.0	650.0	TDR - measured
sub-total		*650.0*	*650.0*	
ADF	*CLK units (ns)*	*16.5*		Calvet Mail - 25-Jun-02
ADC value valid	10.0	165.0	815.0	
ADC pins sensed	0.5	8.3	823.3	
Digital input decimated	5.0	82.5	905.8	
Peak at convolver output	26.0	429.0	1334.8	
Peak detect & dec. done	9.0	148.5	1483.3	
Et LUT done	1.0	16.5	1499.8	
Serial stream selected	1.0	16.5	1516.3	
Delay adjustment	0.0	0.0	1516.3	
Parity calc / 8-10 bit select	1.0	16.5	1532.8	
FPGA out valid - ser clk	0.5	8.3	1541.0	
LSB of chan at TAB	3.0	49.5	1590.5	
MSB of chan at TAB	7.0	115.5	1706.0	
sub-total		*1056.0*	*1706.0*	
TAB	*CLK units (ns)*	*11.0*		TDR - L1Cal section
Resynch inputs	12.0	132.0	1838.0	
Pipelined logic	10.0	110.0	1948.0	
Serialize Slide Win out	12.0	132.0	2080.0	
Ex,y calculations	12.0	132.0	2212.0	
Serialize output	12.0	132.0	2344.0	
SLDB to MTCal data ready		861.0	3205.0	TDR - measured
sub-total		*1499.0*	*3205.0*	
CAL-TRK				
MTCal to MTCM SLDB		544.0	3749.0	TDR - measured
SLDB to TFW		0.0	3749.0	assumes no MTM for Cal-Trk
sub-total		*544.0*	*3749.0*	
TOTAL			**3749.0**	
TFW decision due			3300.0	
Difference			449.0	