Status of ADF System Design
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- Analog Splitters
- ADF board
- ADF crate
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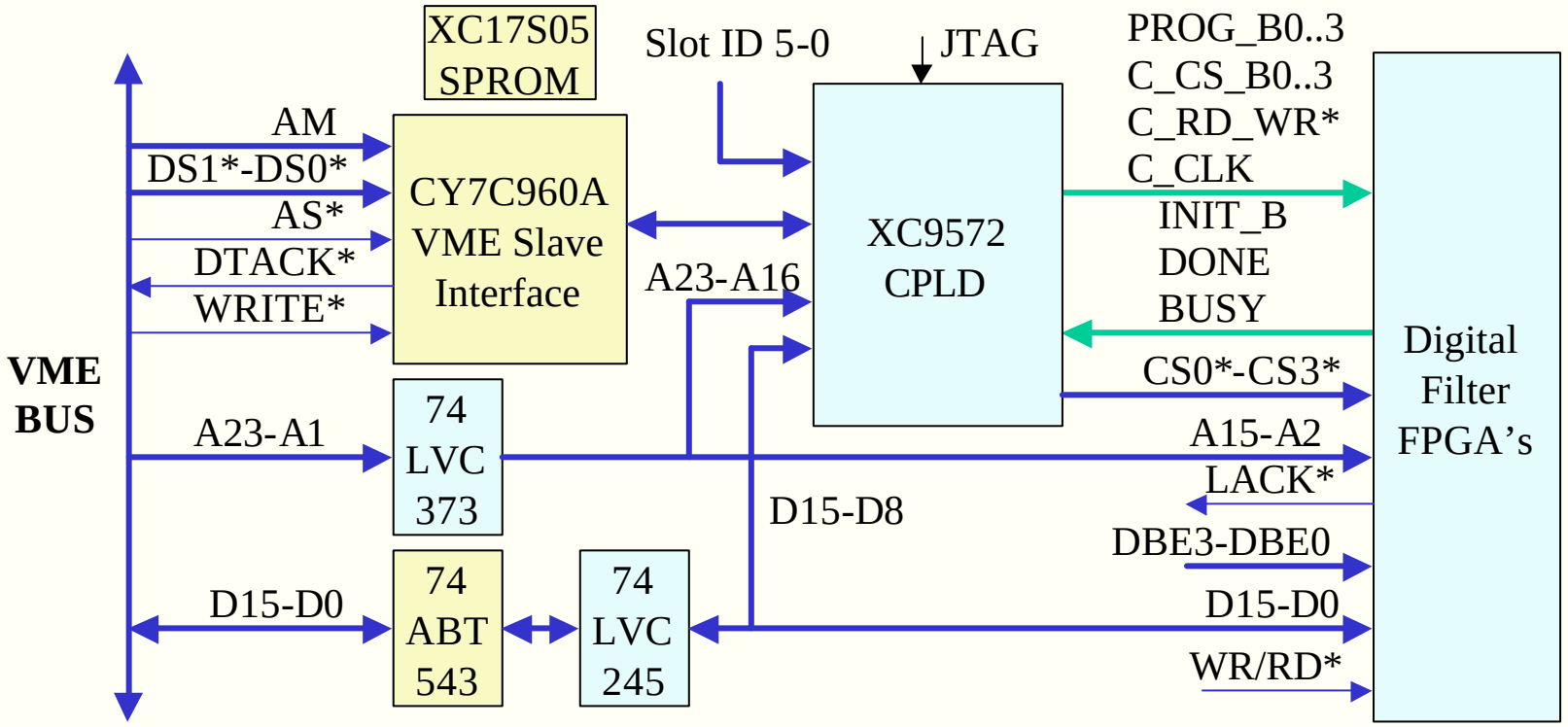
Analog Splitter

- Cabling of 1 board 80% completed
  - *1 minor error found: DC/DC converter need to be soldered on other side of PCB due to top/bottom view inversion*
- Test of prototype scheduled for October
  - *Need BLS/CTFE style cables: some short (~10cm) some ~5 m*
  -
- 3 other boards to cable
  - *will be done internally or not?*
- Still on schedule for installation in D0 during 2003 shutdown (February?) even if a second iteration of design/PCB/cabling is necessary

ADF Board

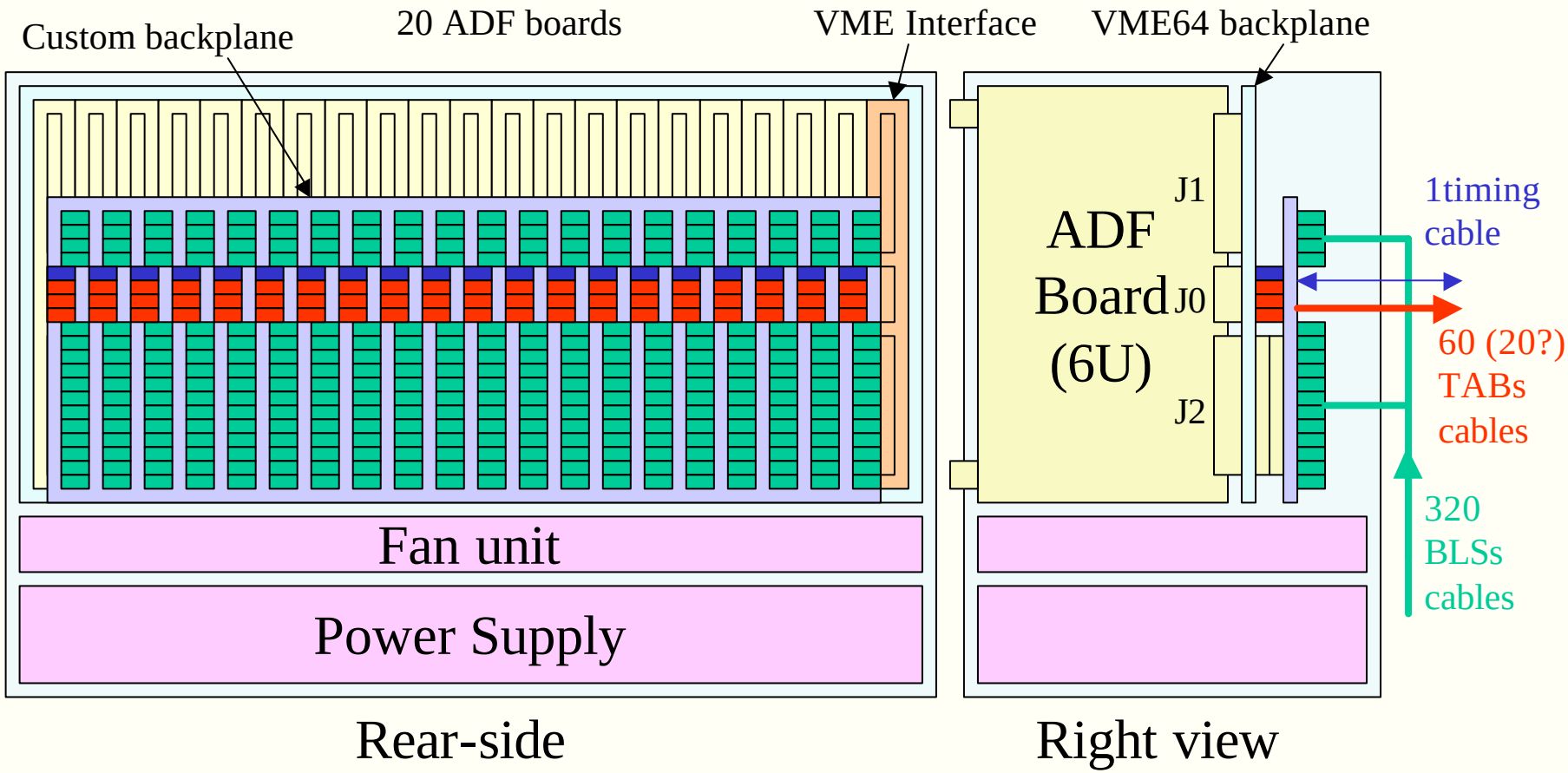
- Core FPGA (digital filter)
  - *VHDL coding 100% completed and simulated*
  - *8 channels synthetized, fitted in XC2V500 FG456 -4*
  - *Post-route simulation done*
- VME interface and bootstrap interface
  - *VHDL coding 100% completed and simulated*
  - *Programmable logic fitted in XC9572XL –10 TQ100C CPLD*
  - *Post-route simulation done*
- Board-level VHDL simulation
  - *Includes 4 FPGA's + VME interface + bootstrap logic*
  - *Just started for behavioral model; must have a more powerful PC for post-route simulations (1Gbyte RAM min.)*
  - *Need some control software to exercice the VHDL model*

VME interface and bootstrap logic



- Download FPGA configuration via VME:
  - *all 4 FPGA's loaded at once or different config on each FPGA*
- VME interface A24 D16-D8 only; no DMA; no interrupt
- Provides 5V <-> 3.3V conversion; Virtex 2 I/O not 5V tolerant

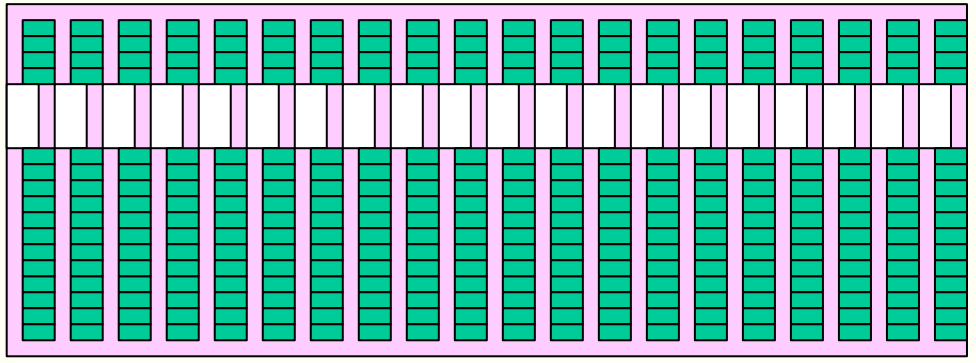
ADF Crate

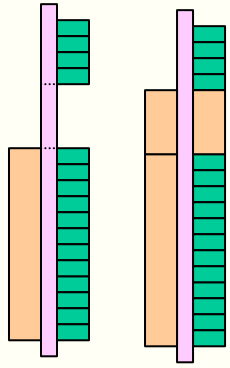


- Crate to be delivered ~November 2002
- Custom backplane: design not started

Custom Backplane

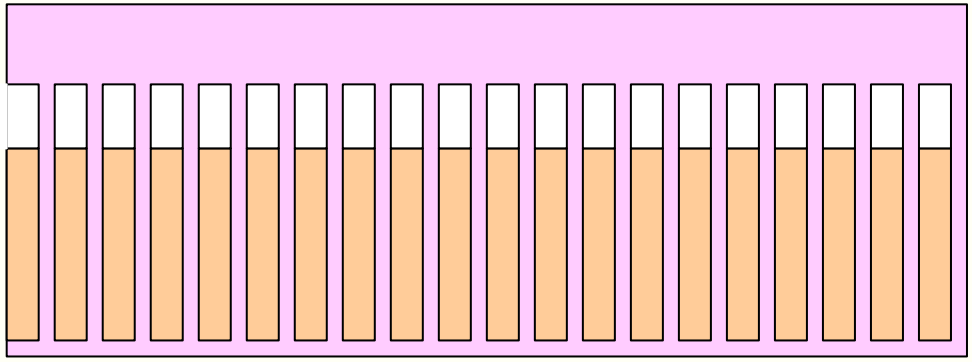
External Side:
20 x 16
AMP 8 points
connectors





option with
J0 transition
connector

Internal Side:
20 VME 160 points
connectors



- Passive backplane; controlled impedance traces
- Need some mechanics to hold (heavy) cables

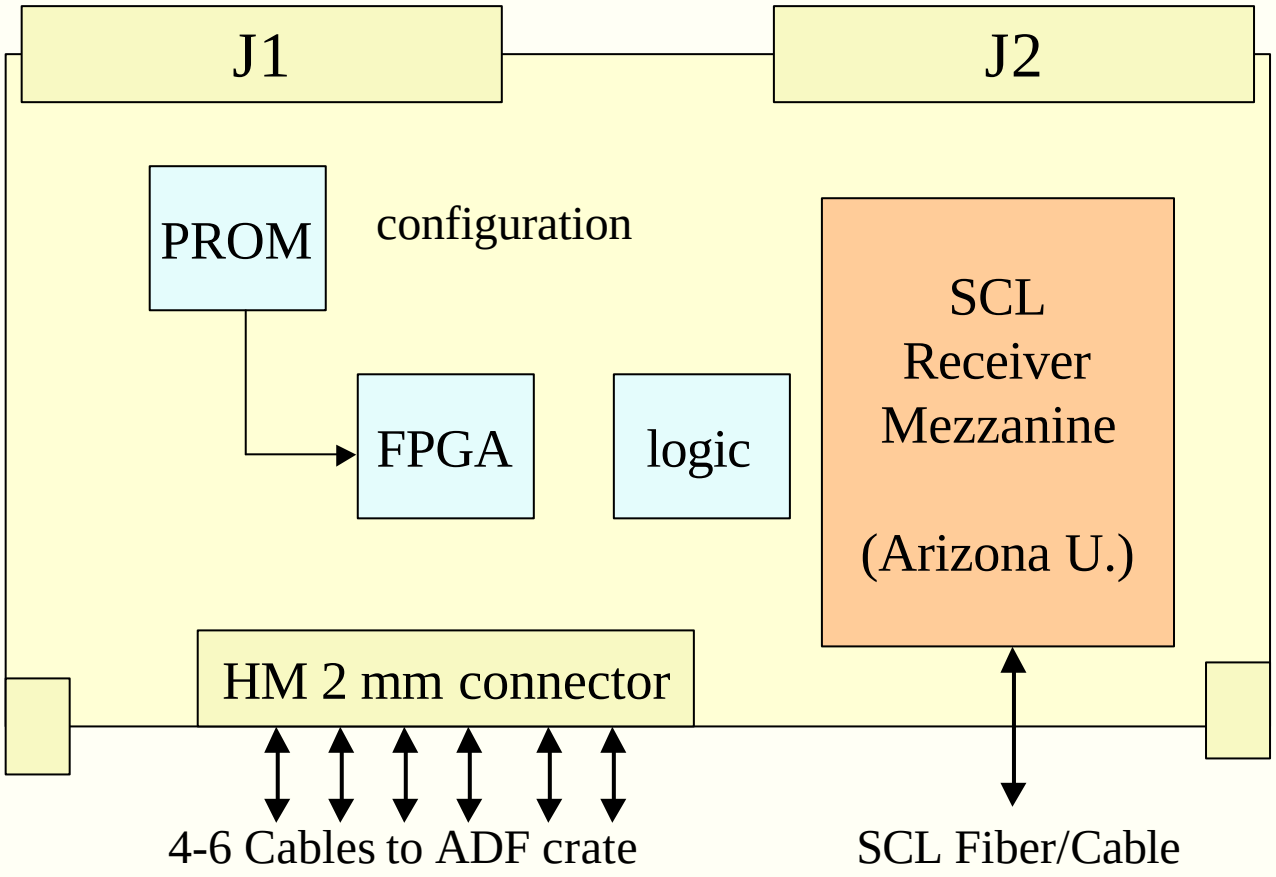
Power Estimation

- FPGA Core 1.5V
  - 3.2 A per ADF board

  -> converted from +5V with DC/DC @85% eff.: 1.2 A / board 23 A /crate
- Logic 3.3 V
  - 0.75 A per board

  -> converted from +5V with DC/DC @85% eff.: 0.6 A / board 12 A /crate
- ADC 3.3 V
  - 2.8 A per board; 60 A per crate
- ADC driver –5 V
  - 0.6 A per board; 12 A per crate
- Crate requirement: +5V 45A; +3.3V 60A; -5V 12A

Timing Card



- VHDL design in progress
- 3U or 6U mechanics; No slow control
- No slot available in ADF crate: back of slot 0? Space in TAB crate?

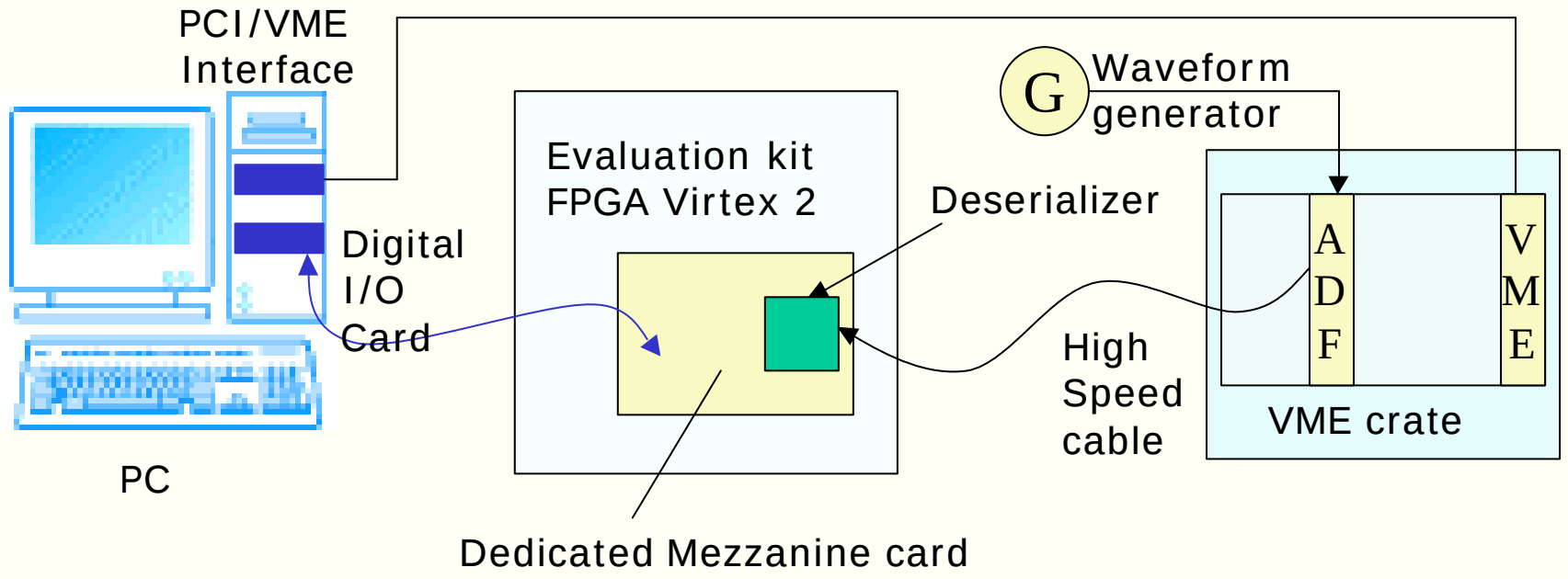
High Speed links

- Use 36 bit out of 48 available in Channel Link
  - 32 data bit
  - 1 start of frame bit (active when LSB's of data are present)
  - 1 indicator of frame length (8 bit or 10 bit)
    - Normal operation: 8 bit frames (digital filter output)
    - If L1 trigger and send raw data enabled: burst of N frames of 10 bit (raw ADC samples for that trigger)
  - 1 BX count
    - Normal operation: counter from SCL; 1 to 159
    - When sending raw ADC samples: send BX Count and Turn Count
  - 1 parity bit

- Operating mode of channel link? DC balanced or not? Deskew?

- Cable:
  - HM 2mm 8 or 10 pairs
  - No progress since last report

Test bench ADF board



- Standards items + dedicated mezzanine card(s)
- Requested summer student for design in 2003

  -> Need PCI/VME interface; EISA/VME unusable (EISA obsolete and not found in PCs for few years)

Software

- Address map: each ADF crate takes full 16 MB space of VME A24
  - need map 4-5 16 MB windows of VME A24-D16/08 in PCI space of TCC computer

A23 –A 19	A18	A17-A16	A15-A13	A12-A0
ADF Card ID	0	FPGA ID	Channel ID	Registers & LUT
	1	0 0	Config. PROG_B and CS_B	
		0 1	Config. DATA	
		0 1	Config. RD_WR_B, CCLK	
		0 1	Config. INIT_B, DONE, BUSY	

- Compatibility and smooth integration with existing TCC software
  - OS : Windows NT/2k? Language: C, C++? Tool: Visual Studio?
  - Libraries: Rogue Wave? STL? Others…
  - Application: multi-threaded? Polling?
- Some code development started to perform board level simulation

Short Term Plans

- Test Analog Splitter
  ~1 week
- Complete ADF board level simulations
  ~1 week
- Design power supply circuit for ADF board FPGA's
  ~2 weeks
- Start ADF board schematic capture
  Begin ~end October at best