Nevis Design Status: Summary

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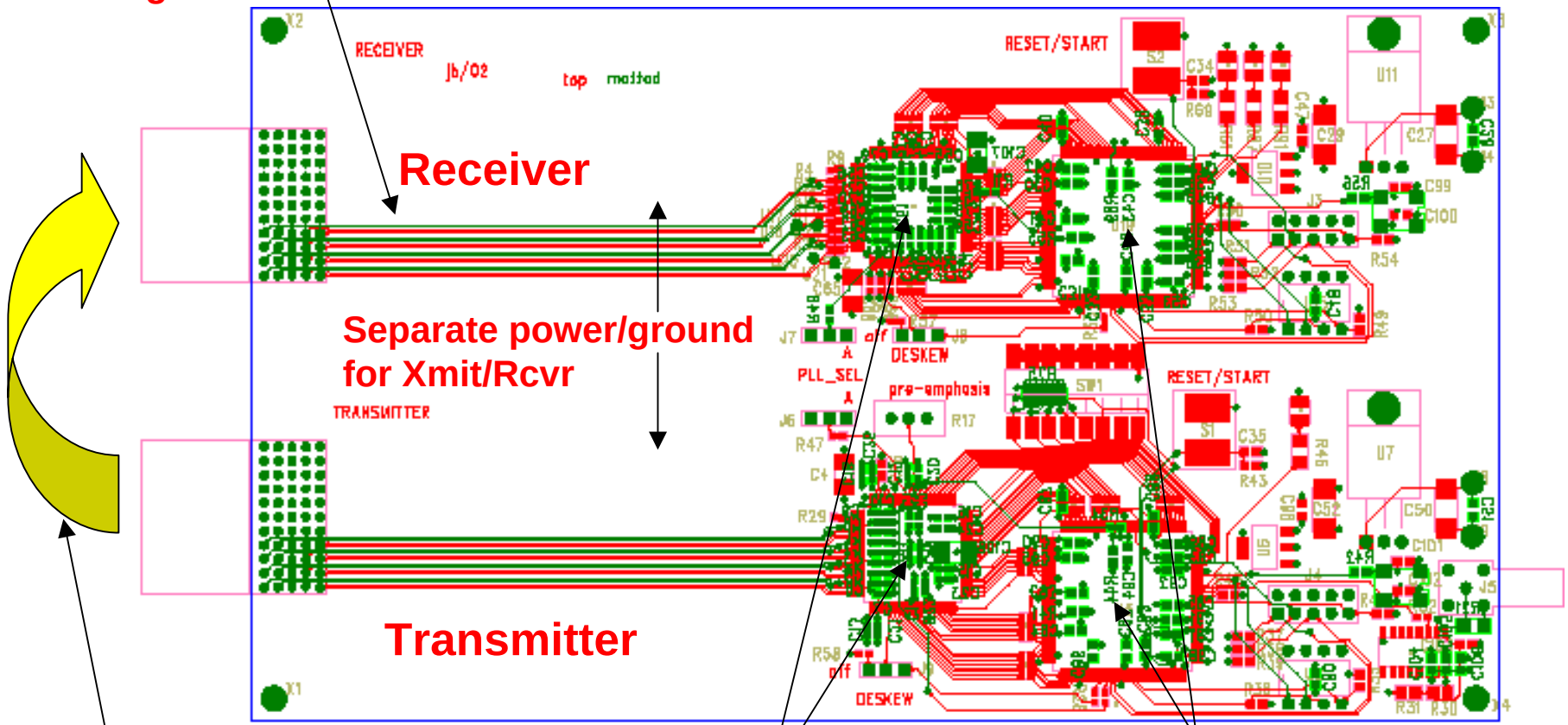
- **Trigger Algorithm Board**
  - **Done**
    - **Jet, EM & Tau Sliding Windows algorithms coded & simulated on Stratix (EP1S10 –6)**
    - **Input section lay out finished**
      - **3 x 48-8 Channel Link Deserializers + Filtering + Stratix for 2 input connectors**
  - **To Do**
    - **Final input data protocol**
    - **Global Chip firmware (concentrates/formats TAB output)**
    - **L2 Data output**
    - **Cal-Track output section**
    - **Monitoring**
- **Global Algorithm Board**
  - **Detailed design not yet started**
    - **waiting for TAB design to finish**
- **Test of ADF-to-TAB data Transmission Scheme**
  - **Essential to verify this to proceed with TAB design**

ADF-to-TAB Cable Tester

Trace length as in TAB



5m Cable/Connector

- AMP 621410-6 (4x5 rows)

Channel Link: xmit/rcvr

- DS90CR481/484: 48-8 (with filtering)

FPGAs: data resynch.

- diff. clocks from Chan Link

Cable Test: First Results

- **Completed Cable-Test Board on 30-Sep**
- **Preliminary Tests**
  - **Eye Pattern** — **good**
  - **Error Free Xmit over freq range** — **30-120 MHz**
    - **our operating point = 60.6 MHz**
    - **corresponds to data rate on cable: 210-840 MHz**
  - **DC balance** — **works**
  - **De-skew Feature** — **works**
  - **Voltage drive strength adjust** — **works**
  - **Long Term Running** — **few hours @ 90MHz w/out error**
- **So Far – no problems observed !**
- **More Thorough Tests Planned**
  - **systematically explore entire parameter space of system**
    - **Frequency, V-drive strength, Common Mode Shifts, DC-balance, De-skew,…**
  - **check bit error rate: spec sheet ~ 10^{-12}**
  - **look for break points**