
# Status of ADF System Design November 2002

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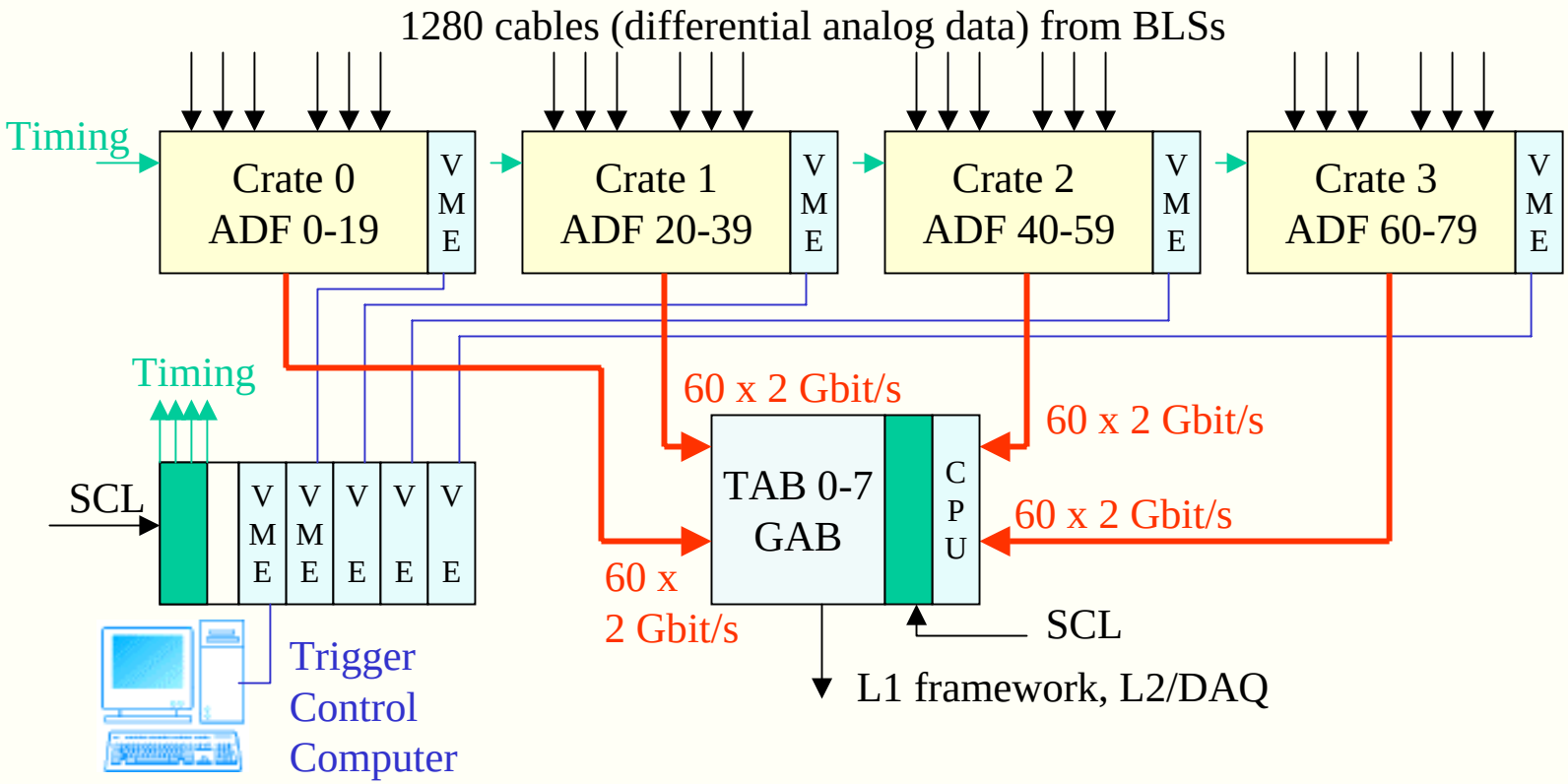
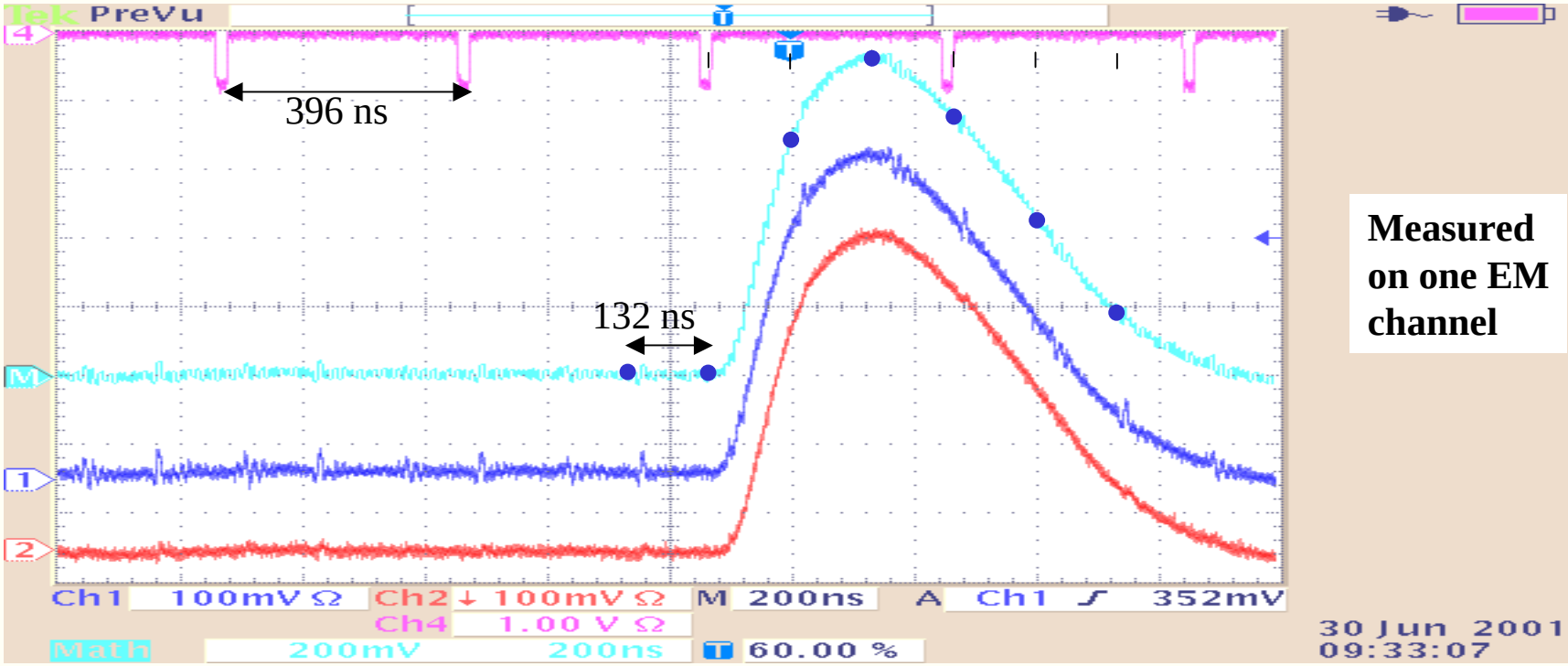
- Algorithm and Simulation
- Analog Splitters
- ADF board
- ADF crate
- Timing card
- Test bench
- Software
- Summary

# ADF System




- 32 analog channels + 3 (ou 1?) output 2 Gbit/s per ADF board
- 20 ADF boards+ 1 interface per crate (« VME Interconnect »)
- 80 ADF boards in 4 VME crates in total
- 1 board for timing distribution

# Trigger Pickoff Signal




**Measured on one EM channel**

- Rise time too long for operation at 132 ns:

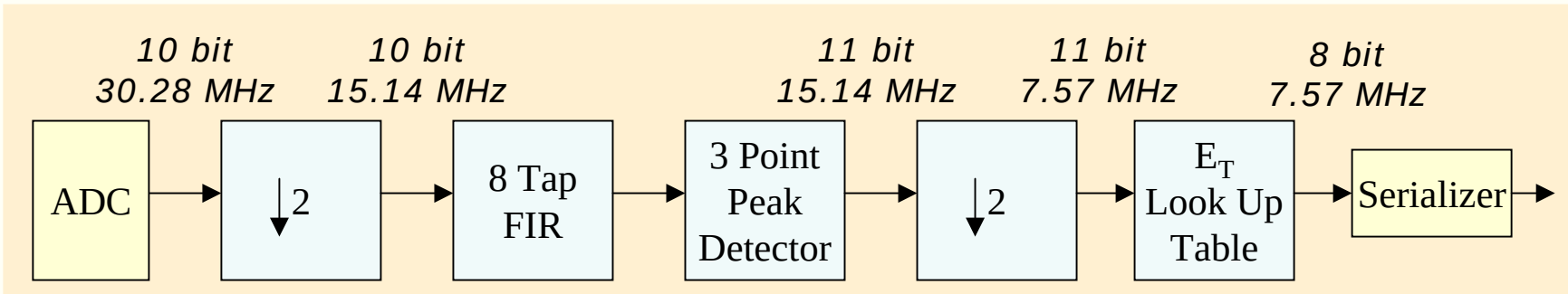
  *Let E=energy deposited for BC #N: 75% of E observed at BC #N-1: can cause fake trigger at BC #N-1 that causes a veto for BC #N which is lost!*
- Long tail: 80% of max after 132 ns; 20% after 396 ns

  *-> Digital Signal Processing*

# Algorithm

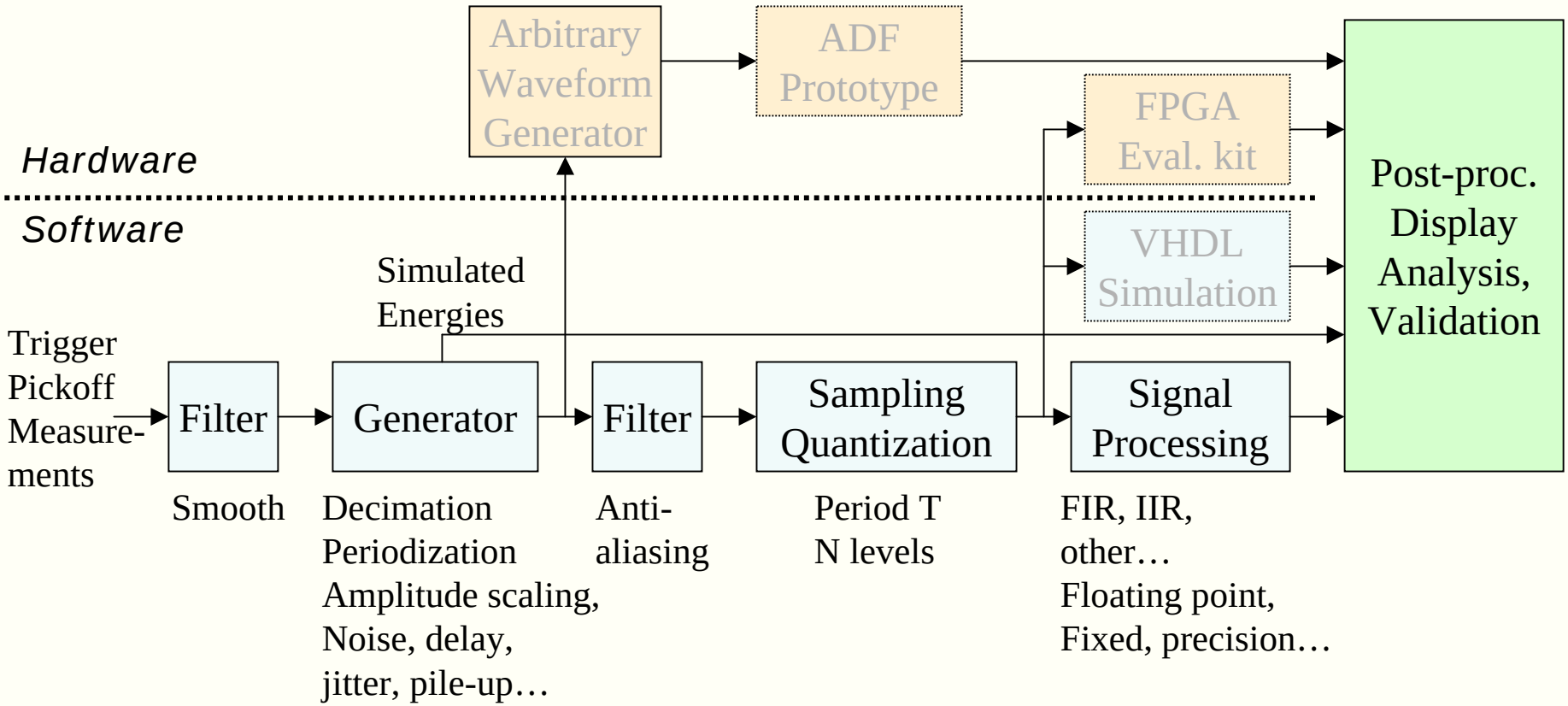
- Algorithm unchanged since Nov. 2001 studies
- Close to what is done in other experiments:
  - ATLAS and CMS: 5 tap FIR @ BC frequency + 3 point peak detector + some logic for saturated pulses
  - Proposal for D0: up to 8-tap FIR @ BC x 2 frequency + 3 point peak detector

    -> very conservative wrt rate and number of taps



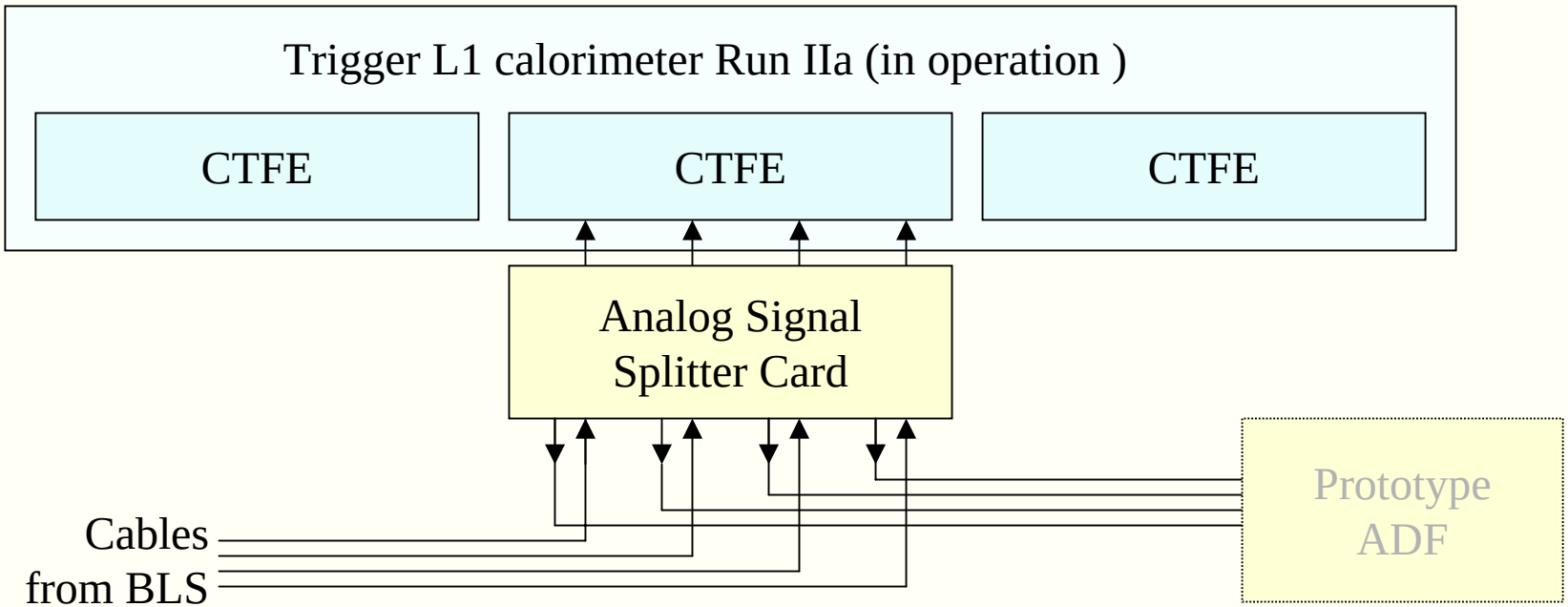

- VHDL coding completed and simulated
- 8 channels fitted in FPGA Xilinx Virtex II 500K gates 456 pins

# Simulation Chain




- Largest part of software operational
- Some improvements to make; work on coherence with VHDL simulation results

# Analog Signal Splitter Card




- Active board for duplicating differential analog signals from 8 trigger towers
  - Collecting raw data samples
  - Test of ADF board prototype in parasitic mode

# Analog Splitter

- One board cabled
  - *Minor error found:*
  - *DC/DC converter need to be soldered on other side of PCB due to top/bottom view inversion*
  - *Missing thermal drain below operational amplifiers*

  *-> Corrected PCB not mandatory but will be done*
- Test bench

  *- quickly made differential source (AD829), cables and adapted loads*
- Preliminary tests (sinus input)
  - *Connector pinout is correct, all channels work; gain is correct*
  - *Bandwidth: over 10 MHz*
- More tests needed

  *- arbitrary waveform generator*
- Schedule for installation in D0?

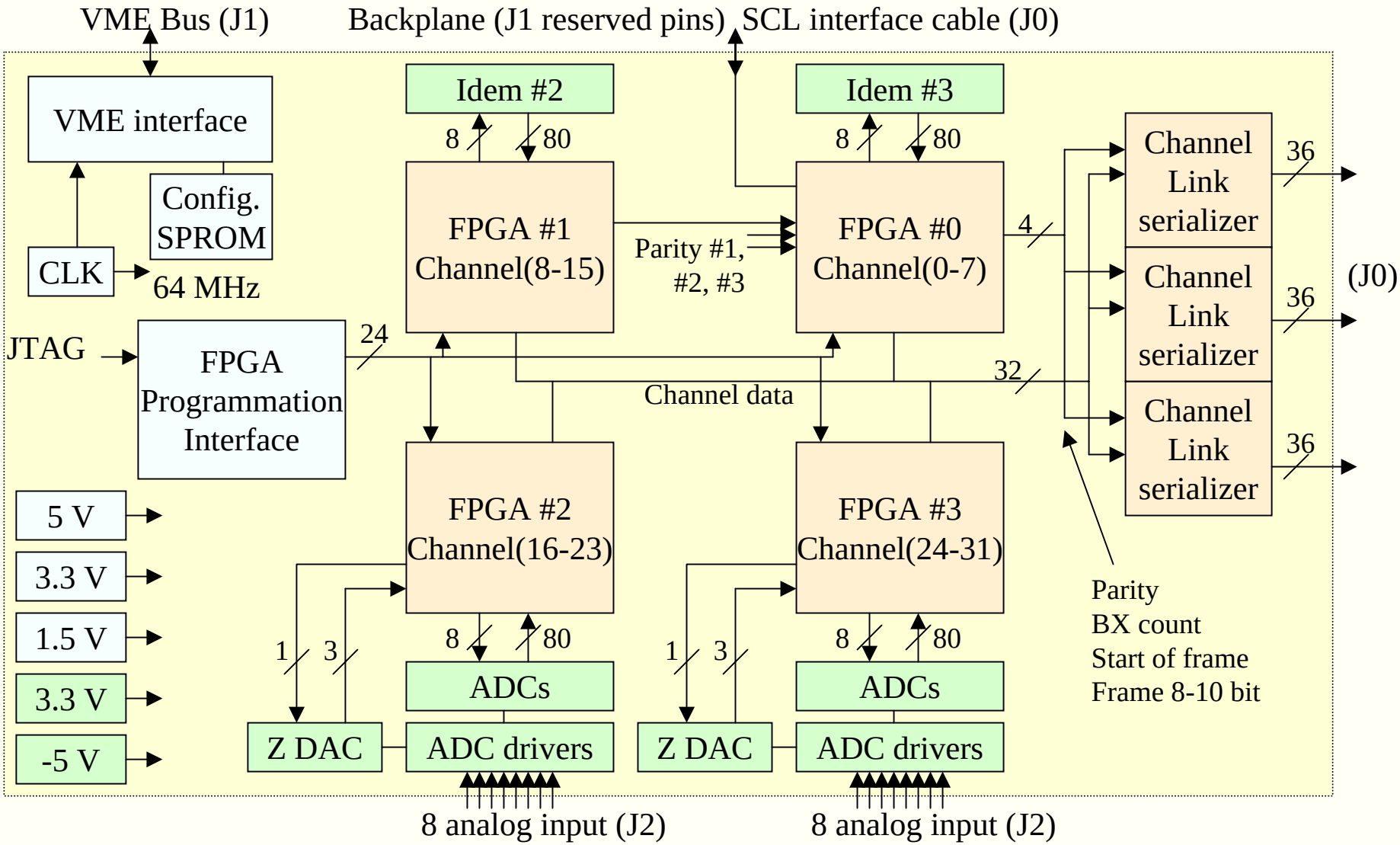
# ADF Board Status

- Core FPGA (digital filter)
  - *VHDL coding 100% completed and simulated*
  - *8 channels synthetized, fitted in XC2V500 FG456 -4*
  - *Post-route simulation done*
- VME interface and bootstrap interface
  - *VHDL coding 100% completed and simulated*
  - *Programmable logic fitted in XC9572XL –10 TQ100C CPLD*
- Board-level VHDL simulation
  - *Includes 4 FPGA's + VME interface + bootstrap logic*
  - *Started for behavioral model*
  - *Some control software was developped to exercice the VHDL model*

  *-> Several errors in the FPGA logic were found and are being corrected*
- Schematic capture: will start in November 2002, although board level simulations not 100% completed

  *- Aim for PCB designed ~end January 2003*

# ADF board Block Diagram

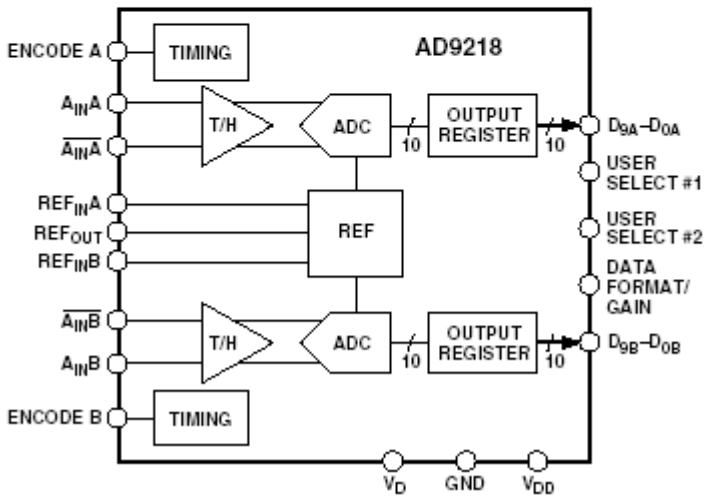


# ADF Channel Analog Section

## 10-Bit, 40/65/80/105 MSPS 3 V Dual A/D Converter

**AD9218**

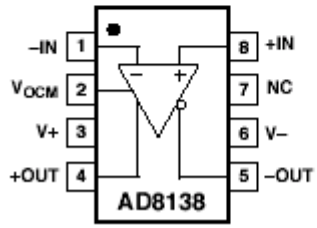
FUNCTIONAL BLOCK DIAGRAM




## Low Distortion Differential ADC Driver

**AD8138**

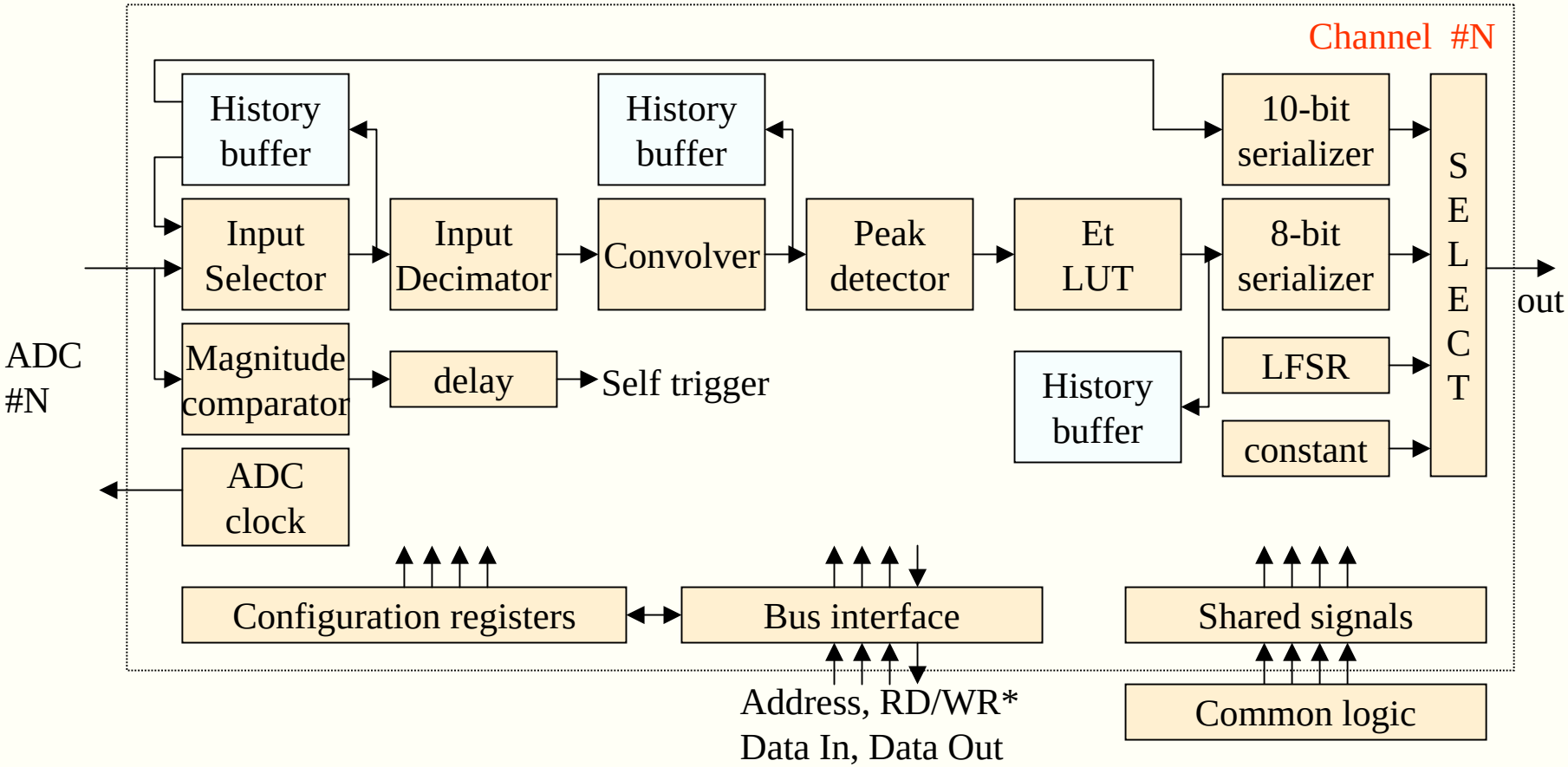
FUNCTIONAL BLOCK DIAGRAM




NC = NO CONNECT

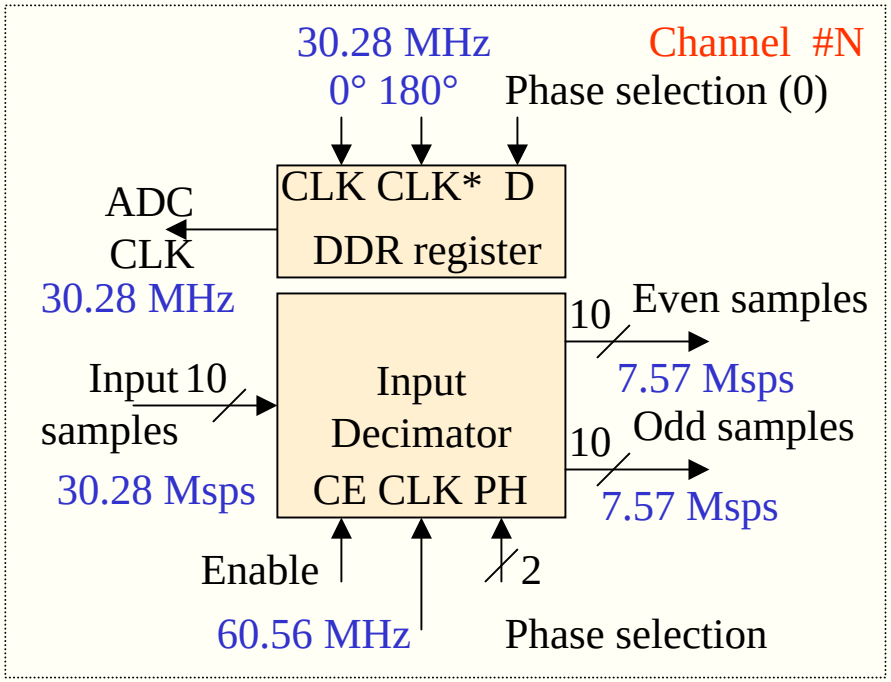
- Design in progress…:
  - Digitization with 10-bit precision, identical input range for all channels
  - Passive RC filter for anti-aliasing; Octal DAC MAX5307 for zero adjust

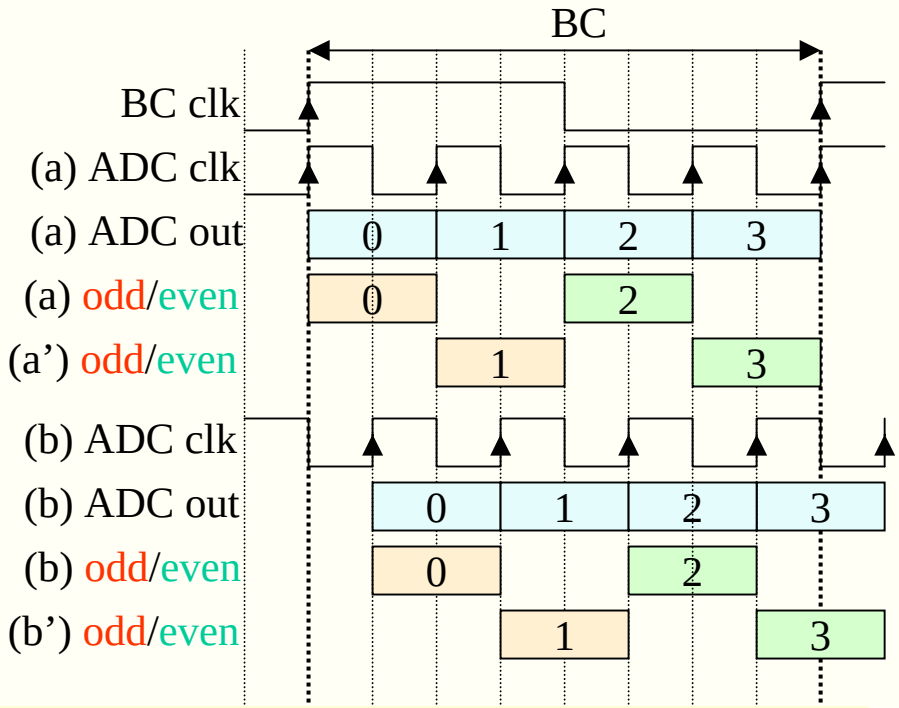
# ADF Channel Digital Section




- Logic duplicated for each channel + common logic for channels within the same FPGA

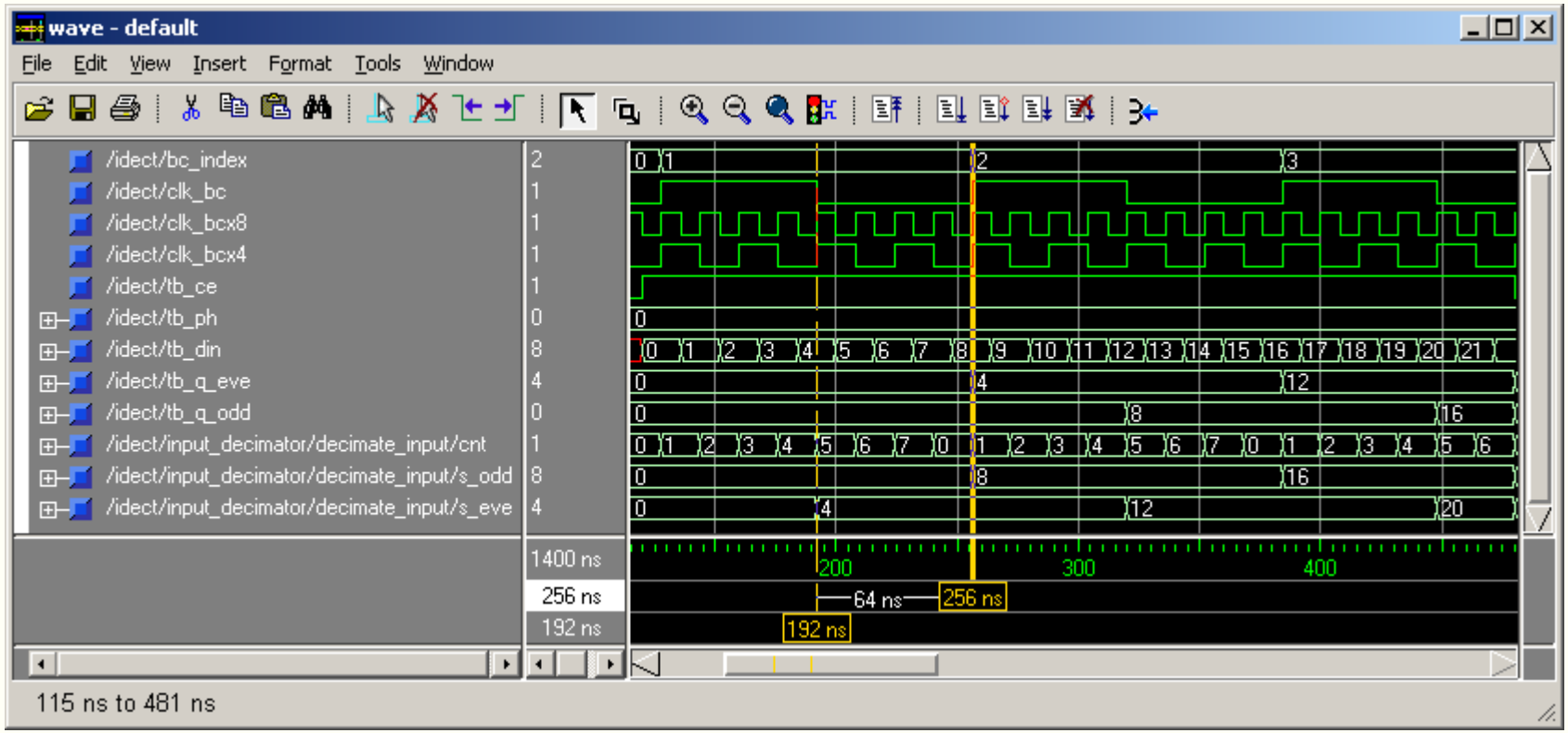
# Input Decimator and ADC Clock



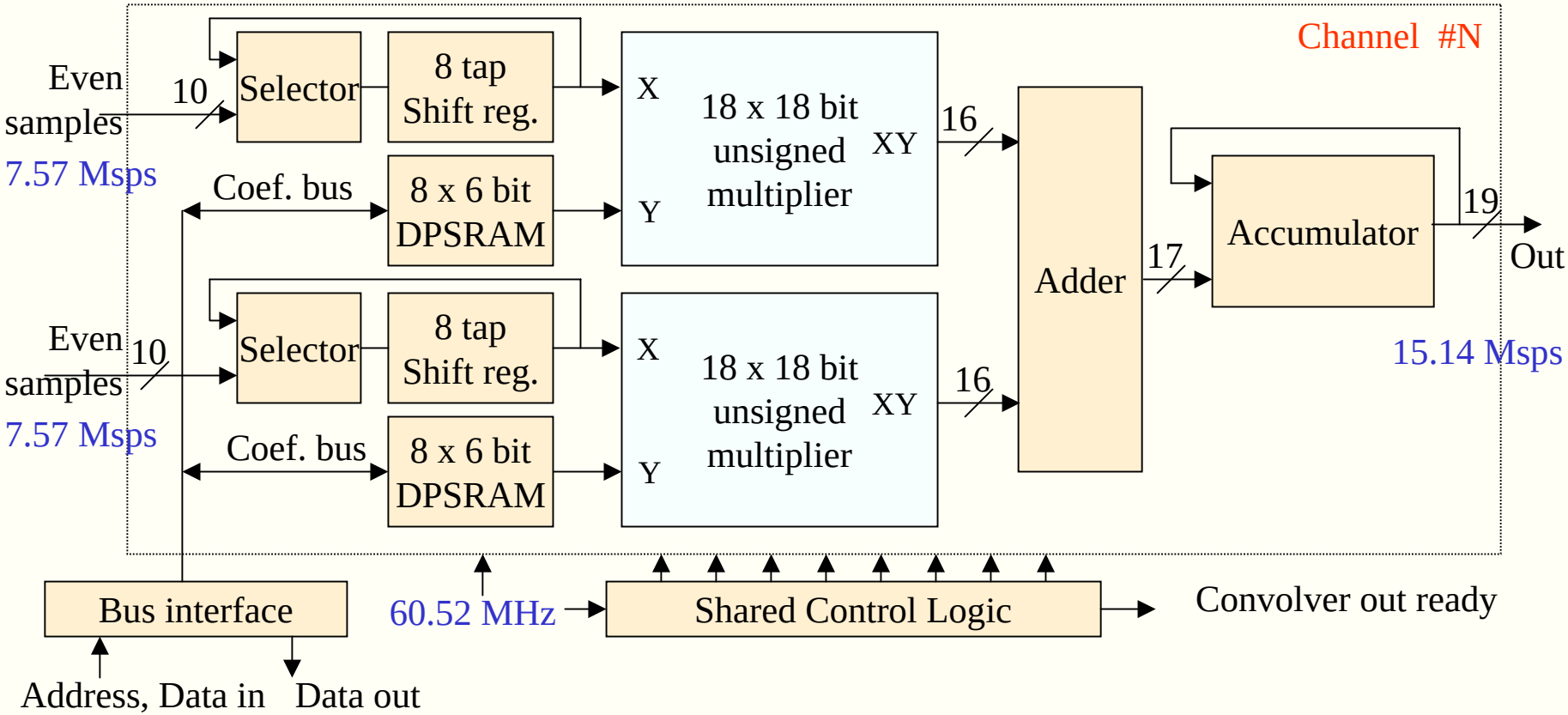

- ADC Clock:
  - *Copy or inverted copy of internal 30.28 MHz clock made with DDR reg.*
- Input decimator
  - *Keep 2 samples per BC out of the 4 converted depending on phase selection*
  - *4 possible phase value: phase adjustment 1:8 BC i.e. 16.5 ns*
  - *Samples output on 2 parallel stream to interface to dual-branch convolver*
  - *Decimation done with constant latency wrt BC clock*

# Input Decimator and ADC Clock



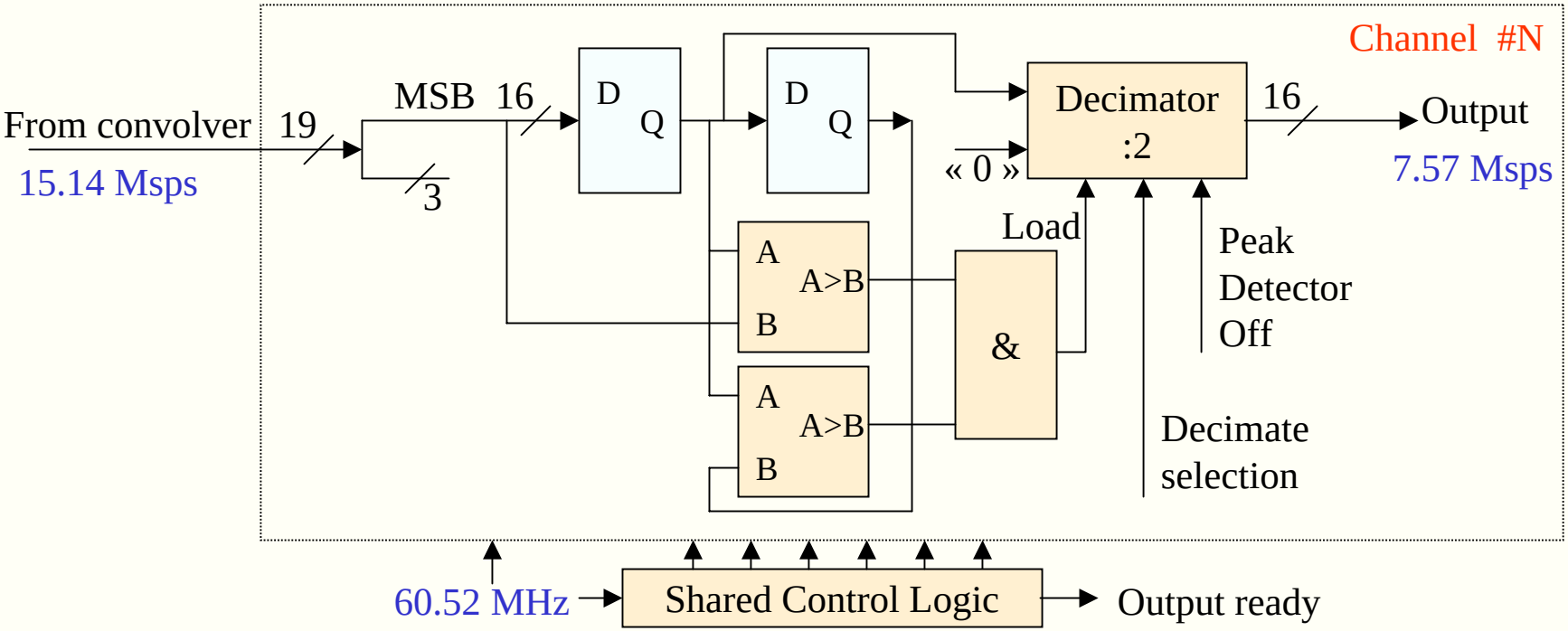

- E.g. Phase Selection=0; BC period = 128 ns:
  - *Samples 0, 4, 8, 12, 16 … are selected*
  - *Samples 0, 8, 16… on q_even with latency of 0.5 BC wrt rising edge of clk_bc*
  - *Samples 4, 12, 20… on q_odd with latency of 0.5 BC wrt rising edge of clk_bc*

# Convolver



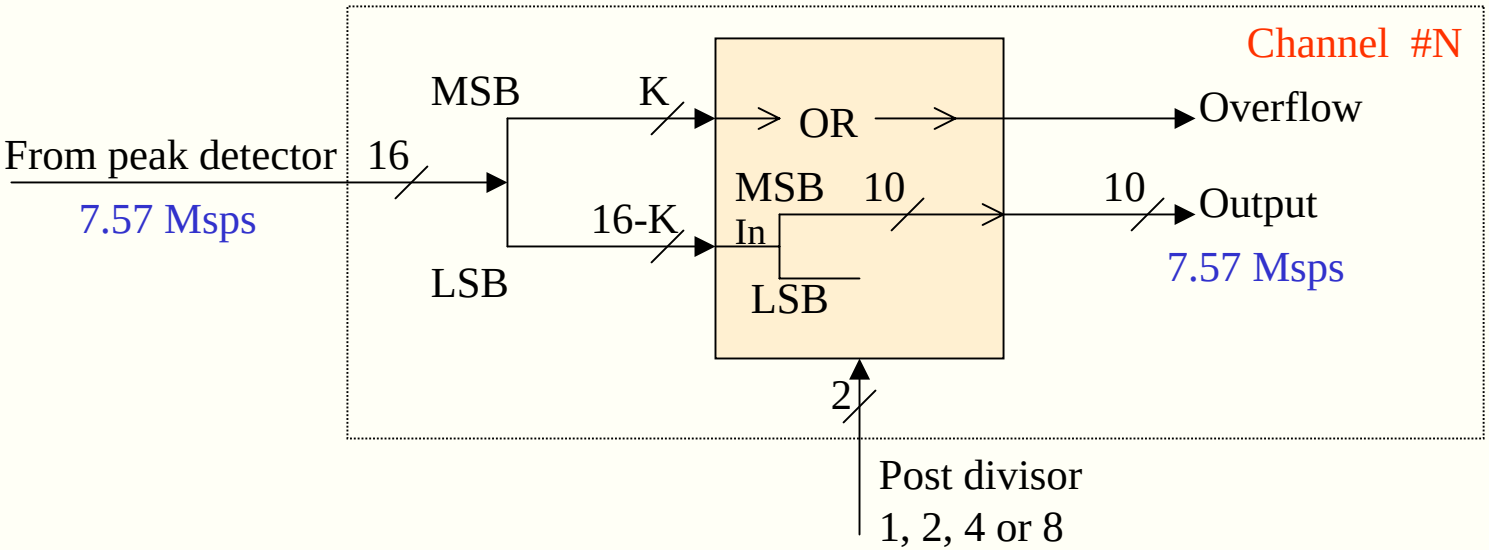

- Dual-branch convolver:
  - faster : 8 tap @ 15.14 MHz (*Single branch: ~4-5 tap)*
  - *But more work because no IP core. Anyway if Xilinx Coregen IP core: no generic size in VHDL code, control logic not shareable*

# Peak Detector Output Decimator



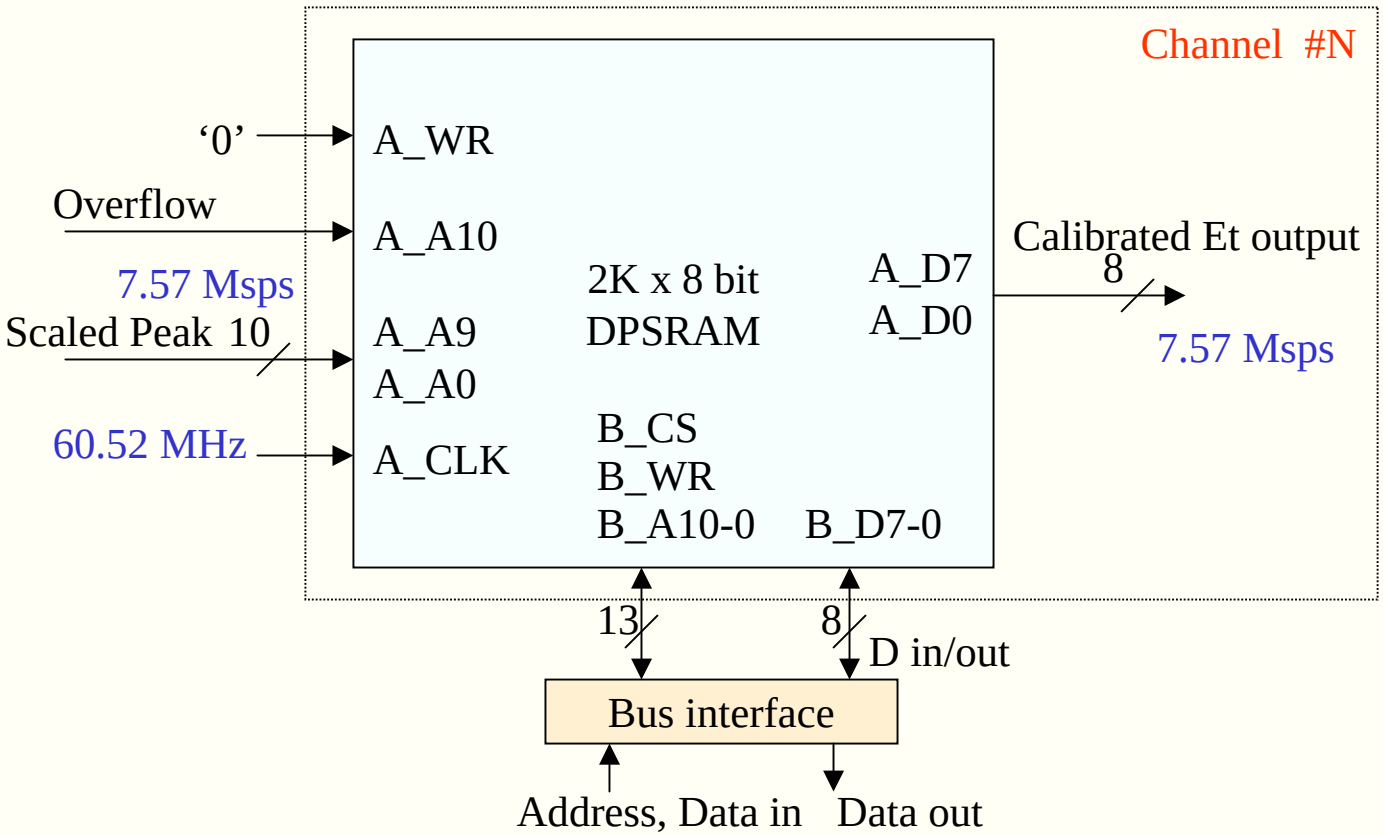

- 3-point peak detector followed by :2 decimator
  - Only 16 MSB of convolver output compared to save logic
  - Peak detector On/Off control
  - Keep 1 output out of 2 (2 possibilities) with constant latency

# Peak Detector Post Divisor



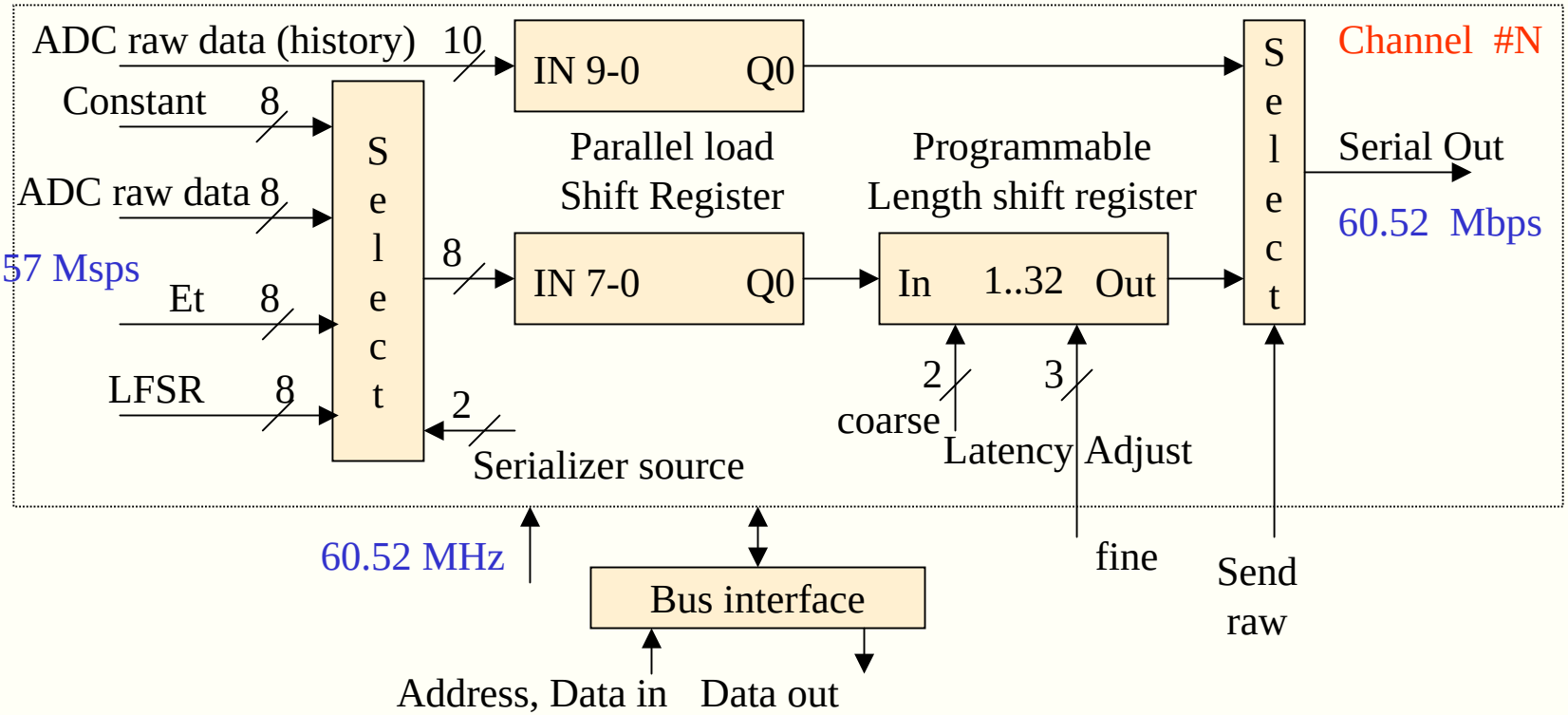

- Arithmetic right shift for result scaling
  - Programmable post divisor value: 1, 2, 4 or 8
  - MSB's that are lost are OR'ed together to make overflow bit
  - Stage in combinatorial logic

# Et Look Up Table



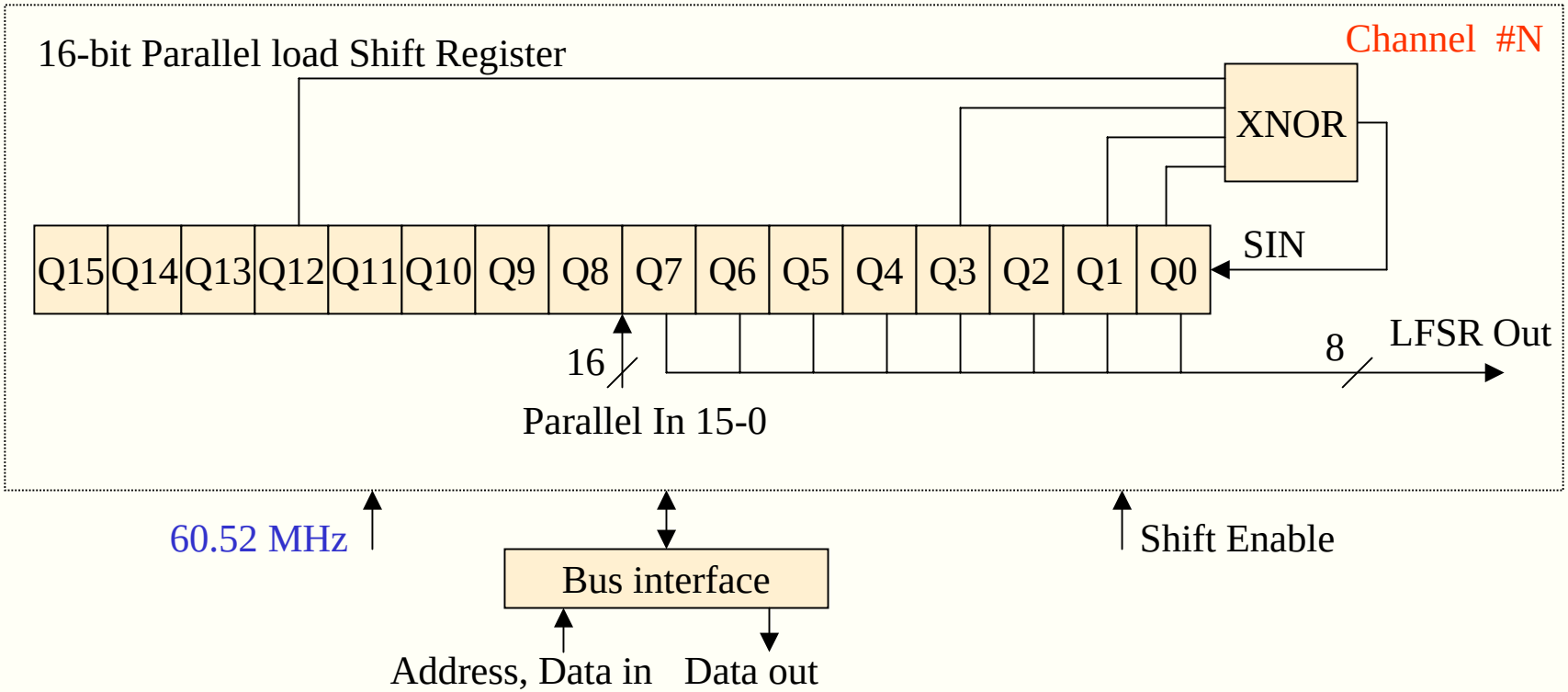

- Look up table for final Et result
  - Conversion from 10 bit to 8 bit Et
  - Arbitrary conversion function (e.g. implement clipping, saturation)
  - Programmable output value when arithmetic overflow (uses ½ LUT)

# Serializer and Latency Adjust



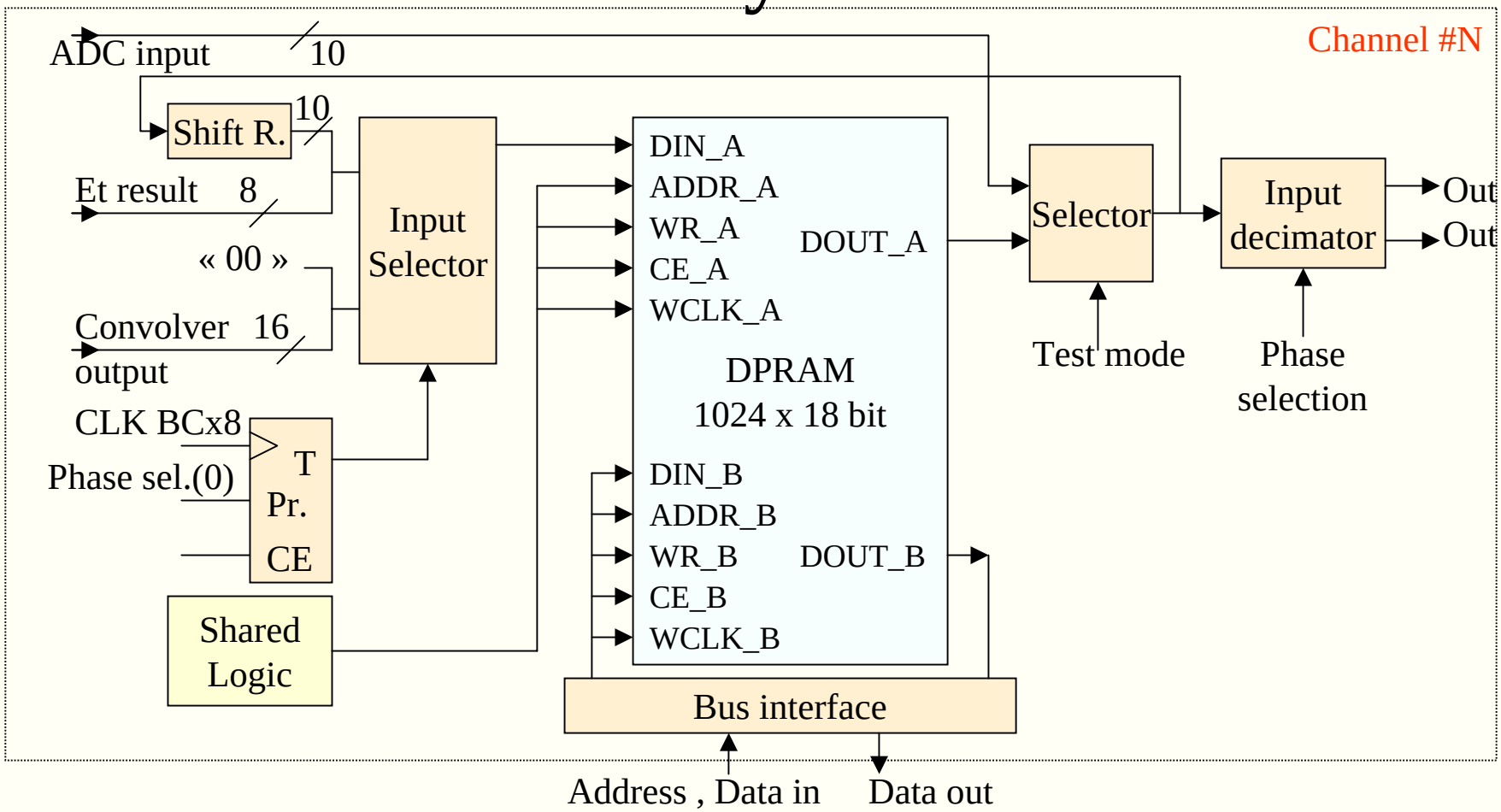

- 4 possible sources of data for 8-bit serial stream
  - 8 MSB of ADC value, Et result, Constant value, pseudo-random value
- Switch to 10-bit frames when sending raw ADC samples
- Per channel coarse latency adjust (+0 to +3 BC); common fine adjust (+1/8 BC to +7/8 BC)

# LFSR



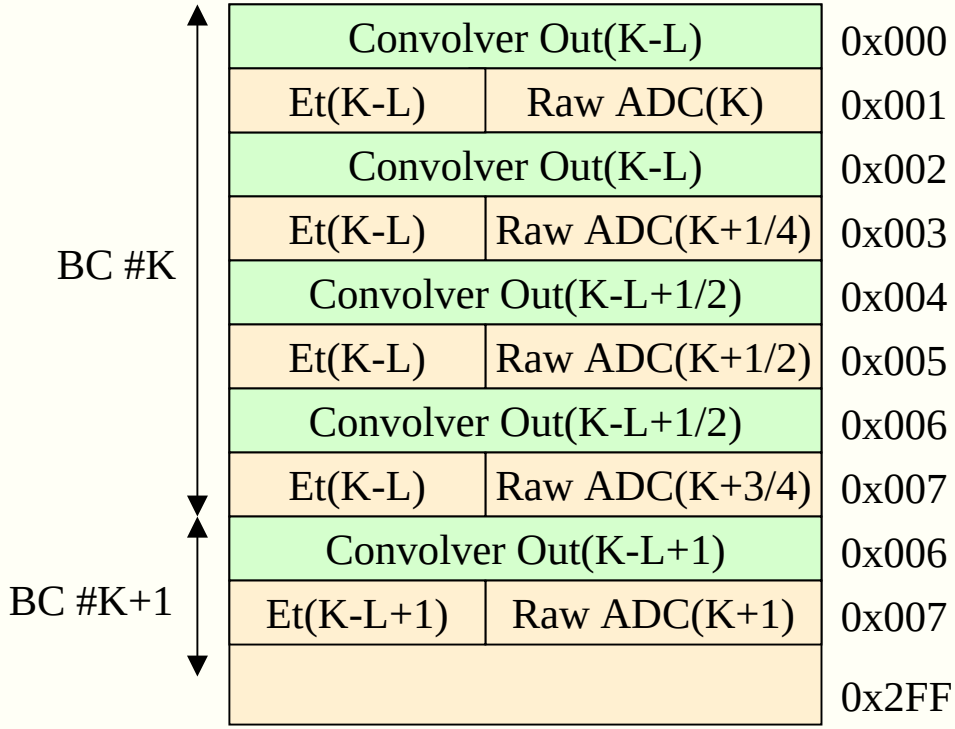

- 16-bit pseudo-random generator
  - Per channel programmable seed
- 8 LSB's can be sent to ADF output serial stream
- Common shift enable for inter-channel synchronization

# History Buffer




- History buffer used for test mode without ADC input:
  - *Play at input of digital filter digital values pre-loaded via bus interface*

# History Buffer Usage

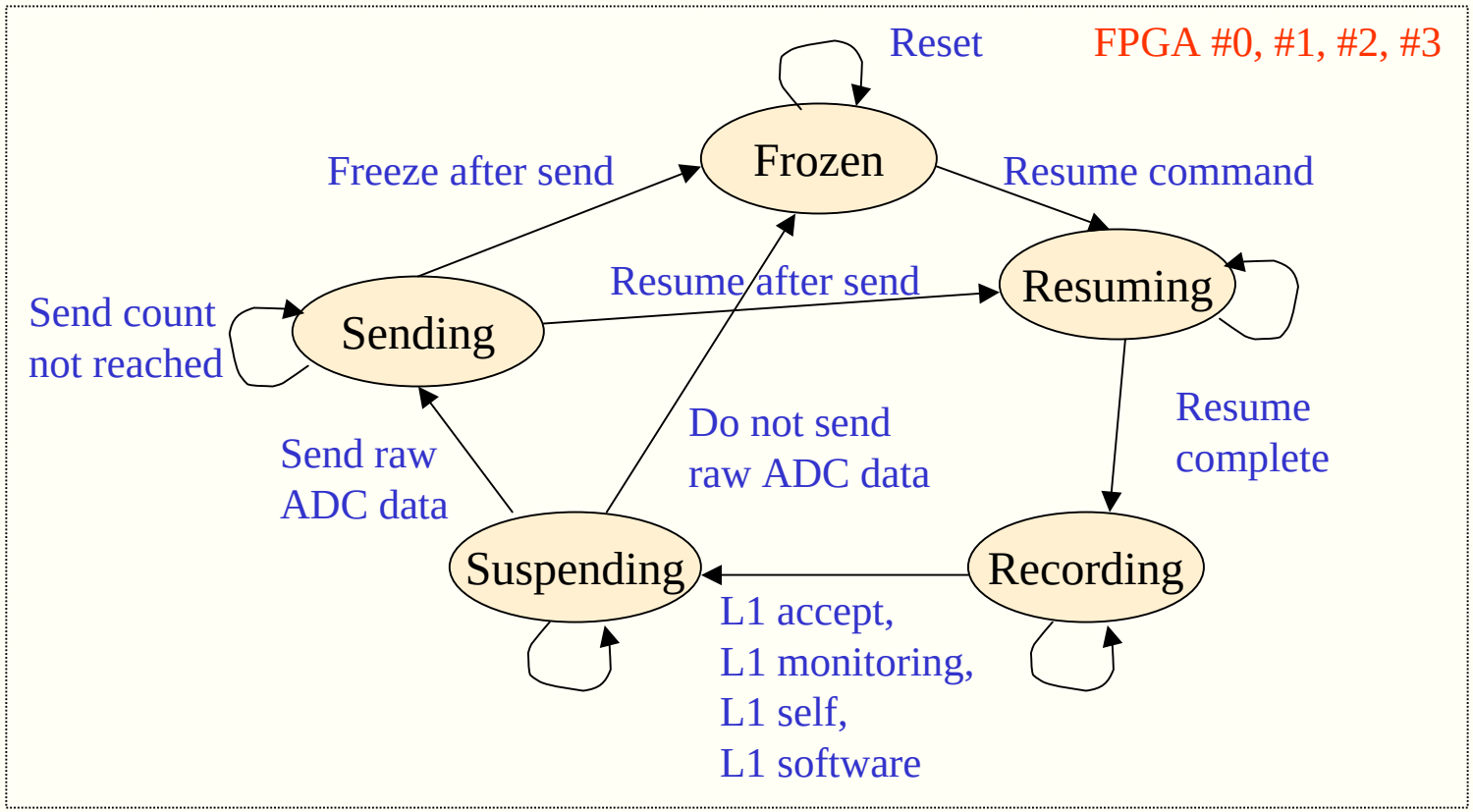



Memory content shown for for phase selection = 0 or 2

For phase selection = 1 or 3, the content of odd and even addresses is exchanged

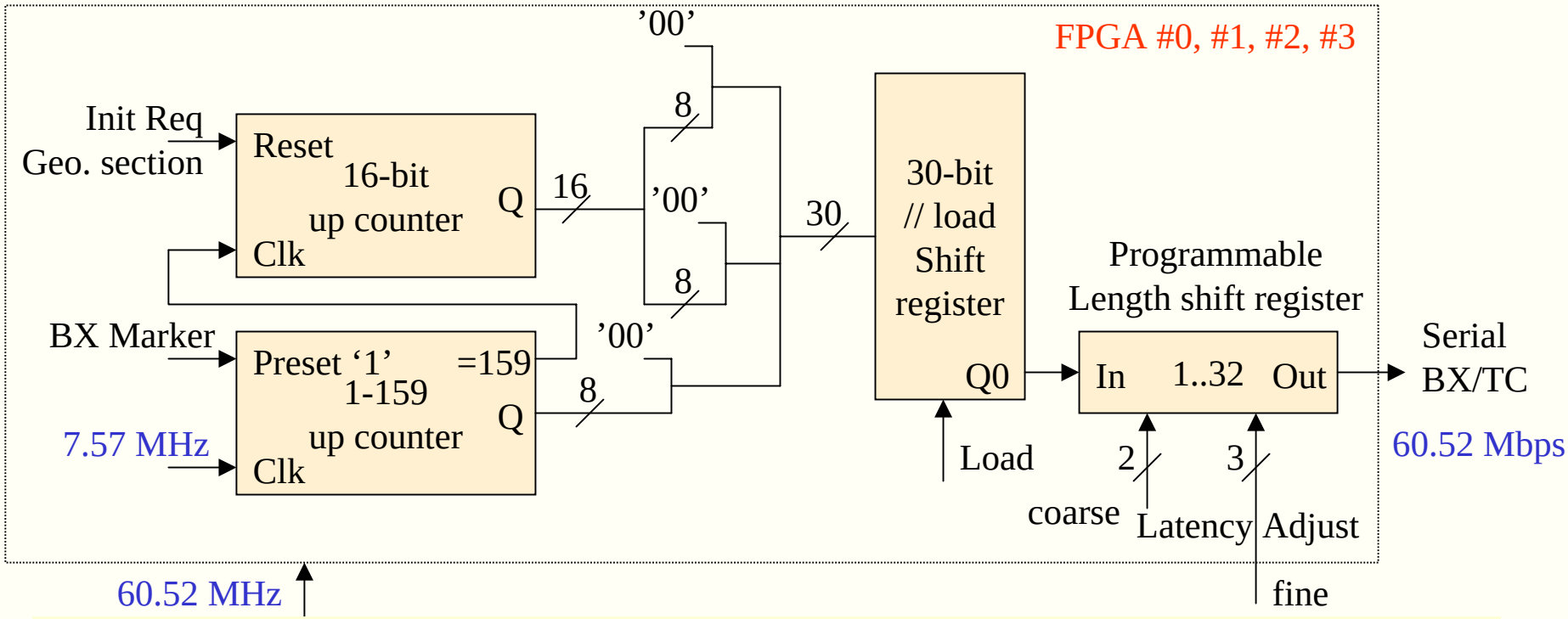
- Shared 1024 x 18 bit SRAM written at BC x 8
  - 512 x 10 bit: raw ADC sample (sample change at BC x 4)
  - 256 (x 2) x 16 bit: convolver output (result change at BC x 2)
  - 128 (x4) x 8 bit: Et filtered output (result change at BC x 1)

# State Machine for raw sample RAM



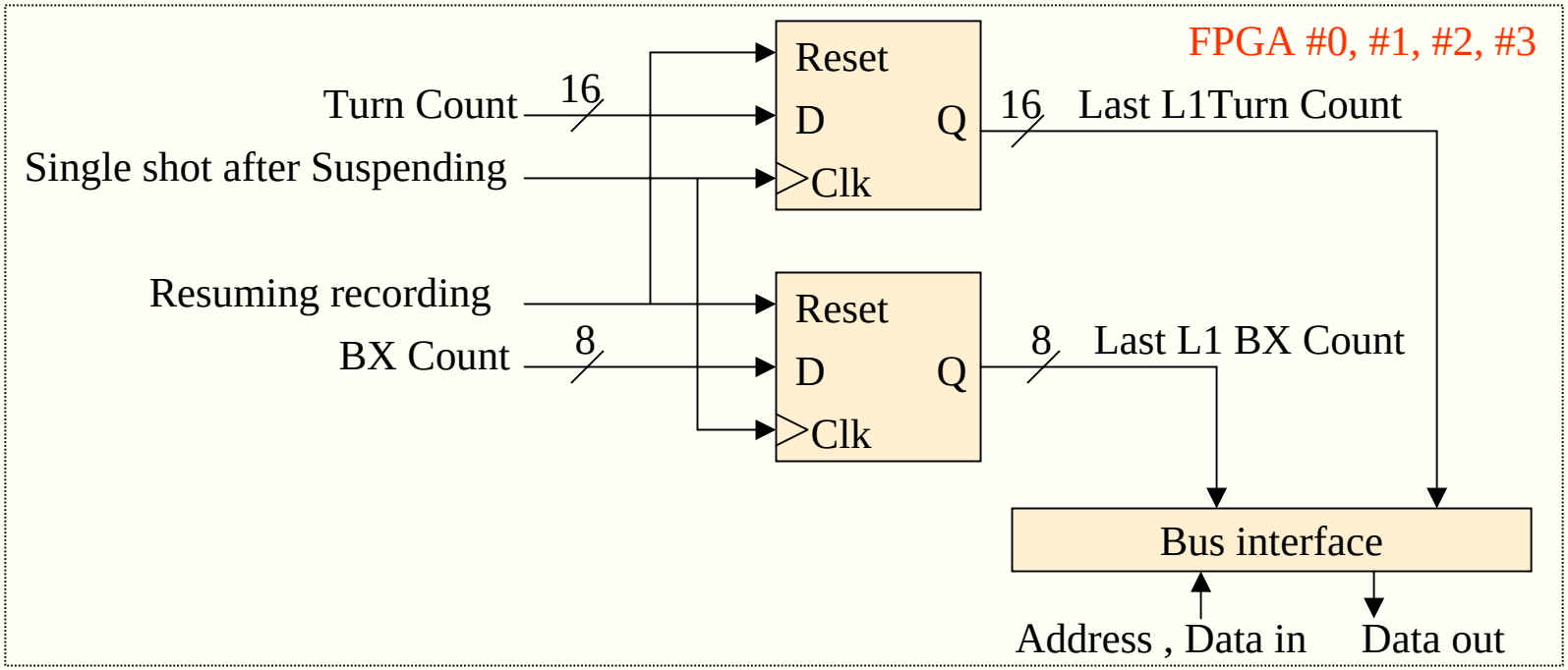

Resume after send: if L1 accept and none of L1 monitoring, L1 self, L1 software flags
Freeze after send: if any of L1 monitoring, L1 self or L1 software flags
L1 accept, monitoring, self, software are previously ANDed with corresponding mask flag

# BX and Turn Count Serializer



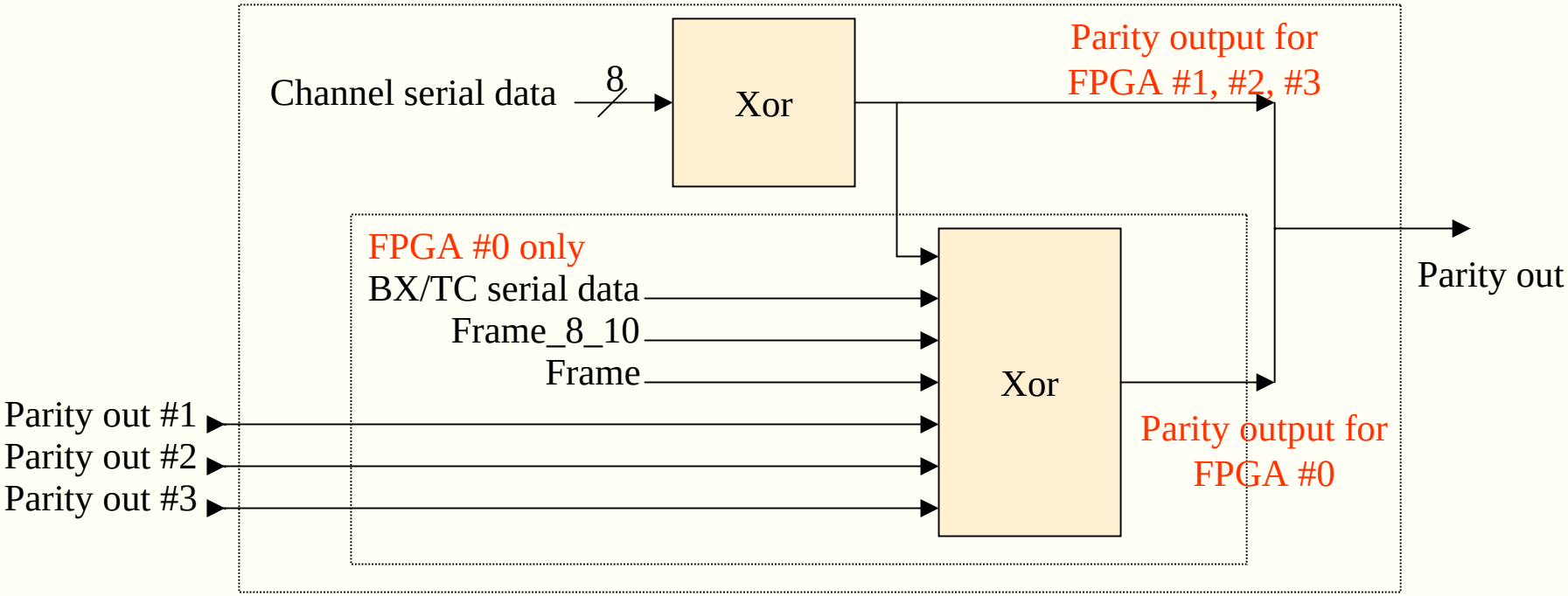

- When sending 8-bit frames to TAB:
  - Load activated every 8 ticks: serial stream is 8-bit current BX count
- When sending 10-bit frames to TAB:
  - Single shot on load: serial stream is: BX count, 8 LSB of turn count, 8 MSB of turn count; these 3 bytes are put in 10-bit frames (pad: 00)

# Last L1 BX and Turn Count



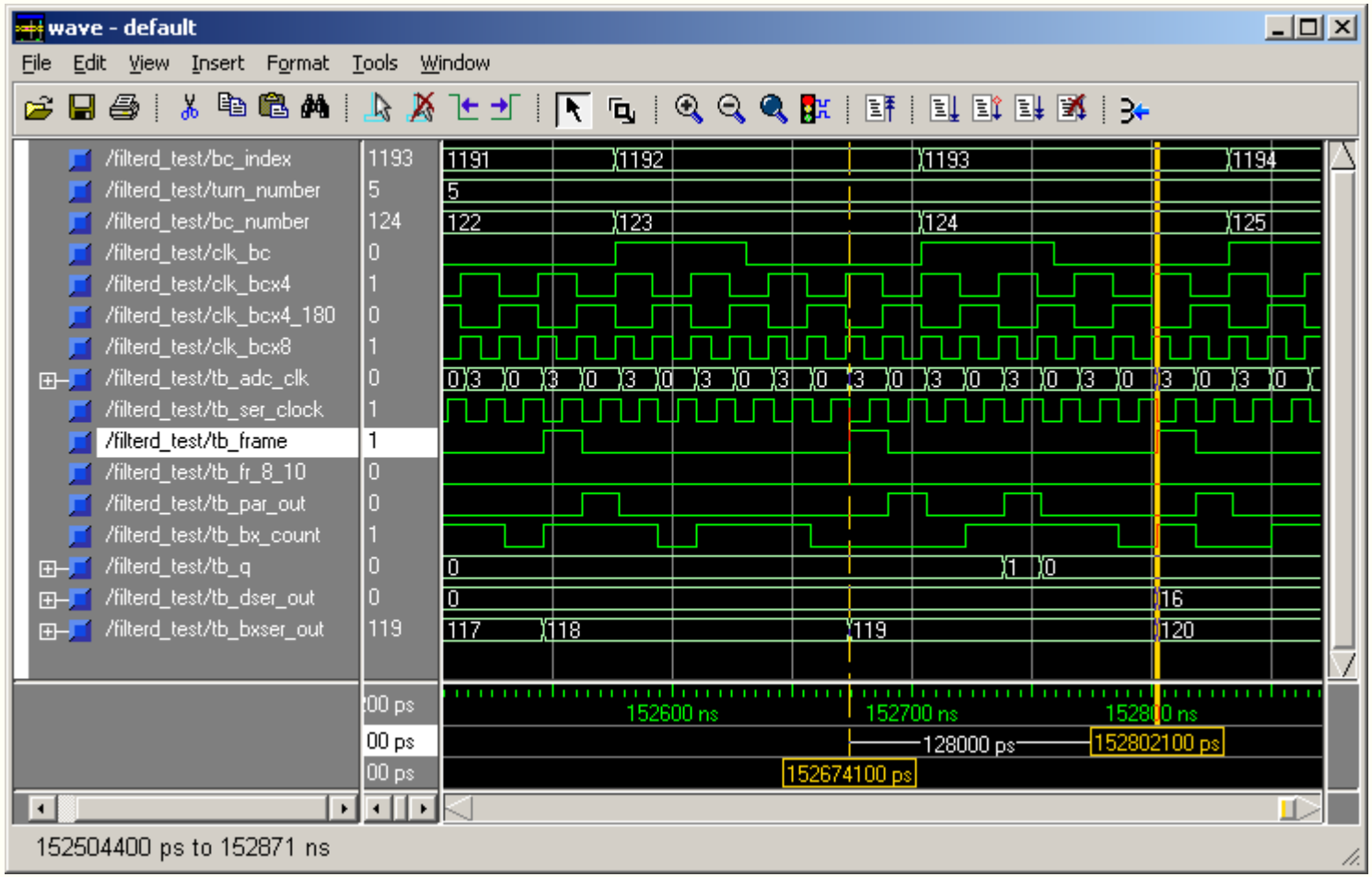

- After trigger causing raw sample recording to freeze:
  - Latch current BX and Turn count
  - Made available for read via bus interface
  - Reset occurs when raw sample recording resumes

# Parity Generation



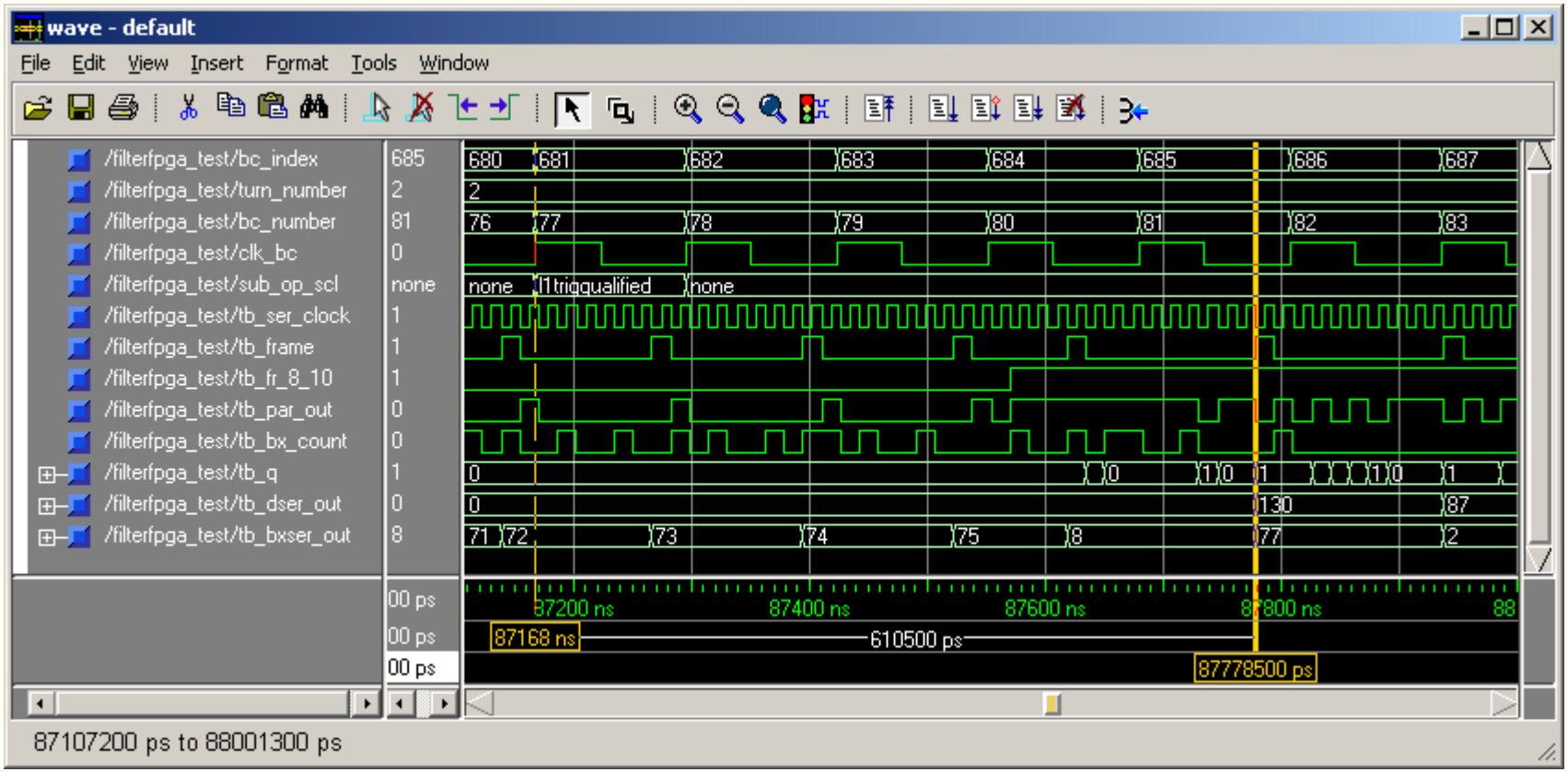

- Parity of 8 channel data calculated by FPGA #0, #1, #2, #3
  - Partial parity of FPGA #1, #2, #3 sent to FPGA #0
  - FPGA #0 computes global parity over 32 channels and ctrl signals
  - Global parity sent to TAB over Channel Link

# Start Of Frame



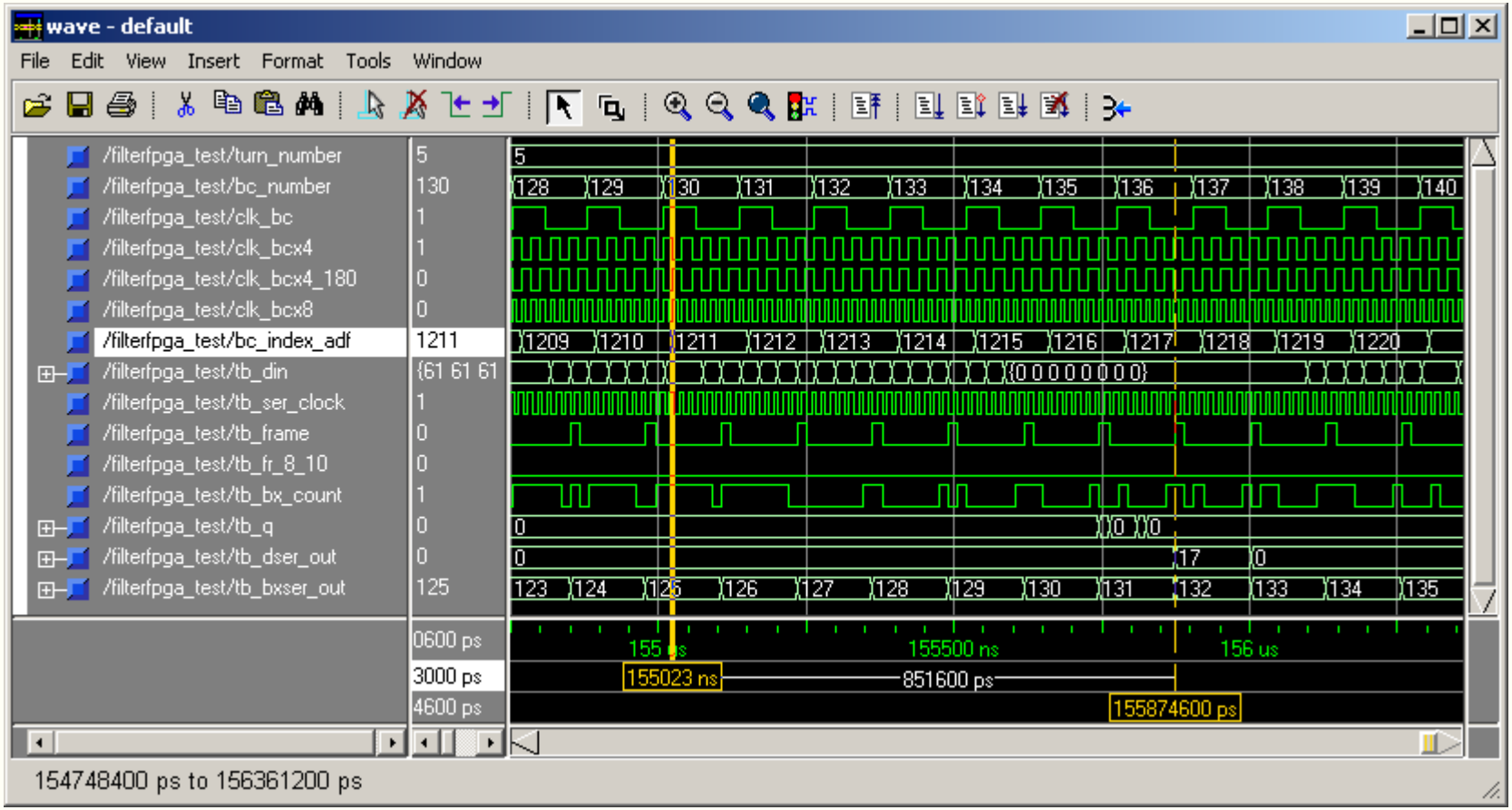

- Frame active when LSB of data is present on serial stream

# Frame_8_10



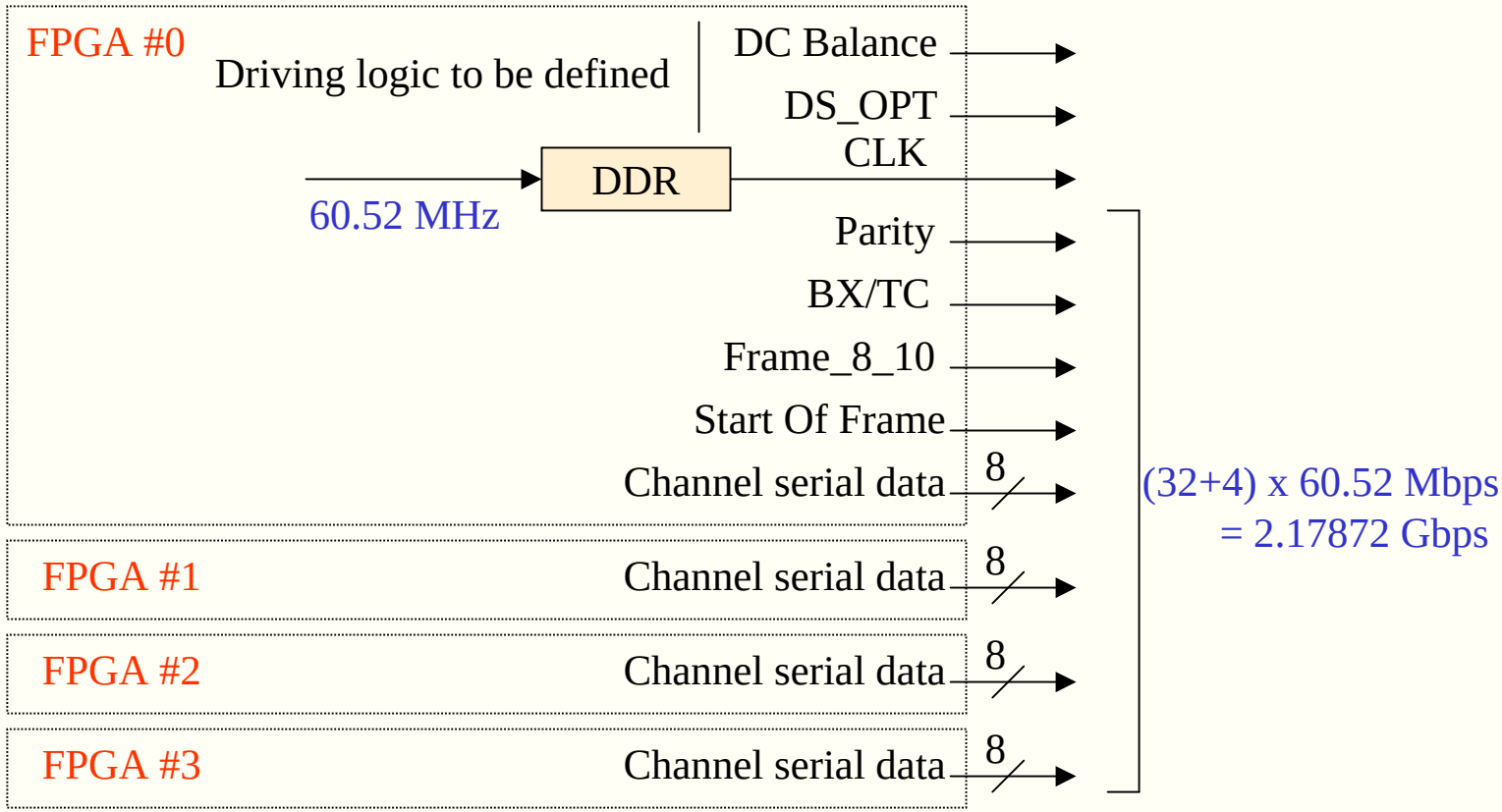

- Frame_8_10 low when sending 8 bit frames; high when sending 10 bit frames (sending raw ADC data following L1 Accept)

# ADF Latency (partial)



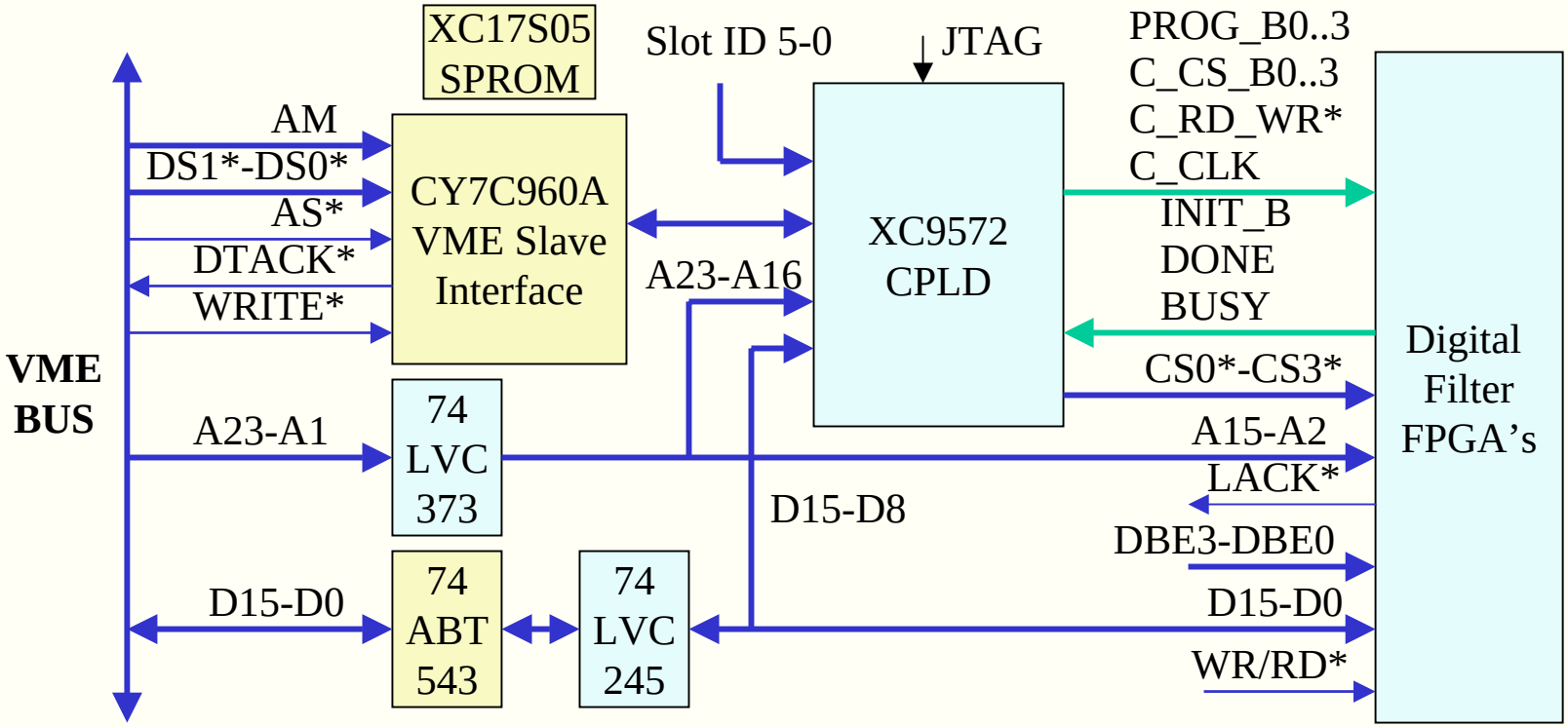

- 6.65 BC from peak at ADC digital output to last bit of result out of FPGA

# Channel Link Interface




- 36 bit lanes used (out of 48 available):
  - 8 channel data from by FPGA #0, #1, #2 and #3; 4 control lanes
- Clock + DC balance control bit + option bit

# VME interface and bootstrap logic




- Download FPGA configuration via VME:
  - *all 4 FPGA's loaded at once or different config on each FPGA*
- VME interface A24 D16-D8 only; no DMA; no interrupt
- Provides 5V <-> 3.3V conversion; Virtex 2 I/O not 5V tolerant

# Types of L1 Trigger for ADF System

- D0 Framework L1 Accept
  - *Generated by D0 framework; sent to all Geographic Sections via SCL*
  - *Fanout to ADF system by SCL Interface Fanout card (SCLIF)*
  - *Indicates that current BC is a L1 accepted event*

- L1 Accept with Monitoring
  - *Generated asynchronously by TCC to indicate that monitoring data of Geo section should be kept for one of next D0 framework L1 Accept*
  - *Sent synchronously by D0 L1 framework to Geo section by L1 Qualifier*
  - *If L1 Framework accept and L1 Qualifier for Monitoring asserted: the current L1 is to be monitored; all history data kept for TCC readout*
  - *L1 accept with monitoring flags are fanout to ADF system by SCL Interface Fanout Card*

# Types of L1 Trigger for ADF System

- L1 Software Accept
  - *Generated asynchronously by TCC to indicate that one of the next L1 crossing should be treated as D0 Framework L1 Accept by ADF system*
  - *Issued by one ADF card upon asynchronous write by TCC,*
  - *bounced-back synchronously to ADF system by SCLIF card*

- L1 Self trigger Accept
  - *Generated by each ADF channel when ADC input greater than programmable threshold*
  - *Wired-Ored for all channels on an ADF card*
  - *Wired-Ored for all ADF cards within each ADF crate and sent to SCLIF*
  - *OR-ed by SCLIF and sent back to all ADF cards synchronously*

# Actions upon L1 Trigger for ADF

- D0 Framework L1 Accept
  - *Send burst of raw ADC data to TAB (if feature enabled); no action if disabled*

    *-> TABs get raw ADC samples around BC that caused L1 trigger in D0*
- L1 Monitoring accept
  - *Send burst of raw ADC data to TAB (if enabled) then freeze history buffer in all channels*
  - *Wait resume recording command to start saving data in history buffer*

    *-> TCC can read ADC raw samples and intermediate results for some BC's that caused L1 trigger in D0*
- L1 Software accept
  - *Same action as L1 monitoring accept*

    *-> TCC can read ADC raw samples and intermediate results for random BC's that did not cause a L1 trigger in D0 (used to check correct operation of ADF system)*
- L1 Self trigger accept
  - *Same action as L1 monitoring accept*

    *-> TCC can record the shape of pickoff pulses on each channel to determine (off-line) optimal digital processing parameter sets*

# Limitations

- History buffer common for sending raw ADC samples to TAB and for read-out via TCC
  - *When recording is frozen (i.e. TCC read-out in progress), sub-sequent L1 accept will not trigger sending of raw ADC samples to TAB*

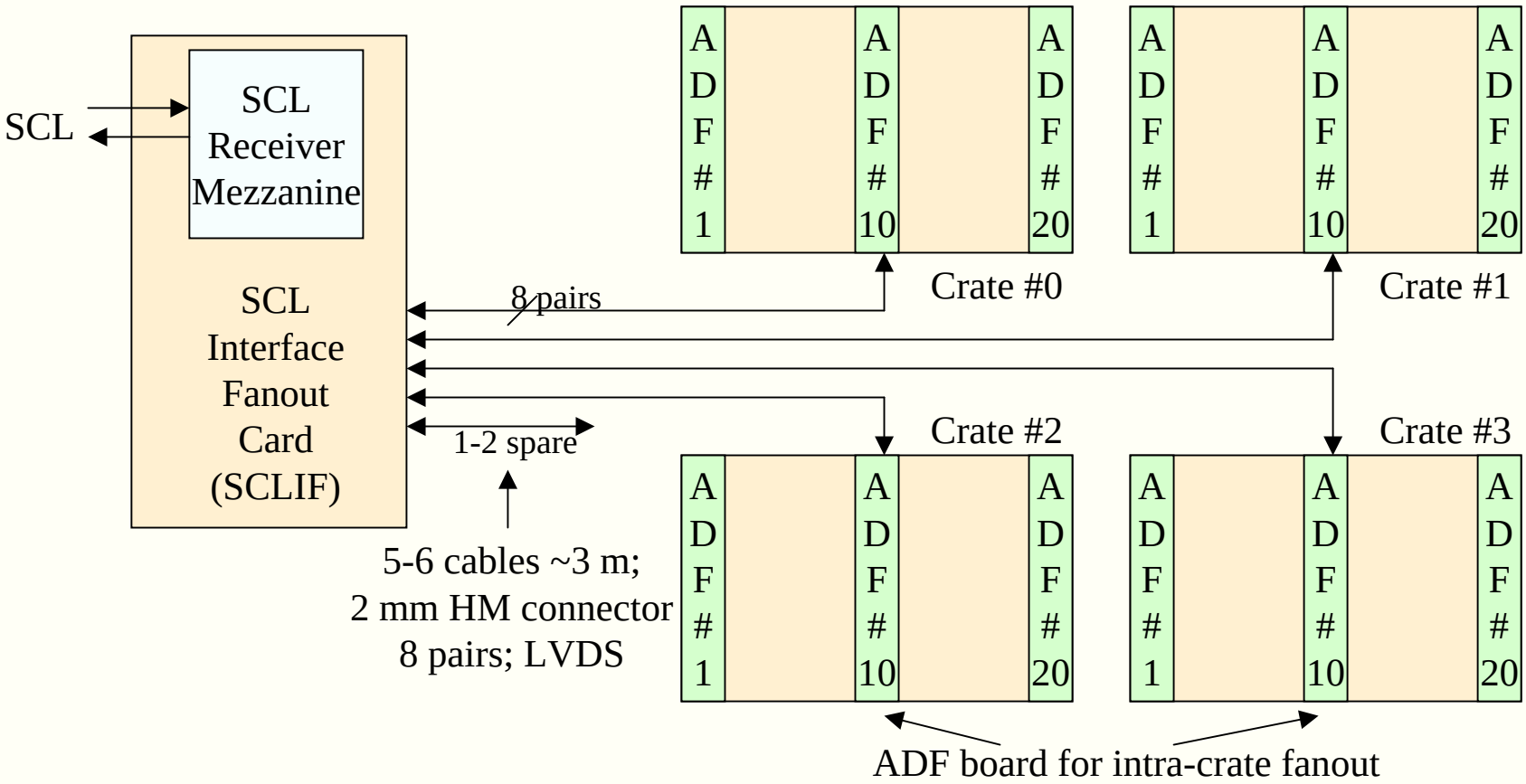
    *-> Raw ADC samples for these L1 accept are lost (but digital filter output continues to flow)*

  - *If no L1 Monitoring or L1 software accept are issued, raw sample recording is never frozen, raw samples for all L1 accept can be sent to TAB*

- Links to send filtered data and raw ADC data to TAB are the same
  - *While sending out raw ADC data to TABs, flow of filtered data is stopped -> can introduce dead-time for L1 if sending time is larger than that of other sub-systems*

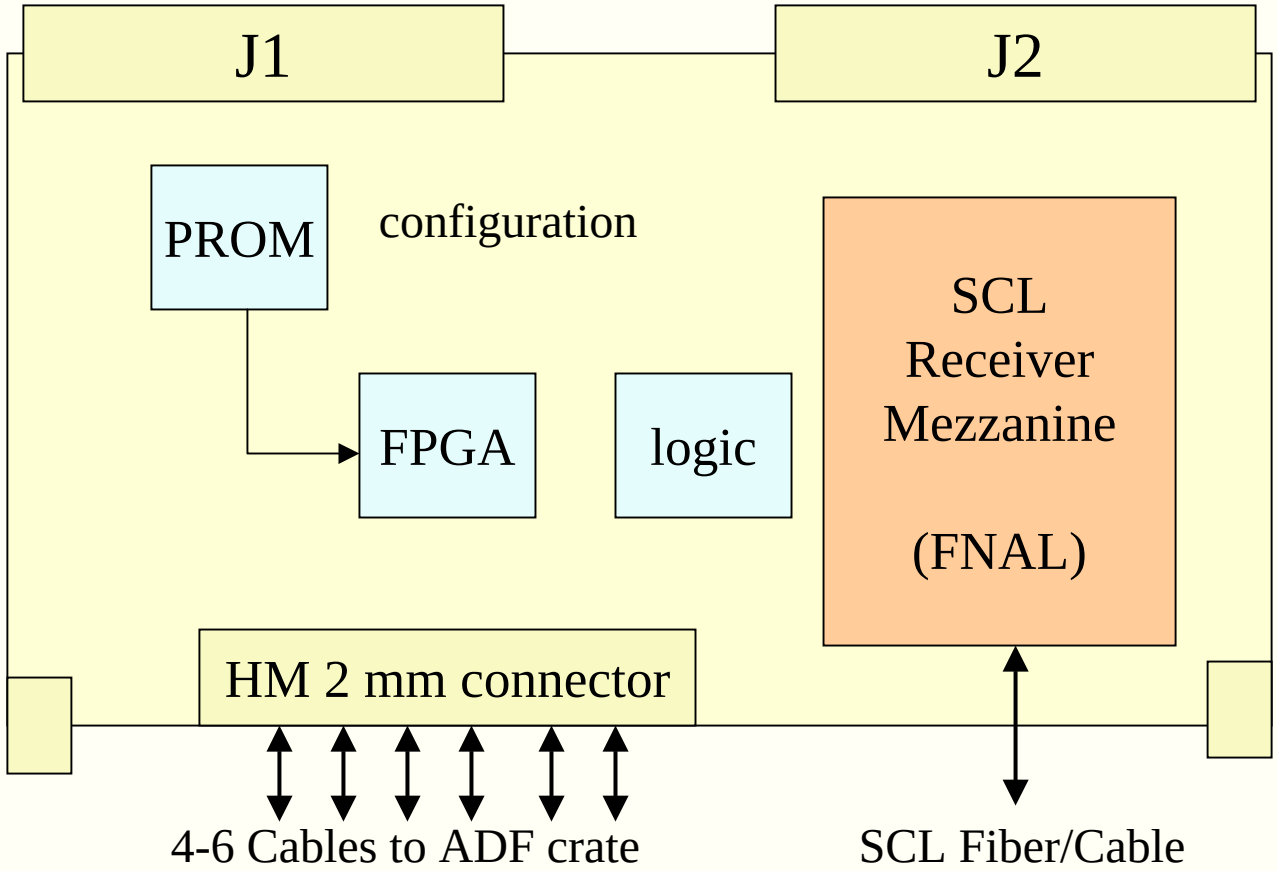
*-> e.g. sending raw samples of 8 BC around L1: 320 bit / channel*
*sending time = 5.28 us*

# SCL signals fanout




- 1 cable to one ADF board in each ADF crate
- ADF board where cable is plugged in charge of fanout within crate

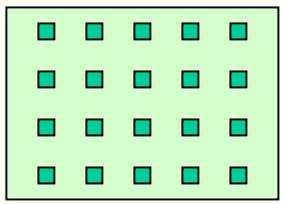
# SCL Interface and Fanout card




- VHDL design in progress
- 3U or 6U mechanics; No slow control
- No slot available in ADF crate -> back of slot 0 if enough space

# SCLIF to ADF communication

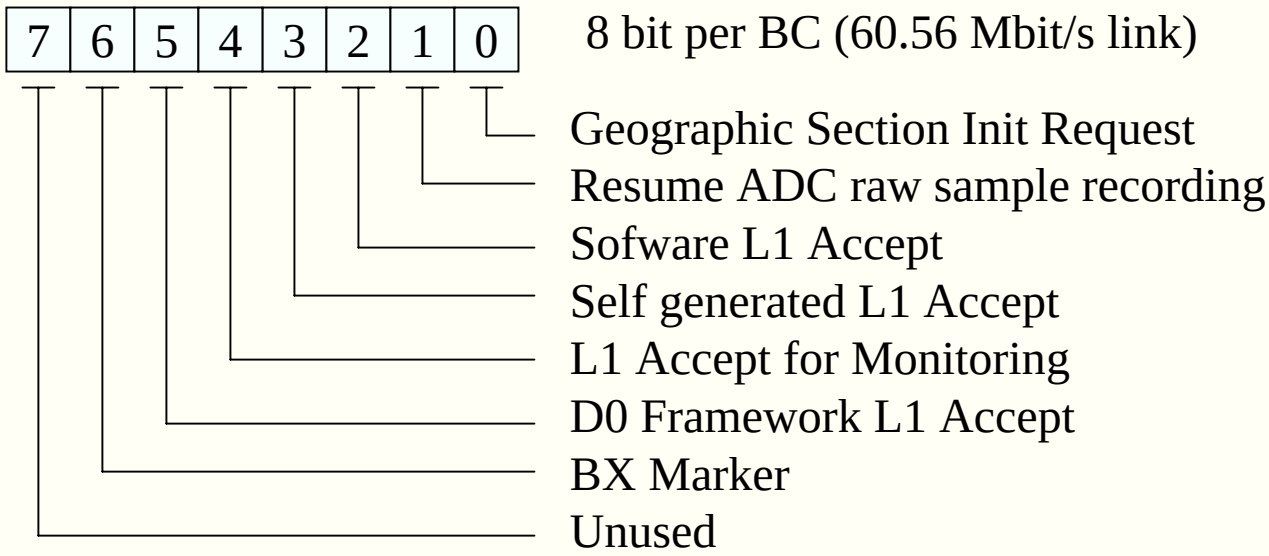
- SCLIF to ADF cable pinout (preliminary)



```
Cable detect rem,loc - GND - BC Clock
CMDD (SCLIF->ADF)    - GND - CMDU (ADF->SCLIF)
BUSY (ADF->SCLIF)    - GND - Self Trigger (ADF->SCLIF)
ERROR (ADF->SCLIF)   - GND - SPARE
```

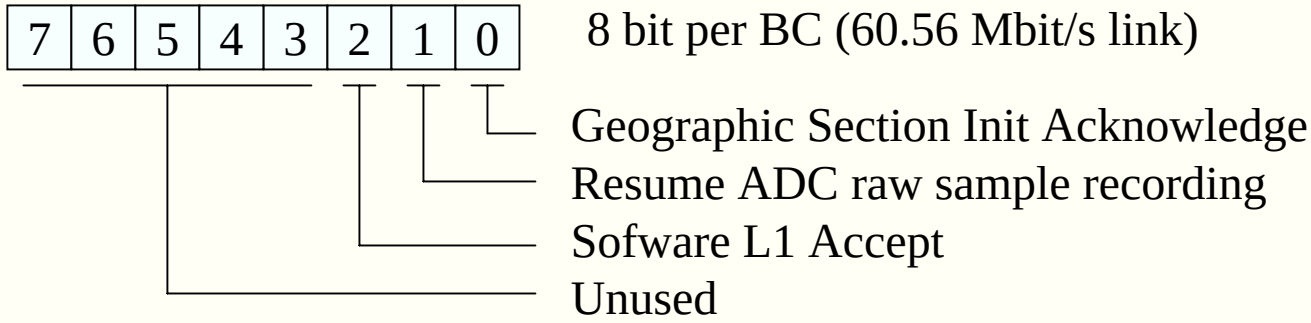
Cable detect remote: wired to GND on SCLIF card; pullup resistor on ADF card
Cable present local: pullup resistor on SCLIF card; active low output of ADF logic

- CMDD: Command Downstream (SCLIF to ADF system)



# SCL to ADF communication (con't)

- CMDU: Command Upstream (ADF to SCLIF system)



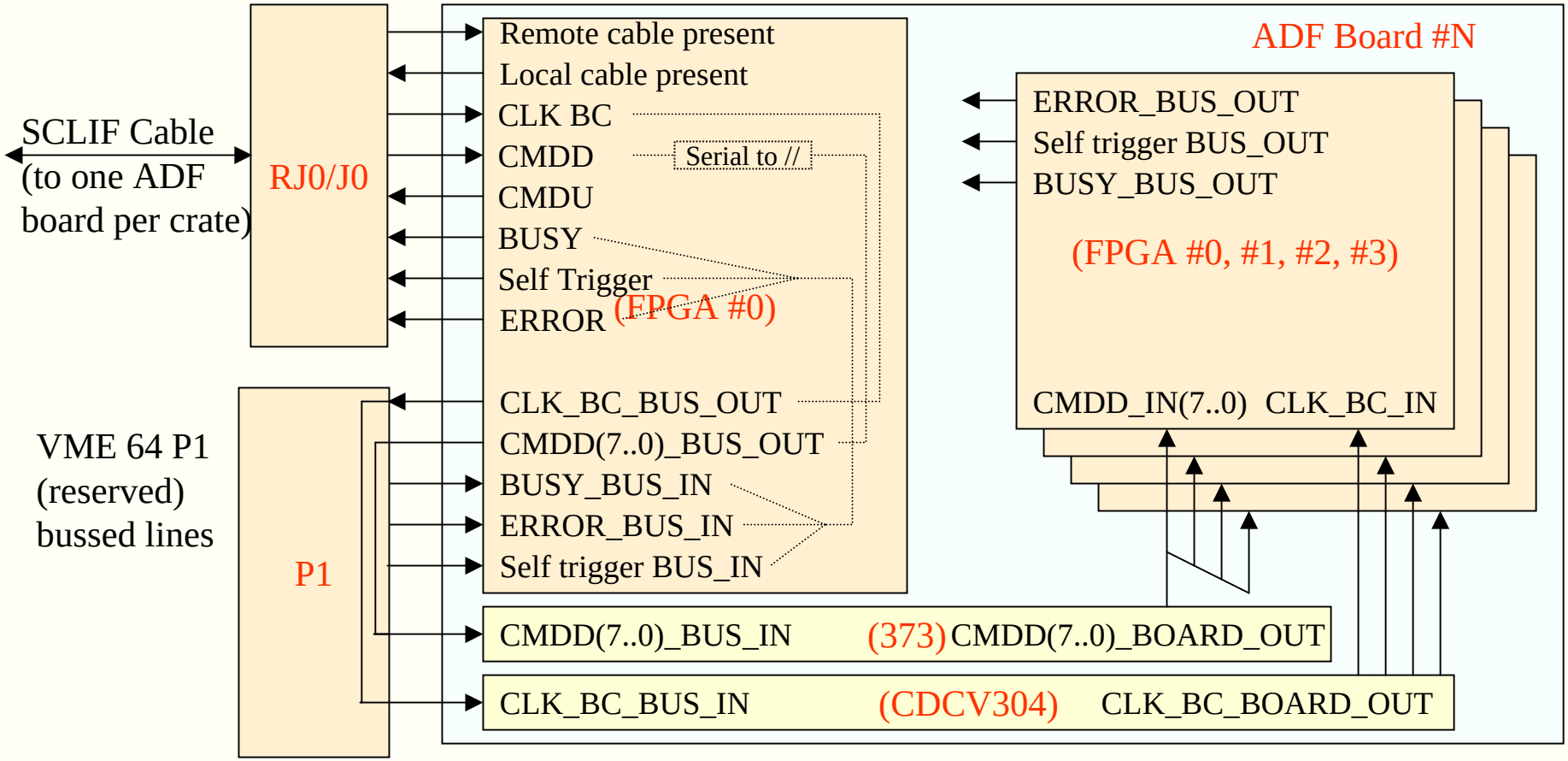

Bits « Resume ADC raw sample recording » and « Sofware L1 Accept »:

- Issued by one ADF card upon Write action by TCC to appropriate register
-Bounced-back by SCLIF to all ADF crates and cards
-> Equal-delay path from TCC to all ADF cards

Bit « Self L1 Accept »:

- Wired-OR self trigger signal for all ADF card within the same crate
- Per crate Self Trigger signal send on cable wires to SCLIF
- All per crate self trigger signals OR-ed by SCLIF to make Self Trigger bit
- Self trigger bit sent to all ADF simultaneously in CMDD serial stream

# Intra ADF crate Signal Distribution




- ADF board where SCLIF cable plugged: makes fanout of signals on backplane; other ADF boards tri-states outputs to bus
  - *All ADF boards get signals from backplane; local fanout for 4 FPGA's*

# Clock Fanout Chip Datasheet

**CDCV304**
**140-MHz PCI-X CLOCK BUFFER**

SCAS643B – SEPTEMBER 2000 REVISED JULY 2002

- General-Purpose and PCI-X 1:4 Clock Buffer
- Operating Frequency: 0 MHz to 140 MHz
- Low Output Skew: <100 ps
- Distributes One Clock Input to One Bank of Four Outputs
- Output Enable Control That Drives Outputs Low When OE Is Low
- Operates From Single 3.3-V Supply
- 8-Pin TSSOP Package

TSSOP
PW PACKAGE
(TOP VIEW)

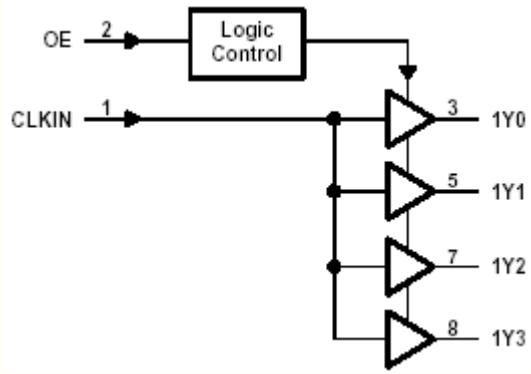

## description

The CDCV304 is a high-performance, low-skew, general-purpose and PCI-X clock buffer. It distributes one input clock signal (CLKIN) to the output clocks (1Y[0:3]). It is specifically designed for use with PCI-X applications. The CDCV304 operates at 3.3 V.

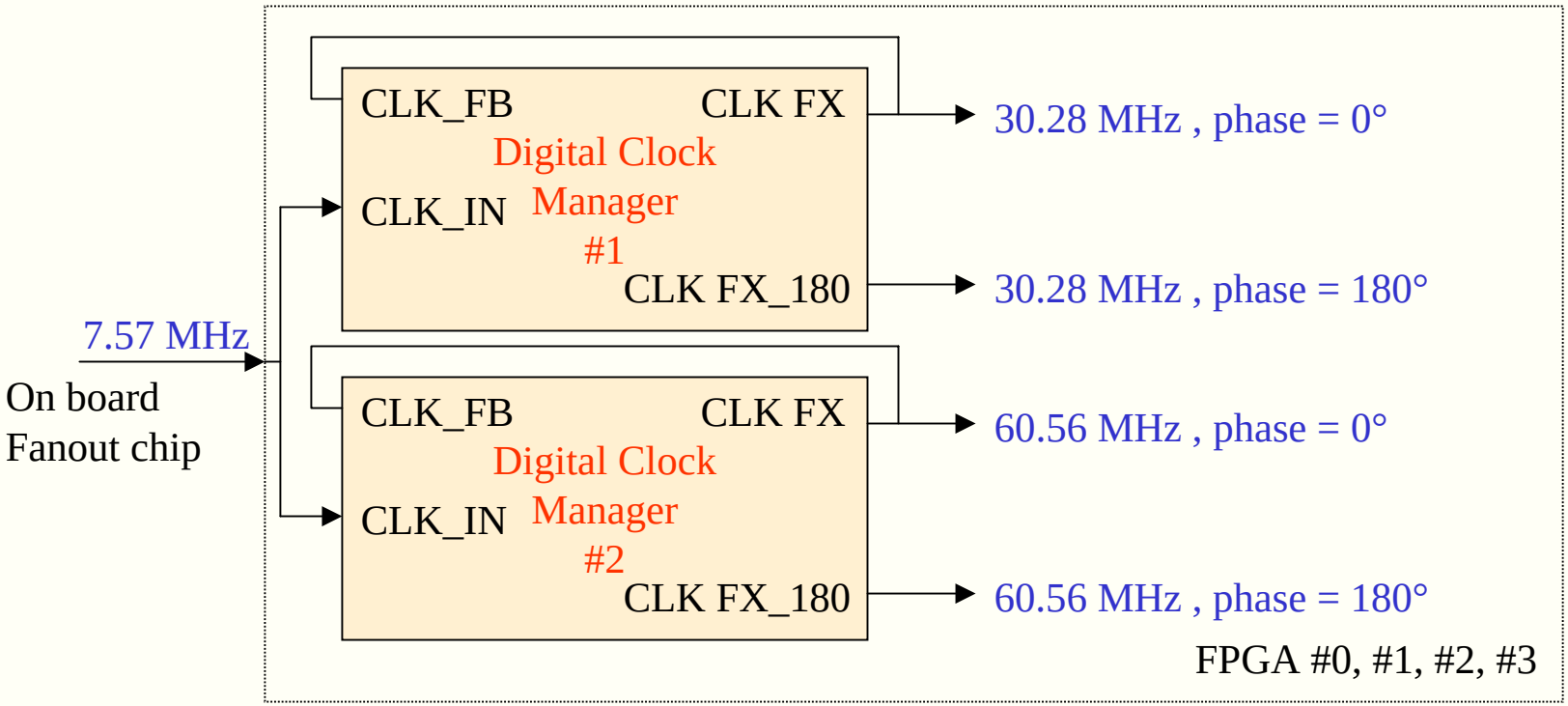
The CDCV304 is characterized for operation from –40°C to 85°C for automotive and industrial applications.

FUNCTION TABLE

| INPUTS | | OUTPUT |
|---|---|---|
| CLKIN | OE | 1Y (0:3) |
| L | L | L |
| H | L | L |
| L | H | L |
| H | H | H |

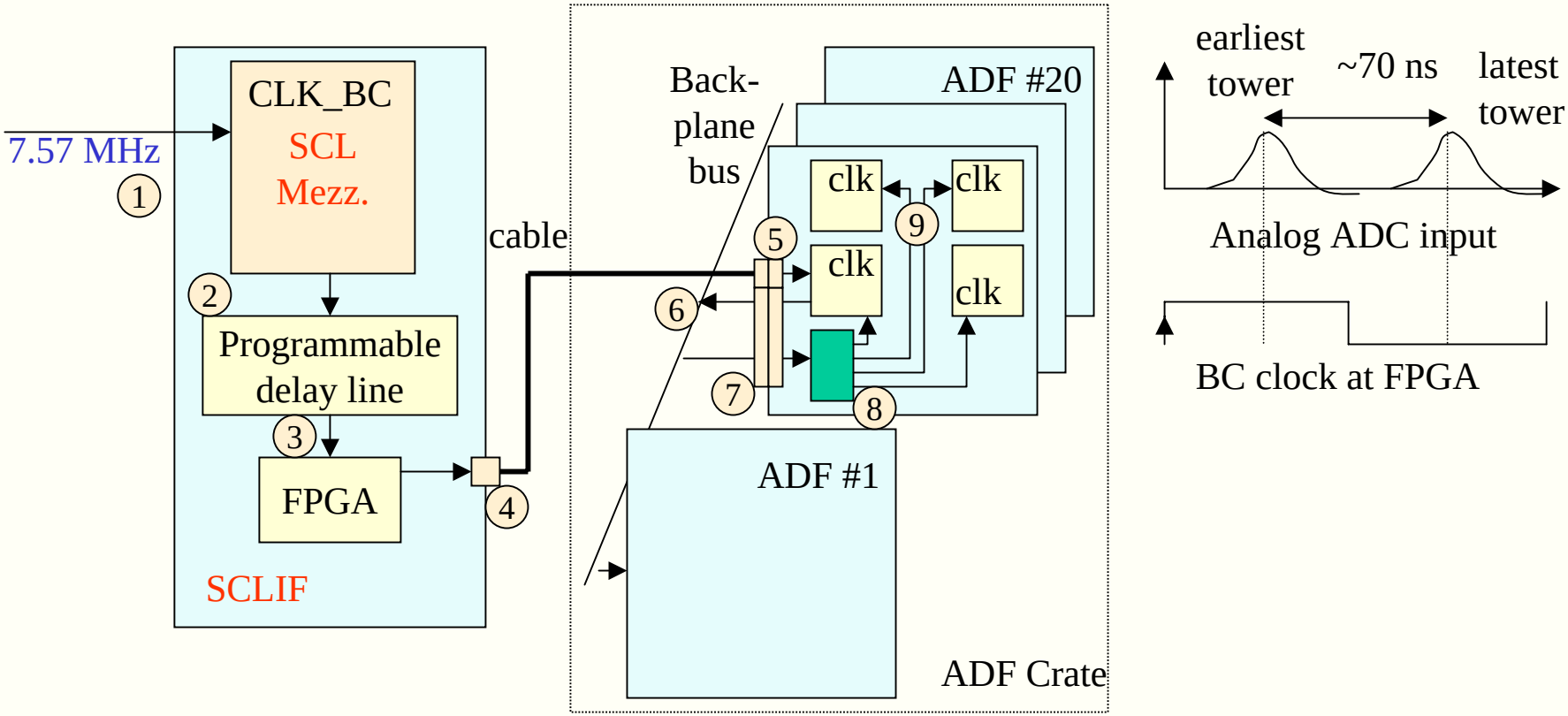


# FPGA Internal Clock Generation



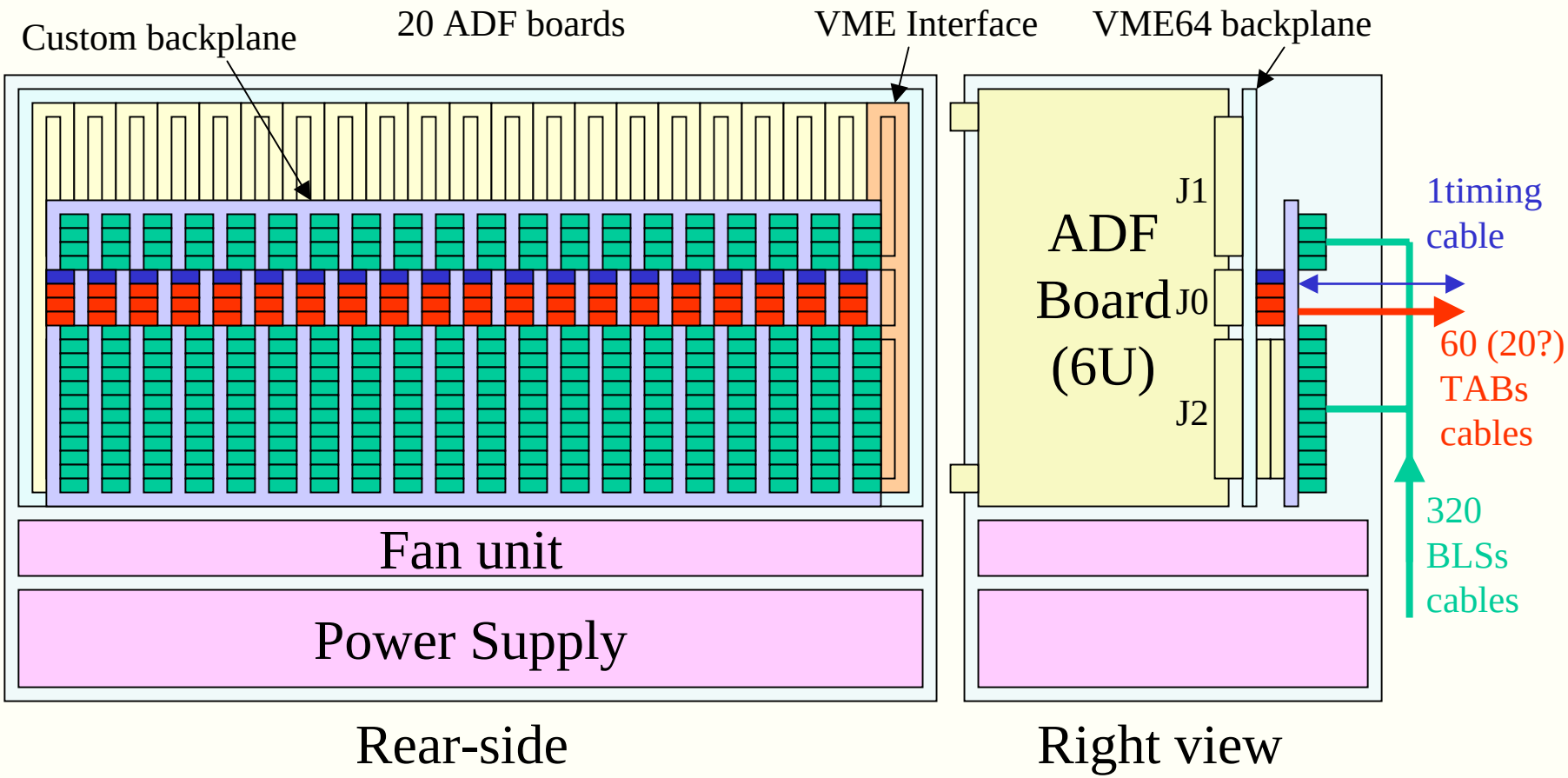

- On-chip BC clock multiplication by 4 and 8
  - *All logic driven at BC x 8 = 60.56 MHz*
  - *ADC clock from clock at BC x 4 = 30.28 MHz*

# System wide BC Clock phase align




- Clock distribution: expected delay dispersion: ~3 ns; jitter: 400 ps?
- Programmable delay line on SCLIF clock: adjusted so that all analog peaks at ADC input fall within same BC period

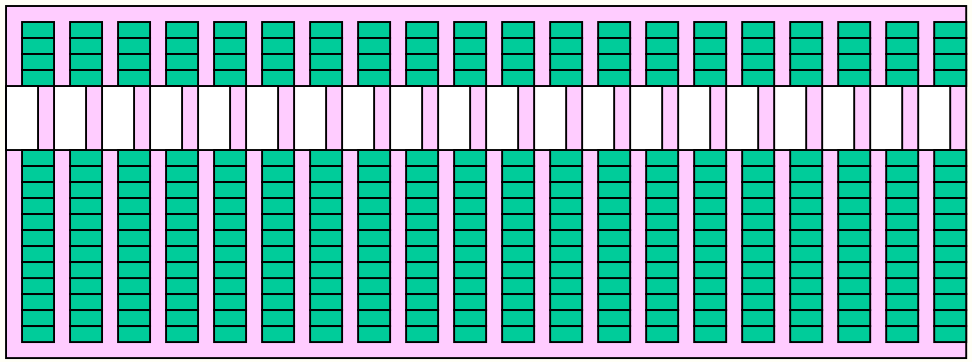
# ADF Crate

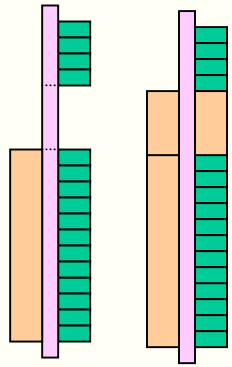



- Crate to be delivered ~November 2002
- Custom backplane: design not started

# Custom Backplane

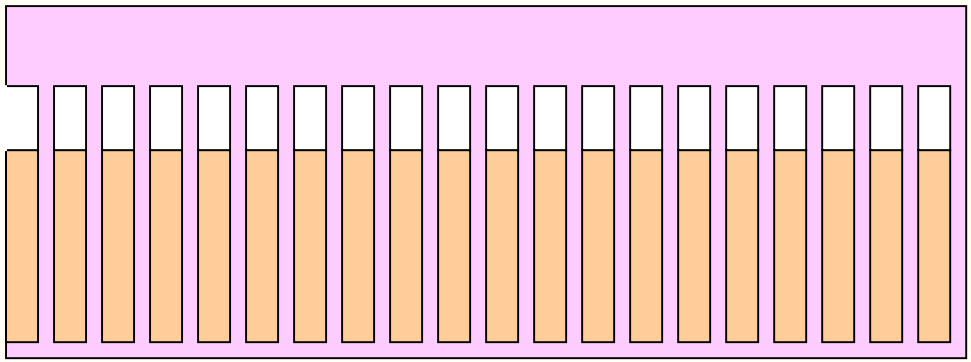
External Side:
20 x 16
AMP 8 points
connectors





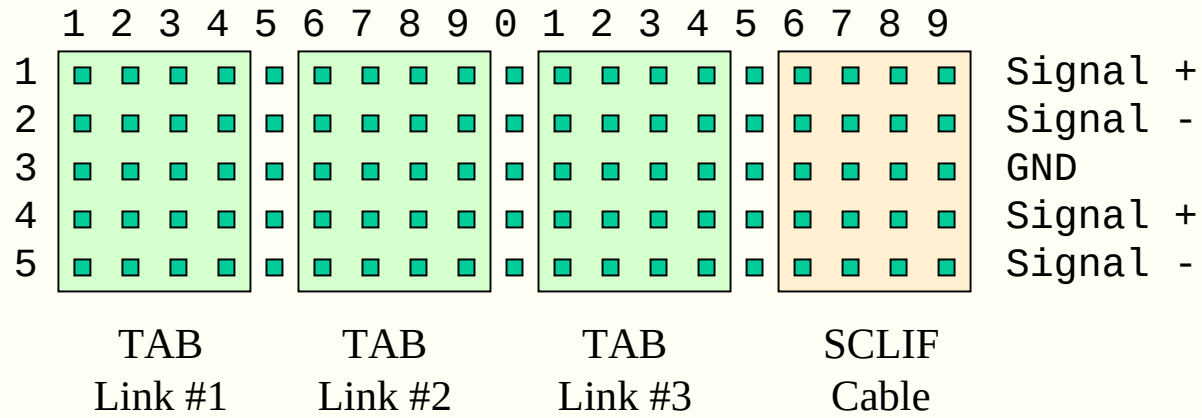
option with
J0 transition
connector

Internal Side:
20 VME 160 points
connectors



- Passive backplane; controlled impedance traces
- Need some mechanics to hold (heavy) cables

# RJ0 Usage (preliminary)




- 19 x 5 2 mm Hard Metric connector can accomodate:
  - 3 cables to TAB each 8 or 10 pairs (if 8-pair cable: GND 5 pins between each cable)
  - 1 cable to SCLIF (for one ADF card in each crate)
- Cable to TAB
  - 8-pair cable could be 7 signals + 1 clock : transmit 7x6=42 bit of Channel Link (out of 48), altough 36 bits are assigned at this stage
  - Cable detection feature?

# Power Estimation

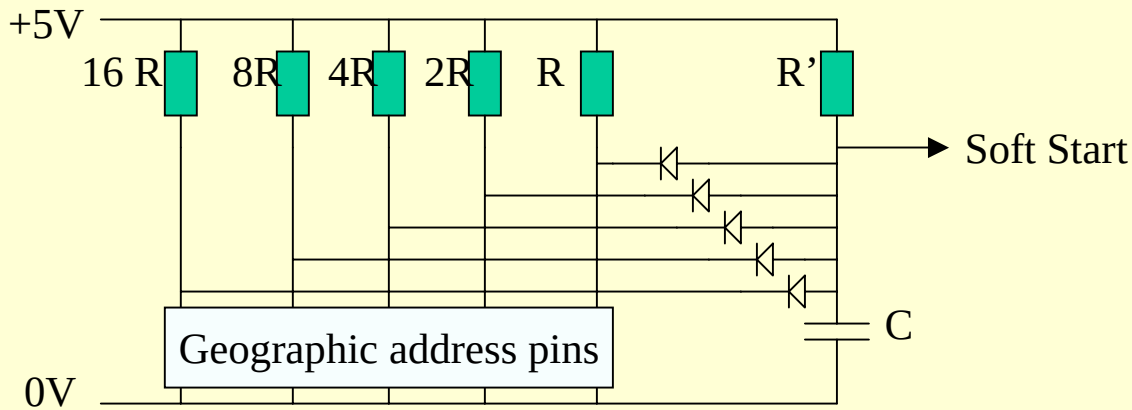
- FPGA Core 1.5V
  - 3.2 A per ADF board

  -> converted from +5V with DC/DC @85% eff.: 1.2 A / board 23 A /crate
- Logic 3.3 V
  - 0.75 A per board

  -> converted from +5V with DC/DC @85% eff.: 0.6 A / board 12 A /crate
- ADC 3.3 V
  - 2.8 A per board; 60 A per crate
- ADC driver –5 V
  - 0.6 A per board; 12 A per crate
- Crate requirement: +5V 45A; +3.3V 60A; -5V 12A

# ADF Power circuitry

- FPGA Core 1.5V
  - converted from +5V with DC/DC converter EL7564
  - Per slot startup delay to power each board after the other




- Logic 3.3 V
  - converted from +5V with DC/DC converter EL7564
- ADC 3.3 V
  - taken from VME 64 P1 connector
- ADC driver –5 V
  - taken from VME 64 P1 connector

# DC/DC Converter Datasheet

élantec

## EL7564C

*Monolithic 4 Amp DC:DC Step-Down Regulator*

EL7564C

### Features

- Integrated synchronous MOSFETs and current mode controller
- 4A continuous output current
- Up to 95% efficiency
- 4.5V to 5.5V input voltage
- Adjustable output from 1V to 3.8V
- Cycle-by-cycle current limit
- Precision reference
- ±0.5% load and line regulation
- Adjustable switching frequency to 1MHz
- Oscillator synchronization possible
- Internal soft start
- Over voltage protection
- Junction temperature indicator
- Over temperature protection
- Under voltage lockout
- Multiple supply start-up tracking
- Power good indicator

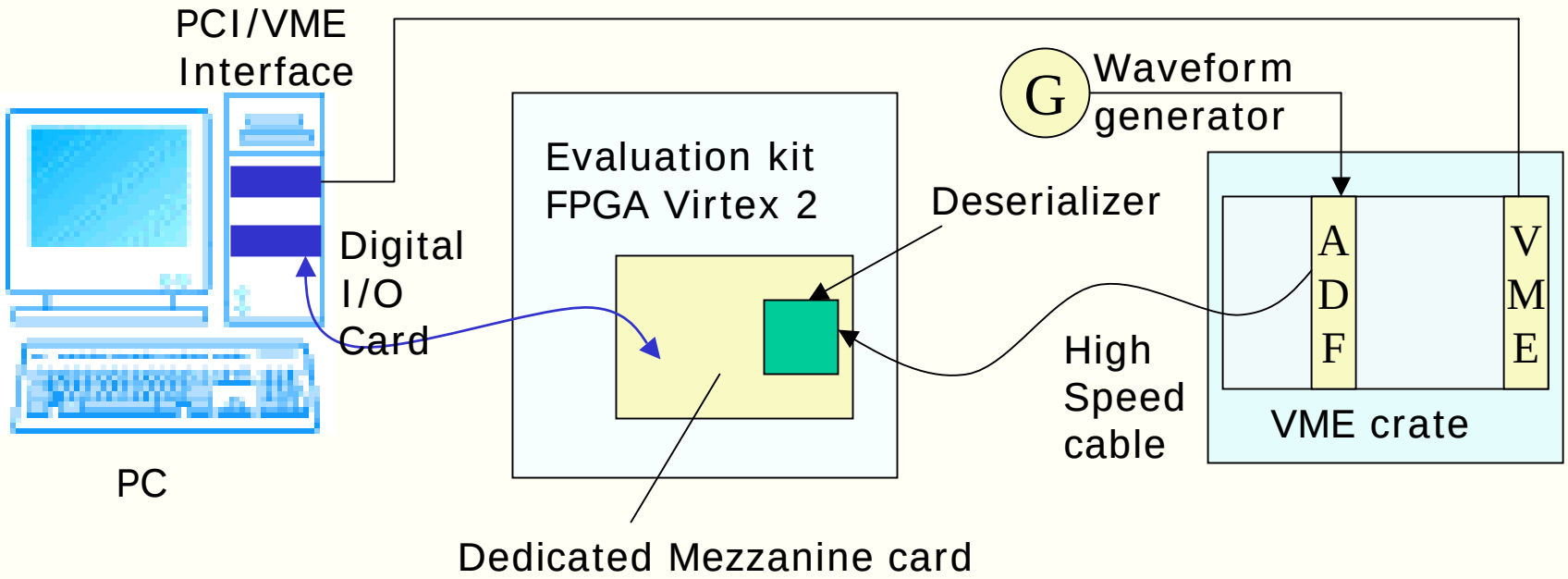
### General Description

The EL7564C is an integrated, full-featured synchronous step-down regulator with output voltage adjustable from 1.0V to 3.8V. It is capable of delivering 4A continuous current at up to 95% efficiency. The EL7564C operates at a constant frequency pulse width modulation (PWM) mode, making external synchronization possible. Patented on-chip resistorless current sensing enables current mode control, which provides cycle-by-cycle current limiting, over-current protection, and excellent step load response. The EL7564C features power tracking, which makes the start-up sequencing of multiple converters possible. A junction temperature indicator conveniently monitors the silicon die temperature, saving the designer time on the tedious thermal characterization. The minimal external components and full functionality make this EL7564C ideal for desktop and portable applications.

The EL7564C is specified for operation over the -40°C to +85°C temperature range.

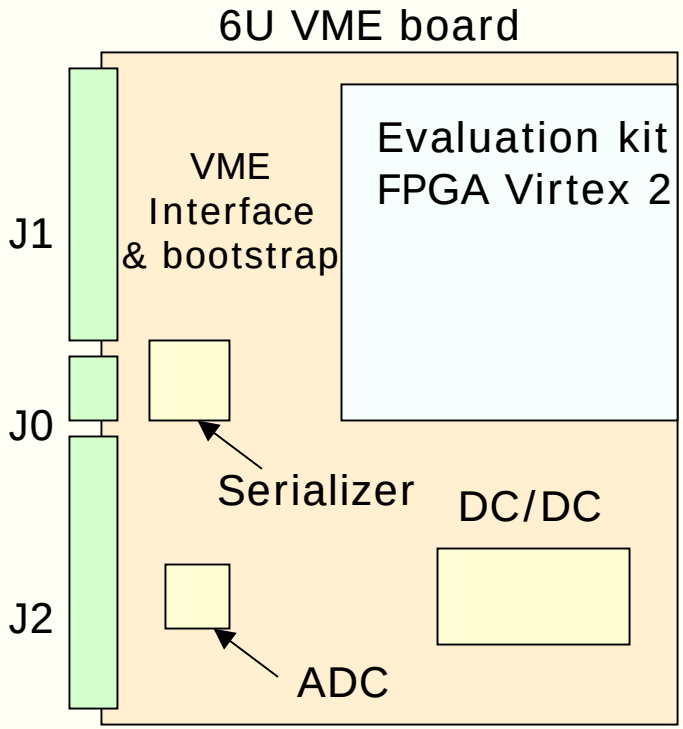
### Typical Application Diagrams

# Test bench ADF board




- Standards items + dedicated mezzanine card(s)
  - *-> Channel Link de-serializer mezzanine: redundent with Nevis development*
  - *-> Mezzanine with 1 ADC (to test 1 analog input + digital filter)*

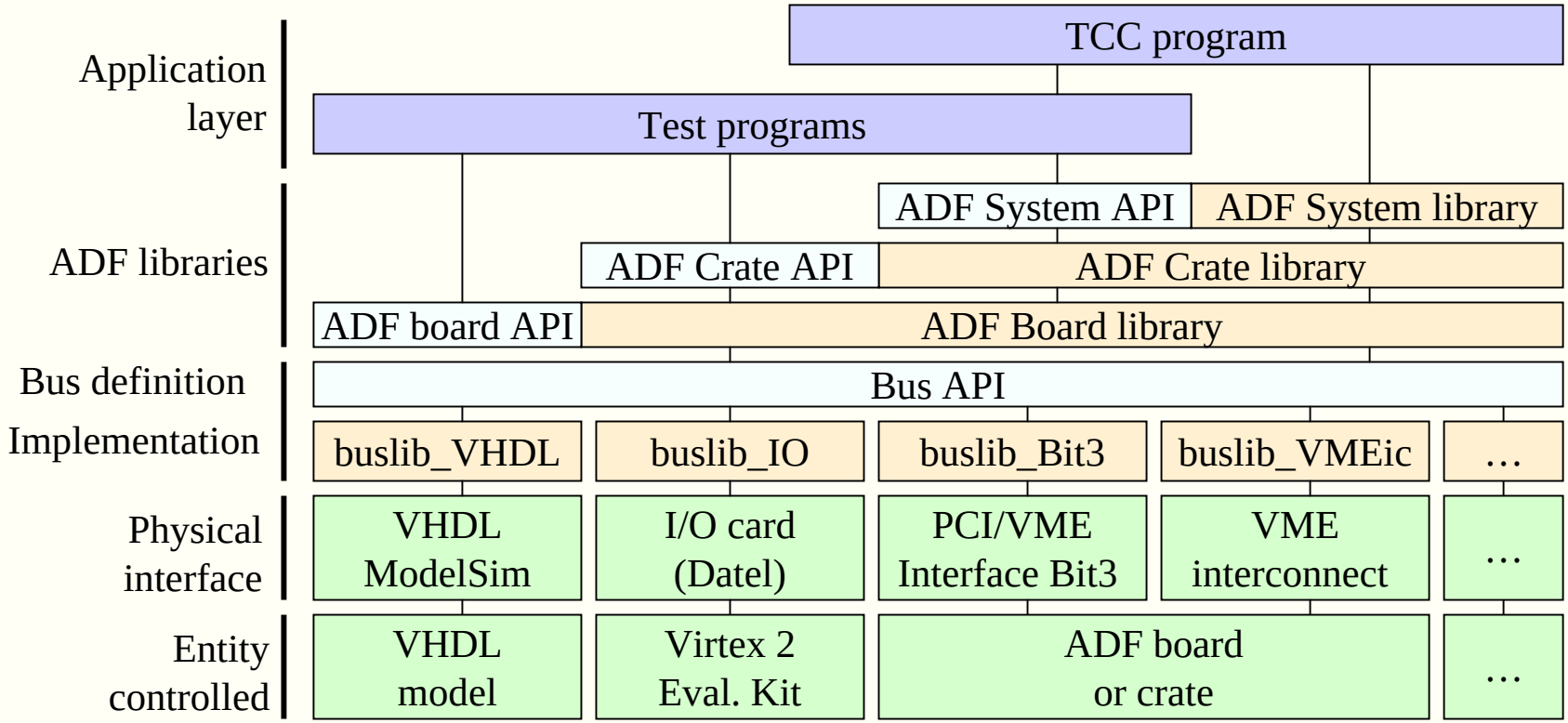
# Reduced ADF board




- Debugging VME interface & bootstrap logic
- Test DC/DC converter and power supply sequencing
- Test 1 serializer with J0/RJ0 PCB traces
- Test 1 analog channel

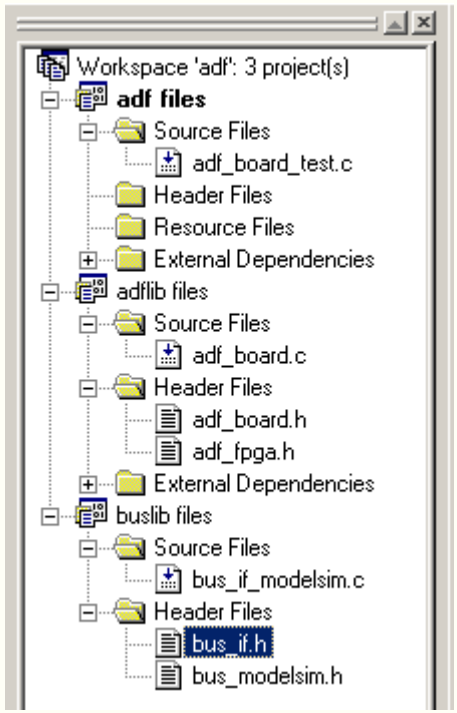
  *-> Design dependant on time and manpower (e.g. summer student)*

# Software




- Modular software built in multiple layers
  - Abstraction of bus interface to support multiple physical implementation as well as SW/HW co-design with VHDL model
  - Static libraries for ADF card, crate and system

# Bus API




```
/* Bus Creation and Deletion functions */
int Bus_Create(BusStruct* *bs, BusArg *ba, char *report, int rep_max, int *rep_sz);
int Bus_Delete(BusStruct* *bs, char *report, int rep_max, int *rep_sz);

/* Bus Open, Close and Control functions */
int Bus_Open(BusStruct* bs, char *report, int rep_max, int *rep_sz);
int Bus_Close(BusStruct* bs, char *report, int rep_max, int *rep_sz);
int Bus_Control(BusStruct* bs, int flags, char *report, int rep_max, int *rep_sz);
int Bus_Sleep(BusStruct* bs, int duration, char *report, int rep_max, int *rep_sz);

/* Bus Read and Write for Byte and Short */
int Bus_ReadByte(BusStruct *bs, unsigned int adr, unsigned char *data, char *report,
    int rep_max, int *rep_sz);
int Bus_ReadShort(BusStruct *bs, unsigned int adr, unsigned short *data, char
    *report, int rep_max, int *rep_sz);
int Bus_WriteByte(BusStruct *bs, unsigned int adr, unsigned char data, char *report,
    int rep_max, int *rep_sz);
int Bus_WriteShort(BusStruct *bs, unsigned int adr, unsigned short data, char
    *report, int rep_max, int *rep_sz);
```

- So far, 10 functions defined
  - At present only one implementation, for VHDL ModelSim simulator

# ADF Board API

```
/* ADFboard Creation and Deletion functions */
int ADFboard_Create(...);
int ADFboard_Delete(...);
/* ADFboard Open, Close functions */
int ADFboard_Open(...);
int ADFboard_Close(...);
int ADFboard_ConfigureFPGA(...);
int ADFboard_SetInDecimatorPhase(...);
int ADFboard_SetOutDecimatorPhase(...);
int ADFboard_PeakDetectorOff(...);
int ADFboard_PeakDetectorOn(...);
int ADFboard_SetPeakDivisor(...);
int ADFboard_TestModeOff(...);
int ADFboard_TestModeOn(...);
int ADFboard_SetCoarseLatency(...);
int ADFboard_SetSerializerSource(...);
```

```
int ADFboard_SetConstantValue(...);
int ADFboard_SetSelfTriggerThreshold(...);
int ADFboard_SetChannelRegisterA(...);
int ADFboard_SetChannelRegisterB(...);
int ADFboard_RegisterFieldOperation(...);
int ADFboard_RamOperation(...);
int ADFboard_FilterCoefficientOperation(...);
int ADFboard_EnableChannel(...);
int ADFboard_DisableChannel(...);
int ADFboard_GetState(...);
int ADFboard_GetStateAndPrint(...);
int ADFboard_GetClockState(...);
int ADFboard_GetClockStateAndPrint(...);
int ADFboard_GetChipID(...);
int ADFboard_GetChipIDAndPrint(...);
int ADFboard_LoadL1Mask(...);
int ADFboard_SendCommand(...);
...
```

- At present, about 30 functions defined and implemented
  - Functions return 0 on success, -1 on error
  - Printable string contains status of error/success
  - A function acts on 0 to 32 channels of the ADF card addressed by appropriate setting of a 32 bit channel selection bit pattern

# ADF Crate Address Map

| A23 | A(22..21) | | A(17..16) | A(15..14) | A(13..0) | Ressource |
|---|---|---|---|---|---|---|
| X | 11 | Slot (2..0) | Slot (4..3) | 0 0 | XX…X | Config. A |
| | | | | 0 1 | | Config. B |
| | | | | 1 0 | | Config. C |
| | | | | 1 1 | | Config. D |
| | Slot (4..0)<br>00001<br>To<br>10100 | | FPGA ID<br>00<br>To<br>11 | XX…X | | Filter Registers & LUT |

- ADF board selected by VME Slot (Geographical addressing)
  - 64 KB taken by 4 registers + 256 KB for filter
- 8 MB of address space per crate (~6 MB used)
  - 4 crates OK with limitation of 32 MB per Bit3 interface

# FPGA Configuration Registers

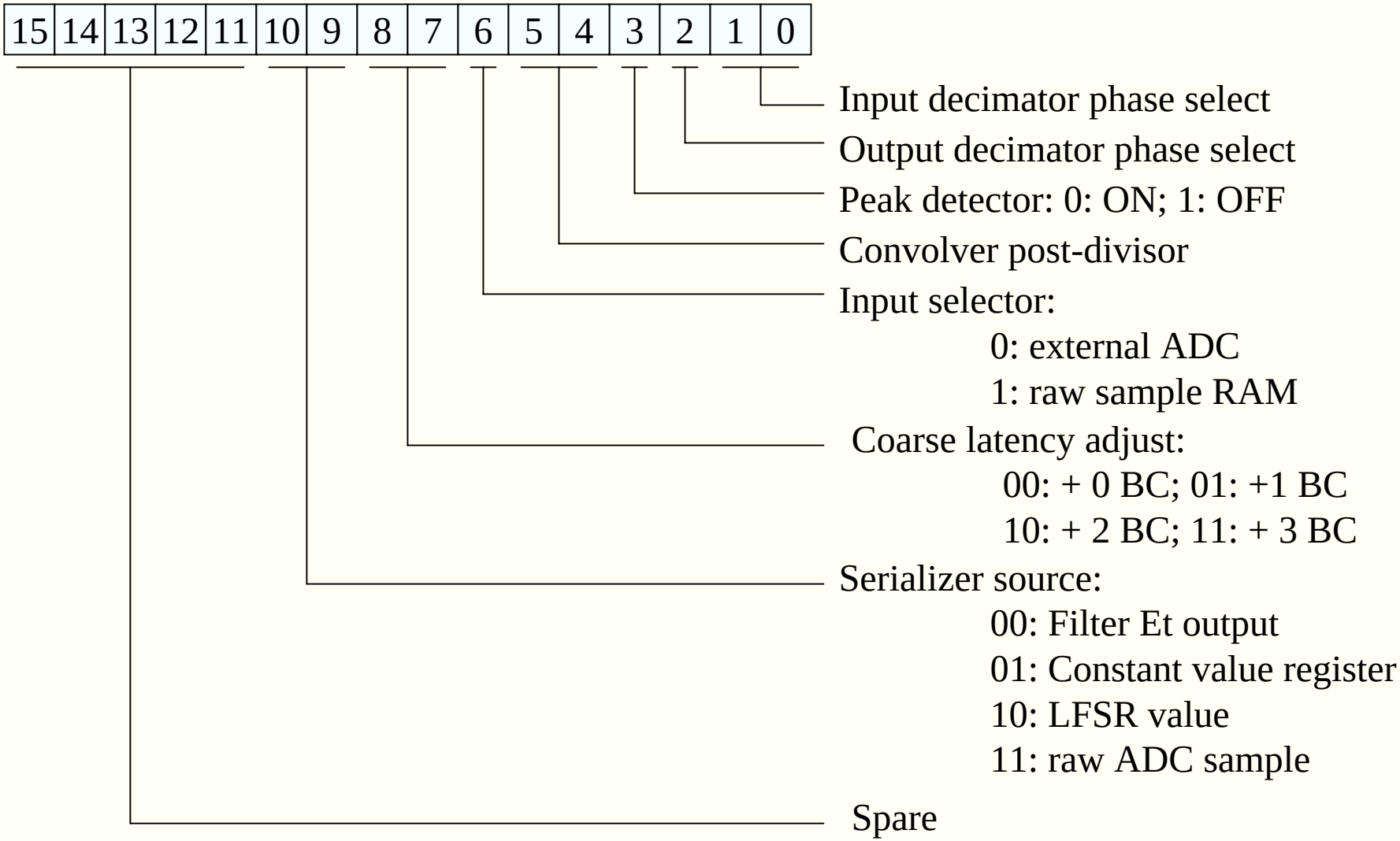
| D (7..4) | D (3..0) | | | | Type | Register |
|---|---|---|---|---|---|---|
| Prog. CS_B FPGA (3..0) | PROG_B FPGA (3..0) | | | | WO | Config. A |
| FPGA configuration DATA (7..0) | | | | | WO | Config. B |
| xxxx | rsvd | RESET | RD/WR* | CLK | WO | Config. C |
| xxxx | x | INIT_B | DONE | BUSY | RO | Config. D |

- All Programmation registers are accessible only in A24/D08
- FPGA Configuration read-back not supported
- Simultaneous download of 4 FPGA's with same configuration or one different configuration in each FPGA

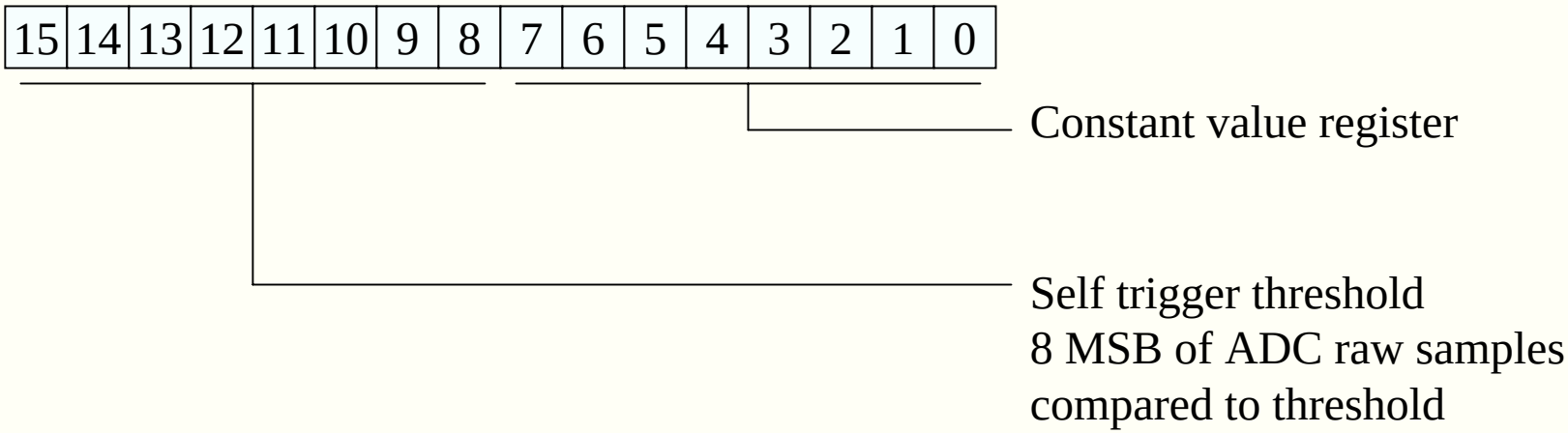
# Filter FPGA Address Map

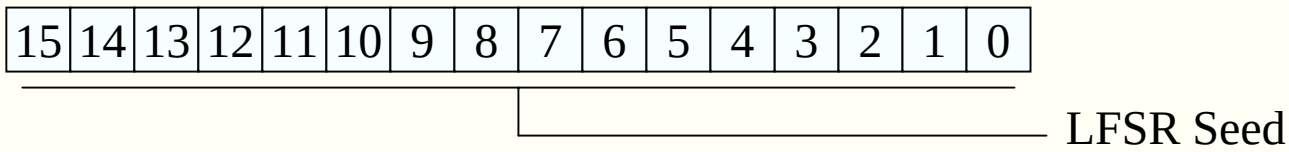
| A(15..13) | | A(11..10) | A(9..7) | A(6..4) | A(3..1) | A0 | Ressource |
|---|---|---|---|---|---|---|---|
| Channel 000 To 111 | 0 | RAM Addr(10..0) | | | | 0 | Et LUT – 2K x 9 bit |
| | 1 | 0 0 | RAM Addr(8..0) | | | 0 | Raw samples – 512 x 10 bit |
| | | 0 1 | RAM Addr(8..0) | | | 0 | Convol. Out – 256 x 16 bit |
| | | 1 0 | RAM Addr(8..0) | | | 0 | Filter Out – 128 x 8 bit |
| | | 1 1 | 000 | CCC | XXX | 0 | Filter Coef. – 8 x 6 bit |
| | | | 001 | XXXXXX | | 0 | LFSR Seed |
| | | | 010 | XXXXXX | | 0 | Channel Register A |
| | | | 011 | XXXXXX | | 0 | Channel Register B |
| | | | 100 | 0 | XXXXX | 0 | Global Register A |
| | | | 100 | 1 | XXXXX | 0 | Global Register B |
| | | | 101 | 0 | XXXXX | 0 | Global Register C |
| | | | 101 | 1 | XXXXX | 0 | Global Register D |
| | | | 110 | 0 | XXXXX | 0 | Global Register E |
| | | | 110 | 1 | XXXXX | 0 | Global Register F |

# Channel Register A

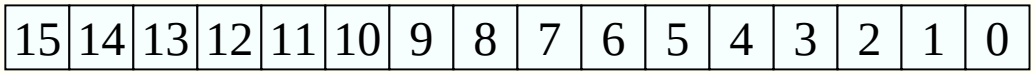


# Channel Register B, LFSR Seed



# Global Register A

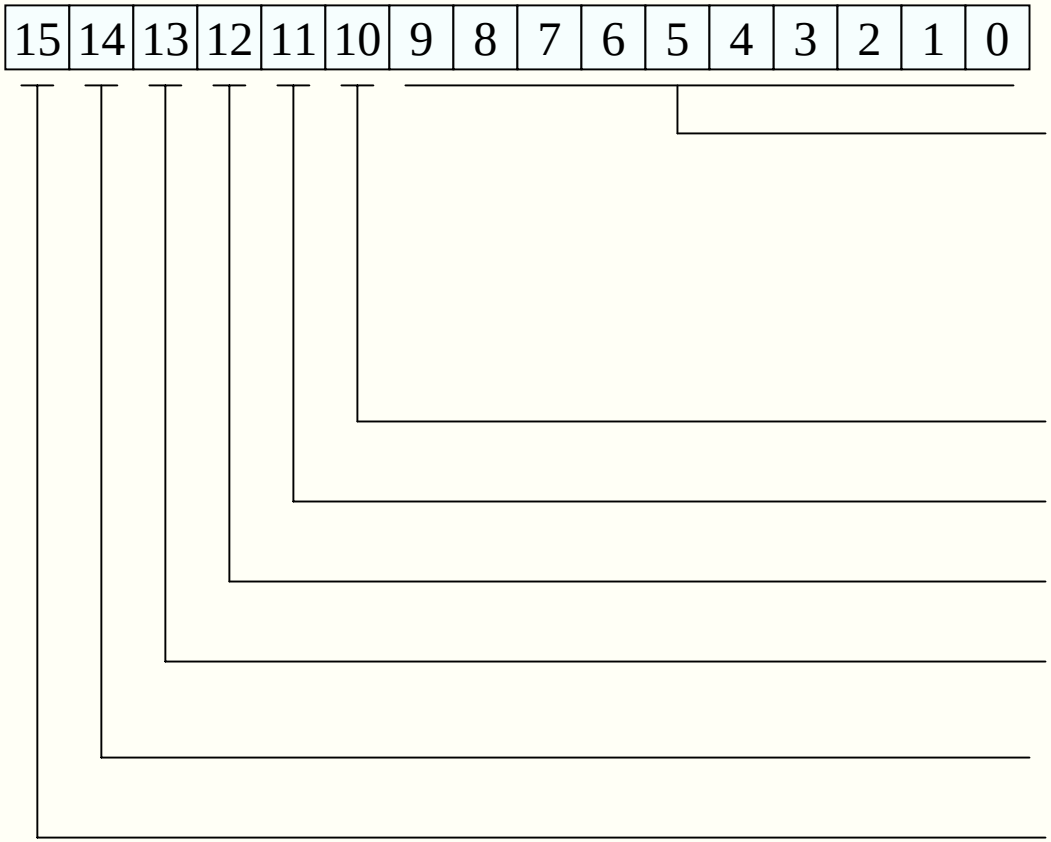



Latency offset count (L)
Raw ADC sample RAM operation:
- write starts at address 0
-read (for send) starts at:
(last_wr_address + L) mod 1024

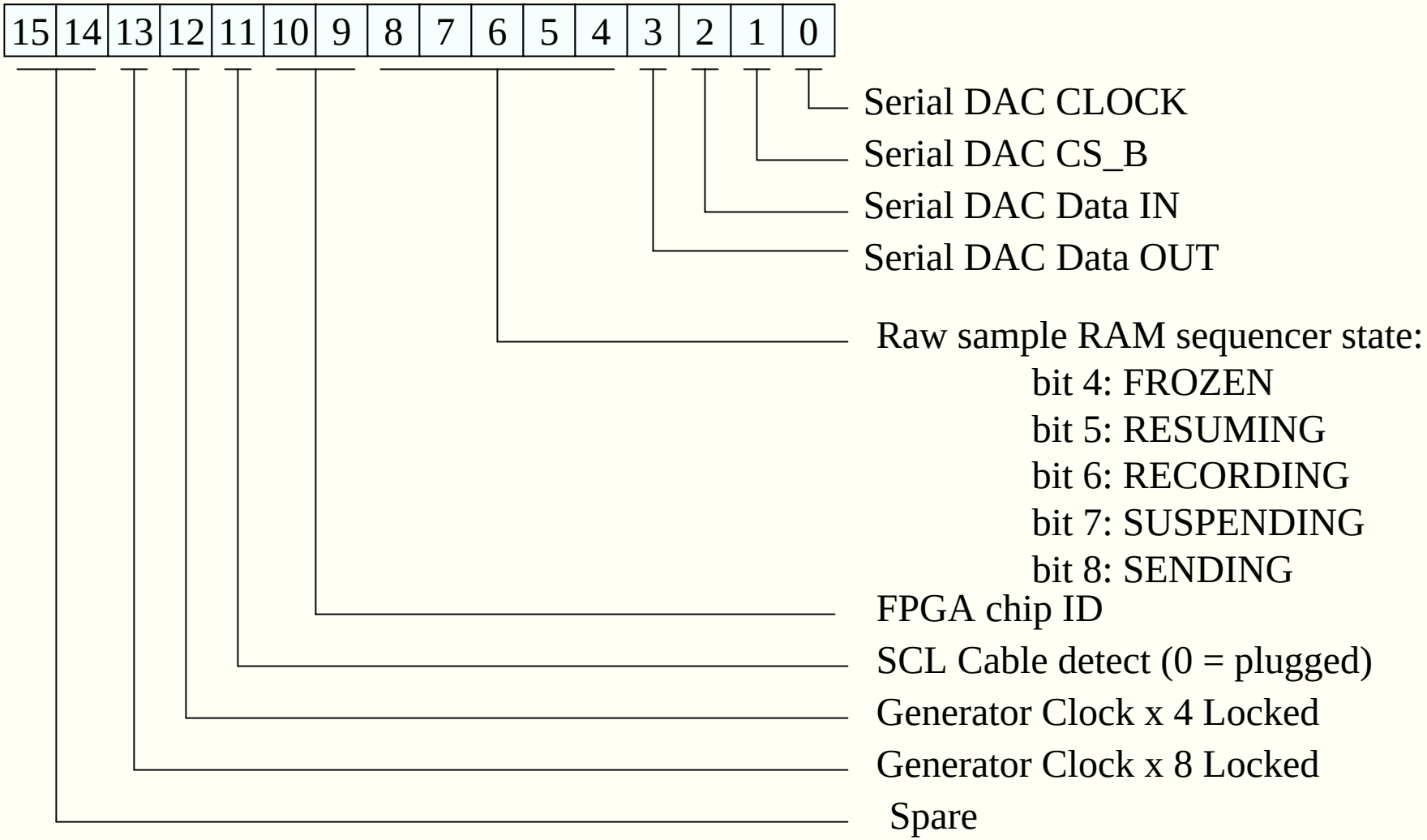
Fine latency adjust:
00: + 0:8 BC; 01: +1:8 BC
10: + 2:8 BC; 11: + 3:8 BC

Spare

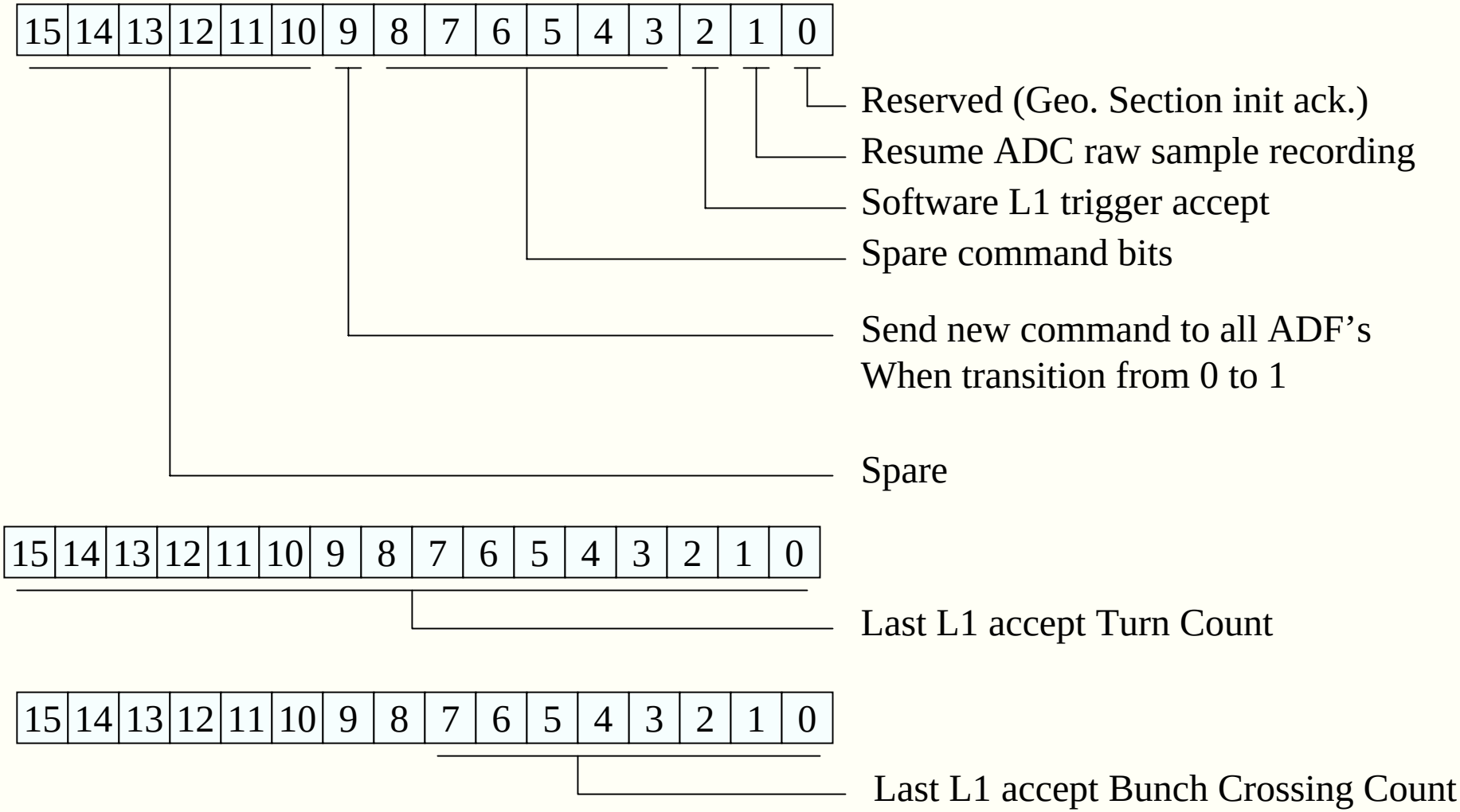
# Global Register B



# Global Register C



# Global Register D, E, F



# Summary

- Analog Splitter:
  - prototype completed, partially tested -> corrections to PCB coming
- Algorithm and Simulation chain:
  - Algorithm unchanged: 8 tap FIR @ BCx2 + 3 pt peak detector + LUT
  - Simulation chain: coherence with VHDL simulation to pursue
- ADF board:
  - Analog section under design; digital section almost completed
  - Schematic to start soon; some board level VHDL simulation to do
- Other ADF system components
  - Crate to be delivered, custom backplane: design not started
  - SCL timing Fanout board: VHDL design and simulation in progress
  - Testbench: 2 ideas around Virtex II evaluation kit – no design started
- Software
  - Some low level functions to control ADF board written and tested
  - Interface with TCC, D0 DAQ, calibration software: no yet addressed