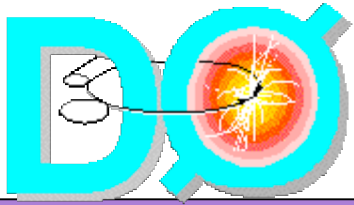


Cable Tester

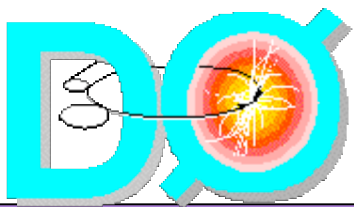
Jovan Mitrevski
Columbia University
DØ Trigger Workshop in Saclay
5 November 2002



Introduction

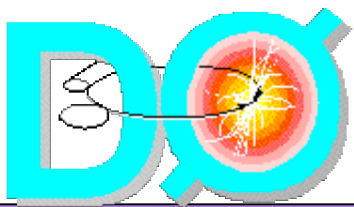


- ◆ At Columbia we built a board to test the National Semiconductor 48-bit LVDS Channel Link chip set for a feasibility study.
 - ◆ DS90CR483 transmitter
 - ◆ DS90CR484 receiver
- ◆ We send the signal over a 5m cable, using only seven of the eight LVDS channels.
- ◆ Although physically one board sends and receives the signals, the transmitter and receiver sides are independent and have separate power and ground.
- ◆ Altera FPGAs control the Channel Link chips on both sides, determining what data gets sent and checking the transmission. The code is written in Verilog. (The TAB coding will be in VHDL due to better support.)



Setup





Zooming in



Board sits upside down on my desk

Switches to set DC-bal. and choose data

Connector to program receiver Altera. Also allows “virtual logic analyzer” SignalTap

Connector to program trans. Altera. Can alternately use ROM.

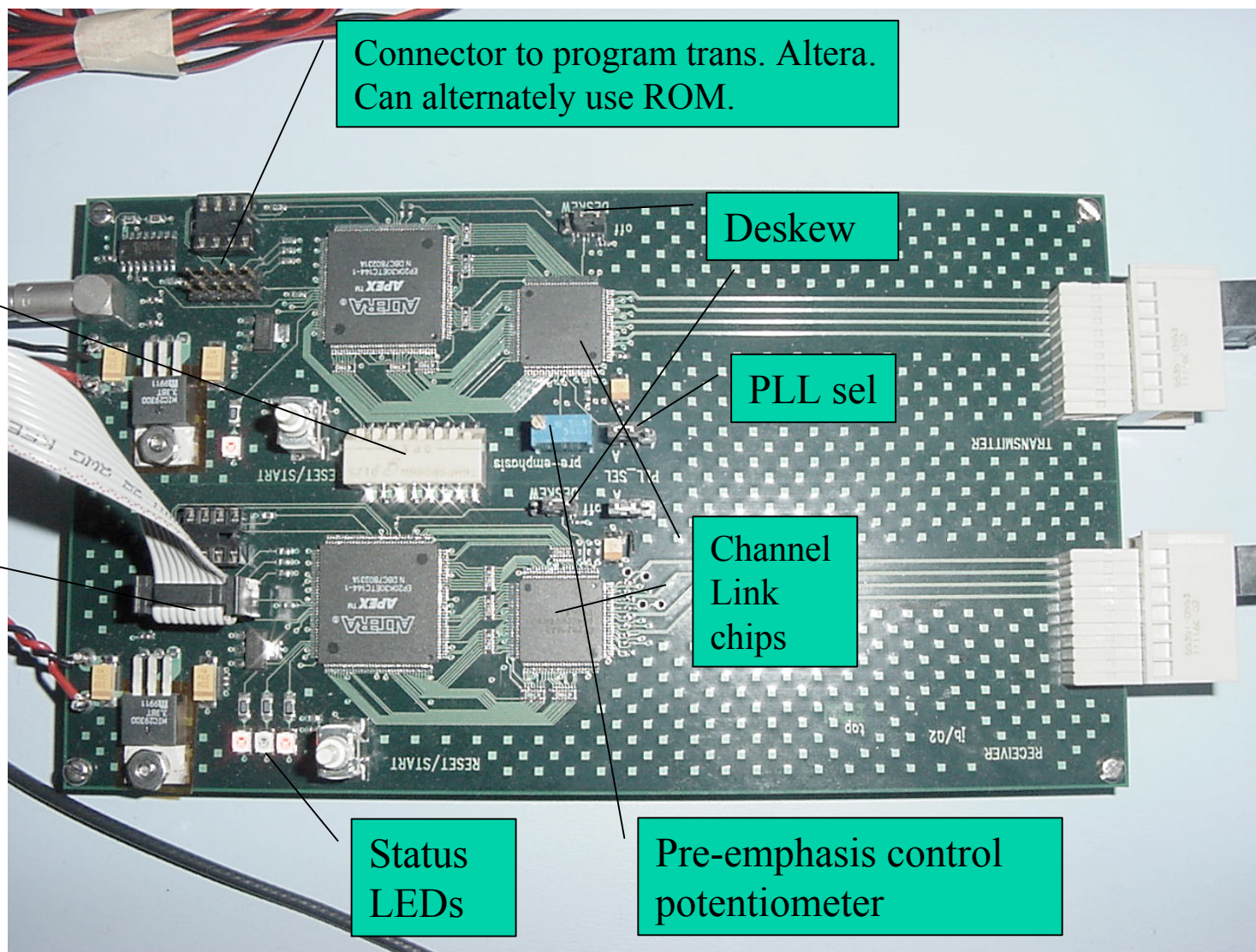
Deskew

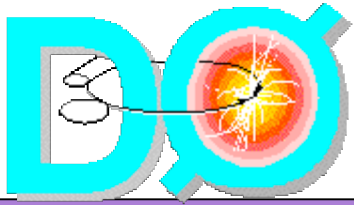
PLL sel

Channel Link chips

Status LEDs

Pre-emphasis control potentiometer

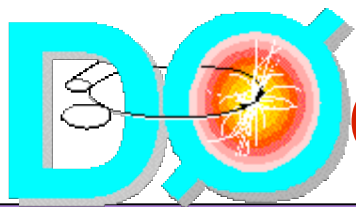




Capabilities of Board



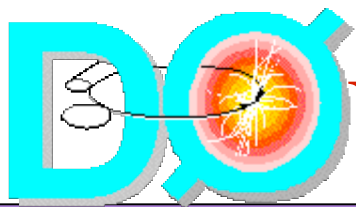
- ◆ The transmitter and receiver are independent, with separate power and ground.
 - ◆ Can test for noise and potential difference on ground, with the understanding that the shielding on the cable connects the two grounds.
 - ◆ Noise on the power levels and drops in voltage can be tested.
- ◆ The PLL range, deskew, DC balance are controlled by switches.
 - ◆ Chips have a new “auto” PLL range setting that is not in the specs that I have.
 - ◆ DC balance control goes through Altera, other switches are direct.
- ◆ Driving strength (pre-emphasis) is controlled by a potentiometer.
- ◆ The board has a clock-in input and two 75 MHz crystals.
 - ◆ Transmitter: can be clocked by external clock or crystal
 - ◆ Receiver FPGA: Can be clocked by “clock out” from the Channel Link or by other crystal.



Capabilities of Board (cont.)



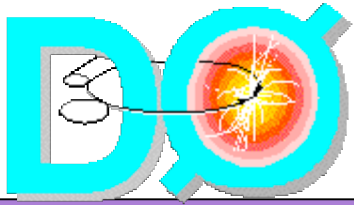
- ◆ The Altera code can be changed, but as it is now, switches control whether all zeros, all ones, AAAs, or pseudo-random data is sent. I have also added a feature that can flip a bit every 30s or so, and parity can be made correct or wrong when the bit is flipped.
 - ◆ Changes in the bit-flipping methodology require recompilation and reloading of the transmitter and possibly receiver code. (The receiver would need to know the policy for data matching.)
- ◆ The receiver currently checks the data both by checking parity and by actual data comparison by knowing what it is supposed to receive based on the transmitted control signals.
- ◆ The receiver counts number of errors, and turns on a LED if an error is found. SignalTap also triggers on an error.
- ◆ Current maximum clock rate is about 95 to 100 MHz, set by the Altera chips, the exact value depending on specifics of the logic and SignalTap tracing.



Very Positive Initial Results



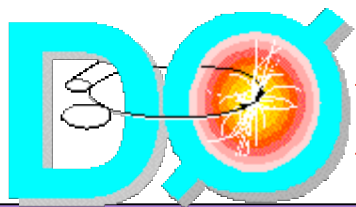
- ◆ Looked at the LVDS signal on an oscilloscope, saw nice eye pattern.
- ◆ Did many runs to measure the error rate; So far, no random errors have been observed, so we have set some limits, which are significantly higher than the supposed specification of 1 error for every 10^{12} bits.
 - ◆ As a check, the receiver code did catch when fake errors were inserted in the transmitter code. Parity errors and data match errors, both individually or together, caused the error count to increase, the error LED to go on, and SignalTap to trigger. A short temporarily inserted on the signal with a screwdriver also causes the many errors to be found and signaled.



Error Rate Measurements



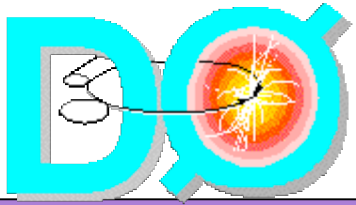
- ◆ Parameters fixed for all testing so far:
 - ◆ PLL Range: auto
 - ◆ Deskew: off
 - ◆ Pre-emphasis: tuned with an oscilloscope
 - ◆ Can make transmission fail by reducing pre-emphasis too much at higher frequencies. The change from no errors to many errors appears to be sharp.
 - ◆ Power to the board is stable, and no noise is introduced to it or the grounds.
 - ◆ Clocking for the transmitter is done with an external tunable signal source.
 - ◆ Clocking for the receiver is from the Channel Link.



Error Rate Measurement (cont.)



Clock (MHz)	Signal type	DC bal	Time run	90% limit, < 1 error in x bits
60	AA and random	Y	4 days 19 h 40 min	2.2×10^{-15}
90	AA and random	Y	1 day 21 h 34 min	3.7×10^{-15}
50	random	Y	1 day 3 h 20 min	1.1×10^{-14}
75	random	Y	2 days 20 h	3.0×10^{-15}
60	random	N	19 h 39 min	1.3×10^{-14}
60	zeros (except for control bit that has one 1 bit) + single inverted bit approx. every 30 s	N	23 h 36 min	1.1×10^{-14}



Conclusion



- ◆ Results look promising, but still a work in progress.
- ◆ Need to check noise immunity on power signal and ground.
- ◆ Any ideas and suggestions would be appreciated.