

Changes to the GAB

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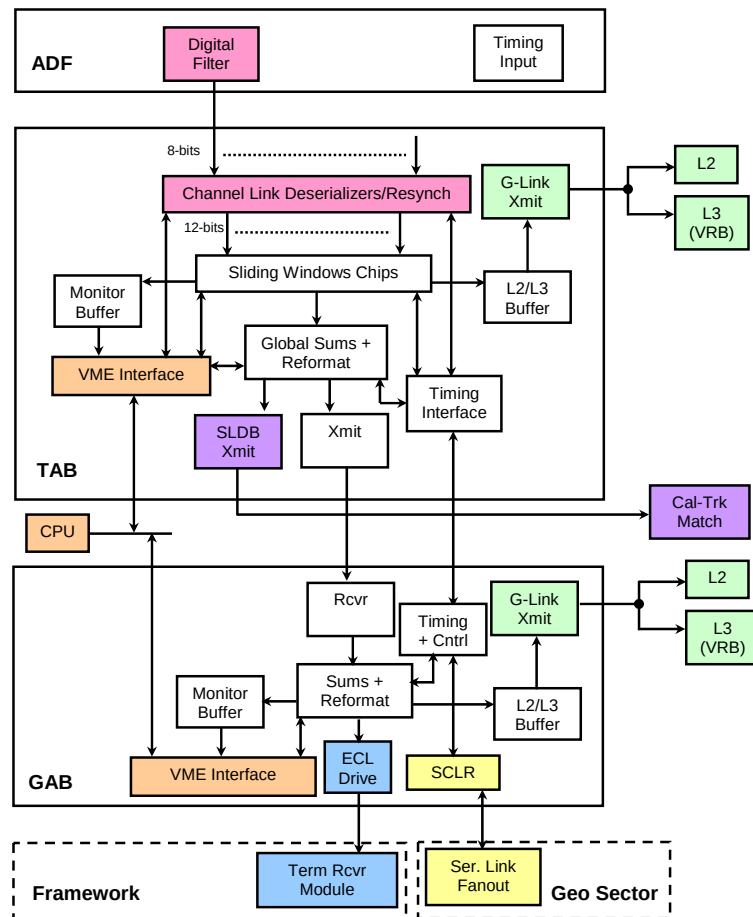
Columbia/Nevis

- **Current System Architecture**
- **Changes to GAB to Streamline this Architecture**
- **How this Affects the Schedule/Costs**

<http://www.nevis.columbia.edu/~evans/l1cal/hardware/hardware.html>

Current TAB/GAB Architecture

16-Jan-03



TAB I/O is Fierce

Signal	I/O	Cables	Where
Power	I	Bus	Rear
ADF TTs	I	30	Rear
Cal-Track	O	3	Front
L2/L3	O	1	Front
Timing (SCL)	I	1	Front
VME	I/O	1	Front

- Lots of Traces on Board
 - 11 768-pin FPGAs +...
- No room for:
 - standard VME
 - SCL mezzanine

GAB (currently) Deals w/ This

1. Trigger Functions
2. VME Interface
3. SCL Interface

VME & SCL to the TAB

Serial VME Interface

- LVDS protocol & same cable/connector type as ADF-to-TAB transmission
- Run at 15 MHz
 - download FPGAs ~10s
 - TAB monitoring ~10ms

Serial SCL Interface

- LVDS & ADF-to-TAB cable
- Run at 7.6 MHz
- Reconstruct BX & TURN on TAB
- Local Clock for testing w/out SCL

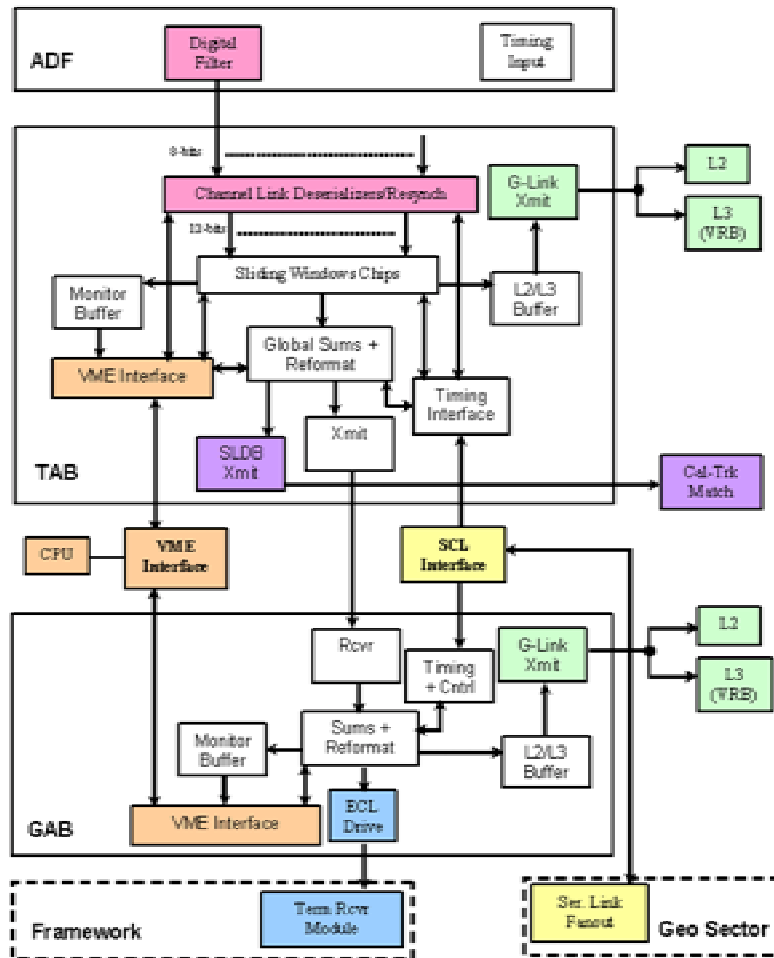
Pair	Description	Pair	Description
<i>ser_clk</i>	link clock	<i>clk7</i>	7.6 MHz clock
<i>ser_frm_in</i>	1 st bit marker + Addr(23:16)	<i>init</i>	init request
<i>ser_addr_in</i>	Addr(15:0)	<i>turn</i>	SCL first_period
<i>ser_data_in</i>	Input Data(15:0)	<i>l1_accept</i>	L1 Accept signal
<i>ser_frm_out</i>	1 st bit marker	<i>pulse</i>	internal synchronization
<i>ser_data_out</i>	Output Data(15:0)	<i>spare</i>	

Testing the TAB Prototype

- **Goal: have TAB ready for July Integration**
- **Problem: TAB Layout Difficult**
 - **Layout Tool (pads) barely up to the Task**
- **TAB Testing Stages at Nevis**
 1. **Electrical/FPGA tests** Signal Tap
 2. **Test Data Readback** VME
 3. **Test Data w/ Simple Timing** Fake SCL
 4. **Output to GAB** GAB
- **Full GAB Functionality not Required until Late in the Game**
- **Solution: Split GAB into Three Boards**
 1. **VME Interface** very simple, 6U?
 2. **SCL Interface** simple, 6U?
 3. **GAB** lives in TAB crate, similar interfaces

The New System

5-Mar-03



Advantages

- **TAB → July Integr. Test**
 - comp's necessary for TAB tests avail. when needed
 - impossible w/out changes
- **Simplifies Design**
 - GAB Layout easier
 - GAB testing easier
 - Maintenance easier

Disadvantages

- **Cost ?**
 - orig: proto=\$12K; prod=\$8K
 - additional cost ~\$4K (fab)
- **Maybe this is an Advantage ?**
 - Engineering ~same
 - Comp's ~same as orig. est.
 - Fabrication signif. easier
 - 6U vme + 9U shell vs 9U vme

Prototype Schedule

Item	Old Sched	New Sched
TAB Assembled	3/14/03	4/25/03
TAB Bench Tested	5/16/03	6/30/03
GAB Assembled	4/11/03	6/24/03
GAB Bench Tested	7/15/03	8/29/03
VME Interface Assembled	—	4/18/03
VME Interface Tested	—	6/30/03
SCL Interface Assembled	—	5/2/03
SCL Interface Tested	—	6/30/03
Start Integration Test	7/16/03	7/16/03
End Integration Test	10/8/03	10/8/03

Production Schedule Unaffected