Changes to the GAB

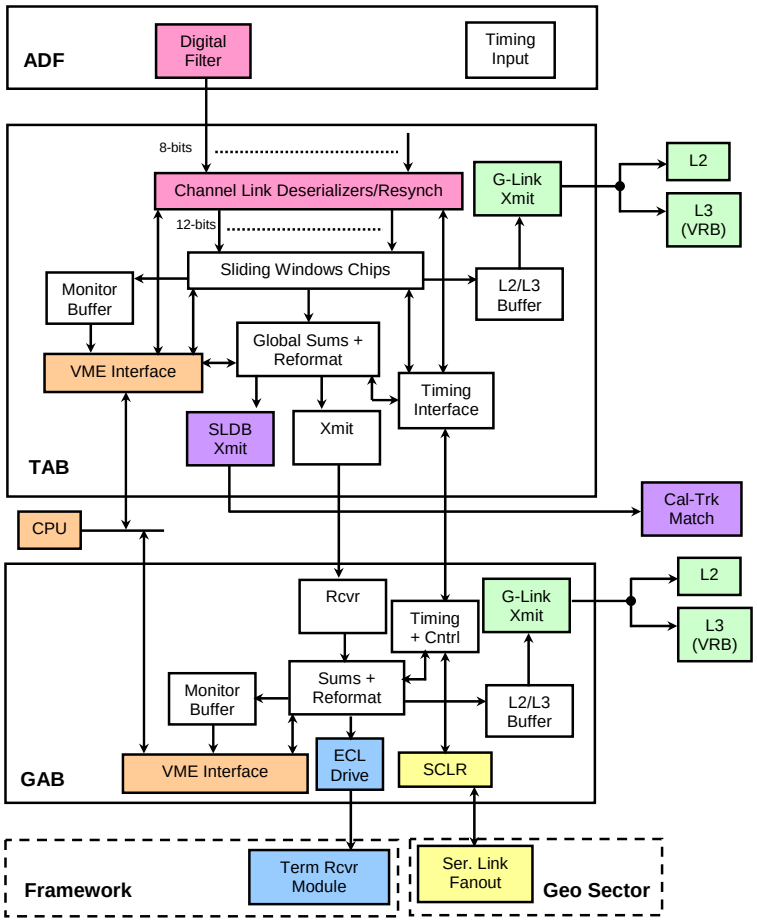
H. Evans **Columbia/Nevis**

- **Current System Architecture**
- **Changes to GAB to Streamline this Architecture**
- **How this Affects the Schedule/Costs**

http://www.nevis.columbia.edu/~evans/l1cal/hardware/hardware.html

Current TAB/GAB Architecture

16-Jan-03



TAB I/O is Fierce

Signal	I/O	Cables	Where
Power	I	Bus	Rear
ADF TTs	I	30	Rear
Cal-Track	O	3	Front
L2/L3	O	1	Front
Timing (SCL)	I	1	Front
VME	I/O	1	Front

- Lots of Traces on Board
  - 11 768-pin FPGAs +…
- No room for:
  - standard VME
  - SCL mezzanine

GAB (currently) Deals w/ This

1. Trigger Functions
2. VME Interface
3. SCL Interface

VME & SCL to the TAB

Serial VME Interface

- LVDS protocol & same cable/connector type as ADF-to-TAB transmission
- Run at 15 MHz
  - download FPGAs ~10s
  - TAB monitoring ~10ms

Serial SCL Interface

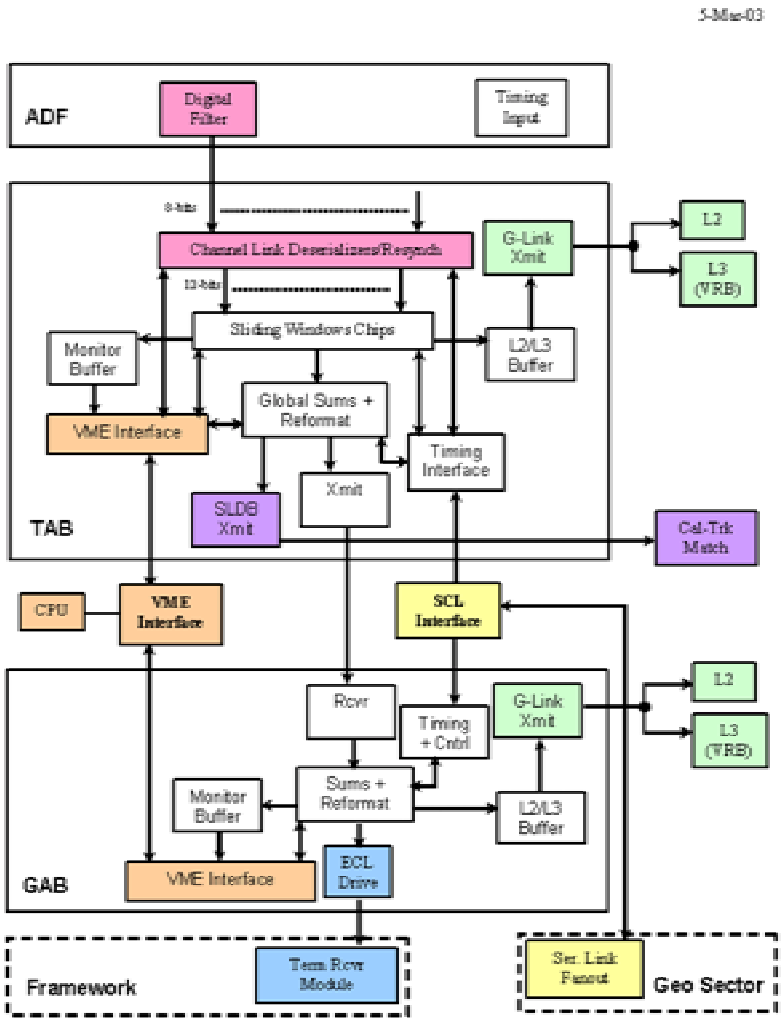
- LVDS & ADF-to-TAB cable
- Run at 7.6 MHz
- Reconstruct BX & TURN on TAB
- Local Clock for testing w/out SCL

Pair	Description	Pair	Description
ser_clk	link clock	*clk7*	7.6 MHz clock
ser_frm_in	1st bit marker + Addr(23:16)	*init*	init request
ser_addr_in	Addr(15:0)	*turn*	SCL first_period
ser_data_in	Input Data(15:0)	*l1_accept*	L1 Accept signal
ser_frm_out	1st bit marker	*pulse*	internal synchronization
ser_data_out	Output Data(15:0)	*spare*	

Testing the TAB Prototype

- **Goal: have TAB ready for July Integration**
- **Problem: TAB Layout Difficult**
  - **Layout Tool (pads) barely up to the Task**
- **TAB Testing Stages at Nevis**
  1. **Electrical/FPGA tests** — **Signal Tap**
  2. **Test Data Readback** — **VME**
  3. **Test Data w/ Simple Timing** — **Fake SCL**
  4. **Output to GAB** — **GAB**
- **Full GAB Functionality not Required until 4)**
  - **integration w/ ADFs only uses 1) – 3)**
- **Solution: Split GAB into Two Boards**
  1. **VME/SCL Interface very simple**
  2. **GAB lives in TAB crate, similar interfaces**

The New System



Advantages

- **TAB → July Integr. Test**
  - **comp's necessary for TAB tests avail. when needed**
  - **impossible w/out changes**
- **Simplifies Design**
  - **GAB Layout easier**
  - **GAB testing easier**
  - **Maintenance easier**

Disadvantages

- **Cost ?**
  - **orig: proto=$12K; prod=$8K**
  - **additional proj cost ~$4K**
- **Maybe this is an Advantage ?**
  - **Engineering ~same**
  - **Comp's ~same as orig. est.**
  - **Fabrication signif. easier**

Prototype Schedule

Item	Old Sched	New Sched
TAB Assembled	3/14/03	5/9/03
TAB Bench Tested	5/16/03	7/15/03
GAB Assembled	4/11/03	6/24/03
GAB Bench Tested	7/15/03	8/29/03
VME/SCL Interface Assembled	—	5/2/03
VME/SCL Interface Tested	—	7/15/03
Start Integration Test	7/16/03	7/16/03
End Integration Test	10/8/03	10/8/03

Production Schedule Unaffected

Current Status

- VME/SCL
  - design ~ done; schematics ~ done; layout started
- TAB
  - layout nearly done; enhanced monitoring added → easier testing

Subsequent discussions

- Examined the possibility/desirability of having other groups design & build one of the new boards (e.g. SCL interface).
- Looked at engineering resources available at Nevis.
- Conclusion: pursue both “GAB” boards at Nevis
  - Best strategy for staying on schedule for Summer integration tests
  - Easier coordination
- First Results
  - Work on VME/SCL Interface proceeding at record pace