Changes to the GAB

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- Current System Architecture
- Changes to GAB to Streamline this Architecture
- How this Affects the Schedule/Costs

http://www.nevis.columbia.edu/~evans/l1cal/hardware/hardware.html
Current TAB/GAB Architecture

16-Jan-03

TAB I/O is Fierce

<table>
<thead>
<tr>
<th>Signal</th>
<th>I/O</th>
<th>Cables</th>
<th>Where</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power</td>
<td>I</td>
<td>Bus</td>
<td>Rear</td>
</tr>
<tr>
<td>ADF TTs</td>
<td>I</td>
<td>30</td>
<td>Rear</td>
</tr>
<tr>
<td>Cal-Track</td>
<td>O</td>
<td>3</td>
<td>Front</td>
</tr>
<tr>
<td>L2/L3</td>
<td>O</td>
<td>1</td>
<td>Front</td>
</tr>
<tr>
<td>Timing (SCL)</td>
<td>I</td>
<td>1</td>
<td>Front</td>
</tr>
<tr>
<td>VME</td>
<td>I/O</td>
<td></td>
<td>Front</td>
</tr>
</tbody>
</table>

- Lots of Traces on Board
  - 11 768-pin FPGAs +...
- No room for:
  - standard VME
  - SCL mezzanine

GAB (currently) Deals w/ This

1. Trigger Functions
2. VME Interface
3. SCL Interface
VME & SCL to the TAB

Serial VME Interface
- LVDS protocol & same cable/connector type as ADF-to-TAB transmission
- Run at 15 MHz
  - download FPGAs ~10s
  - TAB monitoring ~10ms

Serial SCL Interface
- LVDS & ADF-to-TAB cable
- Run at 7.6 MHz
- Reconstruct BX & TURN on TAB
- Local Clock for testing w/out SCL

<table>
<thead>
<tr>
<th>Pair</th>
<th>Description</th>
<th>Pair</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>ser_clk</td>
<td>link clock</td>
<td>clk7</td>
<td>7.6 MHz clock</td>
</tr>
<tr>
<td>ser_frm_in</td>
<td>1st bit marker + Addr(23:16)</td>
<td>init</td>
<td>init request</td>
</tr>
<tr>
<td>ser_addr_in</td>
<td>Addr(15:0)</td>
<td>turn</td>
<td>SCL first_period</td>
</tr>
<tr>
<td>ser_data_in</td>
<td>Input Data(15:0)</td>
<td>l1_accept</td>
<td>L1 Accept signal</td>
</tr>
<tr>
<td>ser_frm_out</td>
<td>1st bit marker</td>
<td>pulse</td>
<td>internal synchronization</td>
</tr>
<tr>
<td>ser_data_out</td>
<td>Output Data(15:0)</td>
<td>spare</td>
<td></td>
</tr>
</tbody>
</table>
Testing the TAB Prototype

• Goal: have TAB ready for July Integration
• Problem: TAB Layout Difficult
  – Layout Tool (pads) barely up to the Task
• TAB Testing Stages at Nevis
  1. Electrical/FPGA tests
  2. Test Data Readback
  3. Test Data w/ Simple Timing
  4. Output to GAB
• Full GAB Functionality not Required until 4)
  – integration w/ ADFs only uses 1) – 3)
• Solution: Split GAB into Two Boards
  1. VME/SCL Interface very simple
  2. GAB lives in TAB crate, similar interfaces
The New System

Advantages
- TAB → July Integr. Test
  - comp’s necessary for TAB tests avail. when needed
  - impossible w/out changes
- Simplifies Design
  - GAB Layout easier
  - GAB testing easier
  - Maintenance easier

Disadvantages
- Cost ?
  - orig: proto=$12K; prod=$8K
  - additional proj cost ~$4K
- Maybe this is an Advantage ?
  - Engineering ~same
  - Comp’s ~same as orig. est.
  - Fabrication signif. easier
Prototype Schedule

<table>
<thead>
<tr>
<th>Item</th>
<th>Old Sched</th>
<th>New Sched</th>
</tr>
</thead>
<tbody>
<tr>
<td>TAB Assembled</td>
<td>3/14/03</td>
<td>5/9/03</td>
</tr>
<tr>
<td>TAB Bench Tested</td>
<td>5/16/03</td>
<td>7/15/03</td>
</tr>
<tr>
<td>GAB Assembled</td>
<td>4/11/03</td>
<td>6/24/03</td>
</tr>
<tr>
<td>GAB Bench Tested</td>
<td>7/15/03</td>
<td>8/29/03</td>
</tr>
<tr>
<td>VME/SCL Interface Assembled</td>
<td>—</td>
<td>5/2/03</td>
</tr>
<tr>
<td>VME/SCL Interface Tested</td>
<td>—</td>
<td>7/15/03</td>
</tr>
<tr>
<td>Start Integration Test</td>
<td>7/16/03</td>
<td>7/16/03</td>
</tr>
<tr>
<td>End Integration Test</td>
<td>10/8/03</td>
<td>10/8/03</td>
</tr>
</tbody>
</table>

Production Schedule Unaffected

Current Status
- **VME/SCL**
  - design ~ done; schematics ~ done; layout started
- **TAB**
  - layout nearly done; enhanced monitoring added → easier testing

H. Evans
D0 PMG: 1-Apr-03
Subsequent discussions

• Examined the possibility/desirability of having other groups design & build one of the new boards (e.g. SCL interface).
• Looked at engineering resources available at Nevis.
• Conclusion: pursue both “GAB” boards at Nevis
  – Best strategy for staying on schedule for Summer integration tests
  – Easier coordination
• First Results
  – Work on VME/SCL Interface proceeding at record pace