

Goals of the Summer Integration Test

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Columbia/Nevis

- **Summer Integration Schedule**
 - 16-Jul-03 – 8-Oct-03
- **Test Infrastructure**
 - what we need & what we will have
- **Global Integration Goals**
 1. Test all Data Links in the L1Cal System for basic functionality
 2. Study Data & Data Transfer Problems
- **Note: this plan will evolve – suggestions welcome!**

<http://www.nevis.columbia.edu/~evans/l1cal/hardware/hardware.html#integration>

Test Infrastructure

- **L1Cal Integration Stand**
 - semi-permanent
 - on sidewalk outside MCH1
 - long-term: assemble full L1Cal system here
- **Infrastruct. (J. Anderson)**
 - Rack(s) & RMI monitors
 - Power/Ground from MCH
 - isolated platform
 - Cabling for:
 - Splitter(s), SCL
 - Ethernet connections
 - Safety review
 - Mainly during shutdown
 - early July
- **We Supply**
 - Crates
 - w/ power supplies & fans
 - Test Equipment
 - Scopes, Logic Analyzers
 - Computers/Software
 - Our prototype cards
 - People to do the testing
- **Information Needed**
 - Power Usage estimates

Links & Testing Priorities

DataPump→ADF	• will be useful during integration	Stage 0
VME/SCL→TAB	• at Nevis	~indep of integration
TAB→GAB	• at Nevis	
SCL→TAB	• availability of SCL signals	Stage 1
VME/SCL→ADF	• kludged interface to ADF	High priority for summer integration
BLS →ADF	• timing from SCL, split signals	
ADF→TAB	• synch between ADF & TAB (VME/SCL)	
	• use ADF test memory	
BLS →ADF →TAB	• synch via SCL	
Latency	• can measure this separately	Stage 2
TAB→Cal-Track	• synch between TAB & Cal-Track	Lower priority for summer integration
	• use TAB test memory	
ADF,TAB→TCC	• TCC interface to ADF & TAB software	
GAB→TFW	• special and/or list	Stage 3
TAB,GAB→L2,L3	• VRBs & VRBCs	Do later
	• mod's to L2,L3 software	

Some Specific Tests

1) BLS Analog Signal Shapes for Digital Filter Studies • using split signals • this is an ongoing test	Stage 0 ~indep of integration
1) Measure Cross-Talk between ADF Inputs • multiple input channels (BLS or DataPump) 2) Data Protocol • goal: can we transmit & receive • this is the basic link test 3) Data Integrity • goal: bit-error-rate measurement in realistic conditions • must have parity checking & error counting in firmware	Stage 1 High priority for summer integration
1) Study Digital Filter with Real System • need sensible filter coefficients?	Stage 2 Lower priority for summer integration
1) Sliding Windows Algorithm with Real Data • 9x9 Trigger Towers Needed • requires ~20 splitters	Stage 3 Do later