Level-1 Calorimeter Trigger (WBS 1.2.1)

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for the Run IIb L1Cal group

Outline

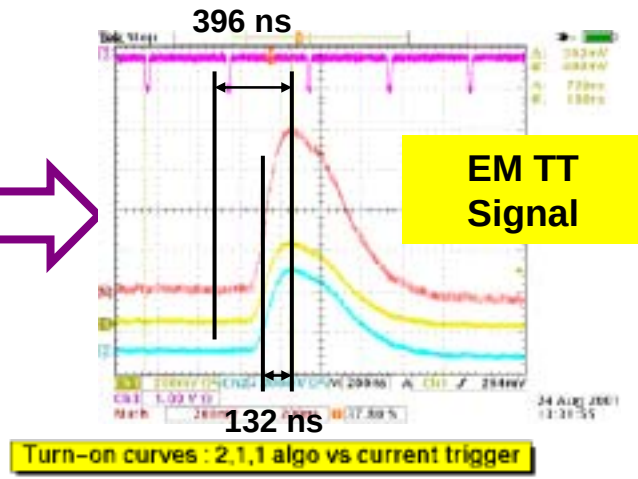
1. Overview & Review
   - System Architecture
   - (Brief) Physics Goals
     - full justification of Run IIb L1Cal: see Lehman Review/TDR
2. Current Status
   - Studies of Data using split signals
   - Data Transmission Studies
   - Roundup of the Prototype Boards
3. Prototype Integration Test
   - Goals of the Test
   - Steps to a Successful Test
4. Getting to the End
   - Progress on the Schedule
   - Projections for the Future

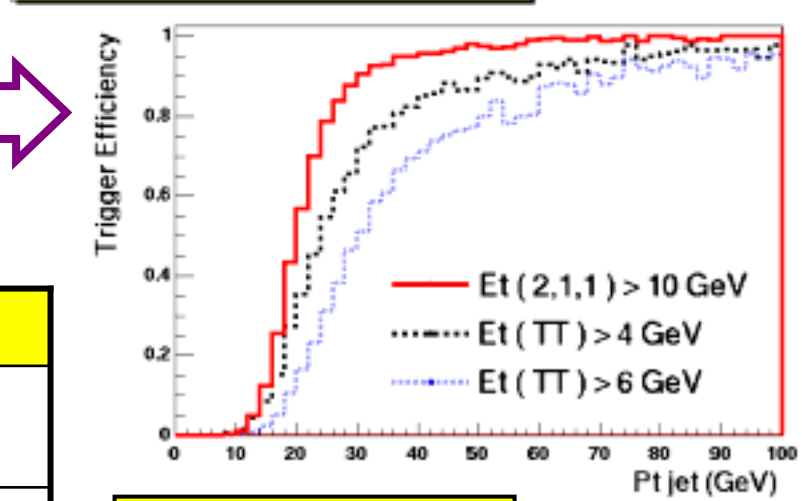
(5. Handy Glossary of Acronyms)

Run IIa Limitations

1. **Signal rise > 132 ns**
   - cross thrsh before peak ⇒ trigger on wrong x'ing
   - affects high-Et events
   - prevents 132 ns running

2. **Poor Et-res. (Jet,EM,MEt)**
   - slow turn-on curves
     - 5 Gev TT thresh ⇒ 80% eff. for 40 GeV jets
   - low thresholds ⇒ unacceptable rates at $\mathcal{L} = 2\times10^{32}$



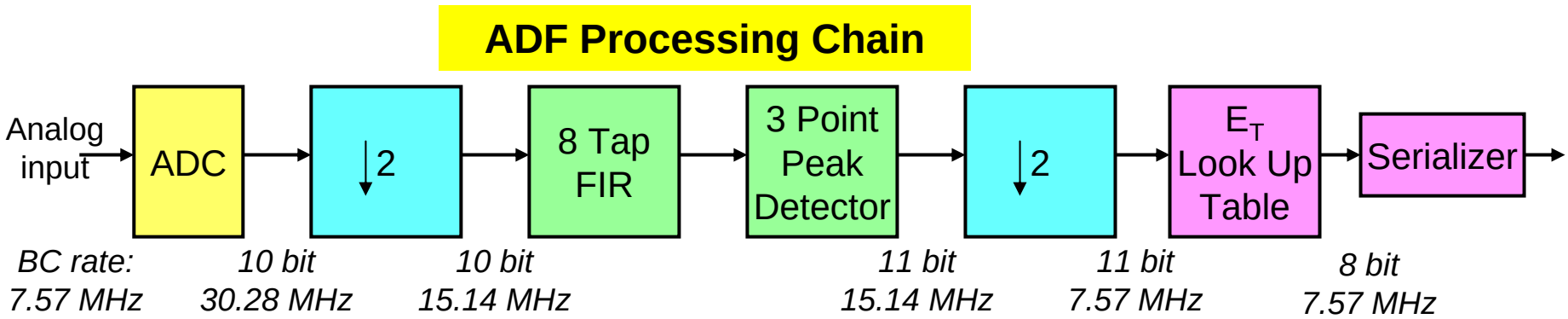


Trigger	Phys. Chan	Rate (kHz)
EM Trigger 1 TT>10 GeV	W → ev	1.3
Jet Trigger 2 TT>5 GeV + MEt>10 GeV	ZH → vvbb	2.1 (L = 2e32)

L1 Rate Limit 5 kHz

Run IIb Solutions (1)

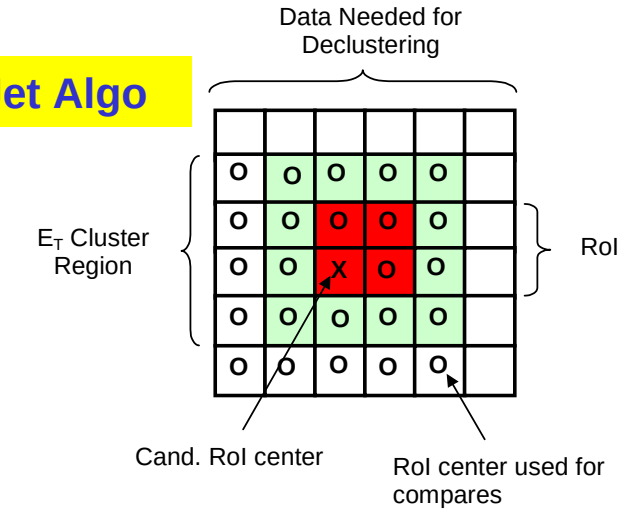
- **Solution to Signal Rise Time: Digital Filtering**
  - digitize Cal trigger signals
  - 8-tap FIR (6-bit coeff's) + Peak Detector run at BC×2
  - reformats output for transmission to physics algo stage
- **Benefits**
  - allows running at 132 ns (keeps this option open)
  - improvements in energy resolution (under study)
  - note: this stage is necessary as input to algo stage



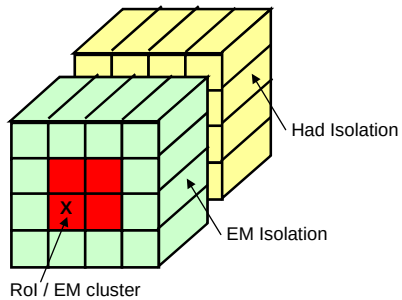
Run IIb Solutions (2)

- **Solution for Rates: Sliding Windows Algo**
  - Et cluster local max. search on 40×32 (η×ϕ) TT grid
  - Jet, EM & Tau algo's
  - Better calc of missing Et
  - Topological Triggers
  - Jet, EM clust output for matching with L1 Tracks
- **Benefits**
  - ×2.5–3 Jet Rate reduction at const. eff.
    - ZH→*νν*bb Rate: 2.1→0.8 kHz
  - Similar gains for EM &Tau
  - MEt, Topological Triggers under study

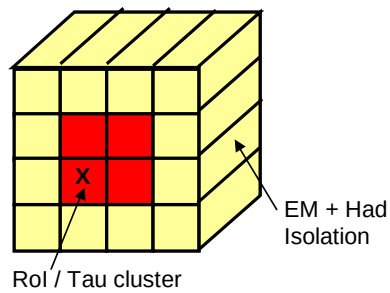
Jet Algo



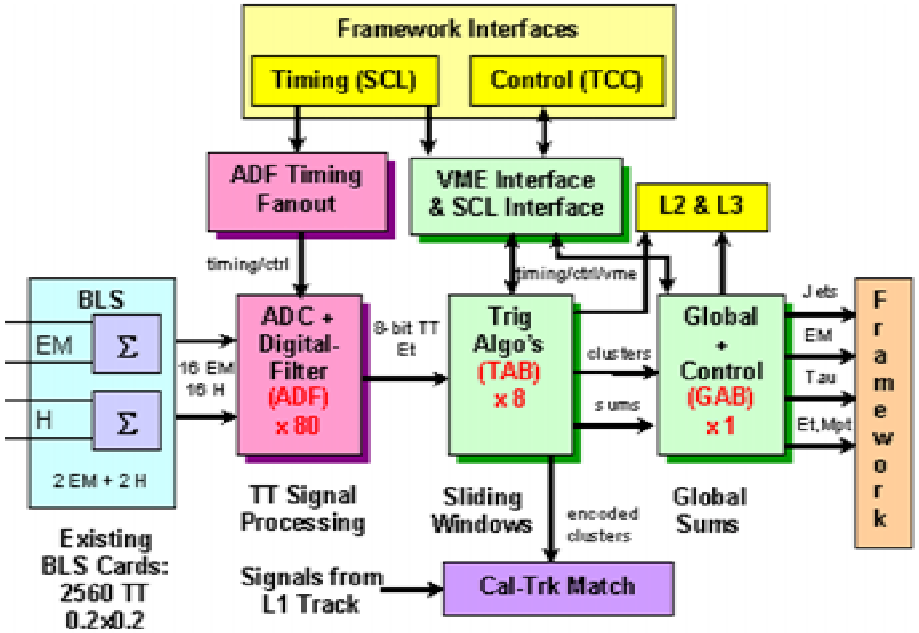
EM Algo



Tau Algo



The Run IIb L1Cal System



Custom Board	No	Purpose
ADF: ACD/Dig. Filt.	80	digitize, filter, E-to-Et
ADF Timing F'out	4	ADF control/timing
TAB: Trig Algo Board	8	algo's, Cal-Trk out, sums
GAB: Global Algo Board	1	TAB ctrl/time, sums, trigs to FWK
VME/SCL Board	1	VME comm & timing f'out to TAB/GAB

Group Responsibilities

Saclay — **ADFs/ADF Timing/Splitters**
- Physicists: J.Bystricky, P.LeDu*, E.Perez
- Engineers: D.Calvet, Saclay Staff

Columbia/Nevis — **TABs/GABs/VME-SCL**
- Physicists: H.Evans*, J.Parsons, J.Mitrevski
- Engineers: J.Ban, B.Sippach, Nevis Staff

Michigan State — **Framework/Online Software**
- Physicists: M.Abolins*
- Engineers: D.Edmunds, P.Laurens

Northeastern — **Online Software**
- Physicists: D.Wood

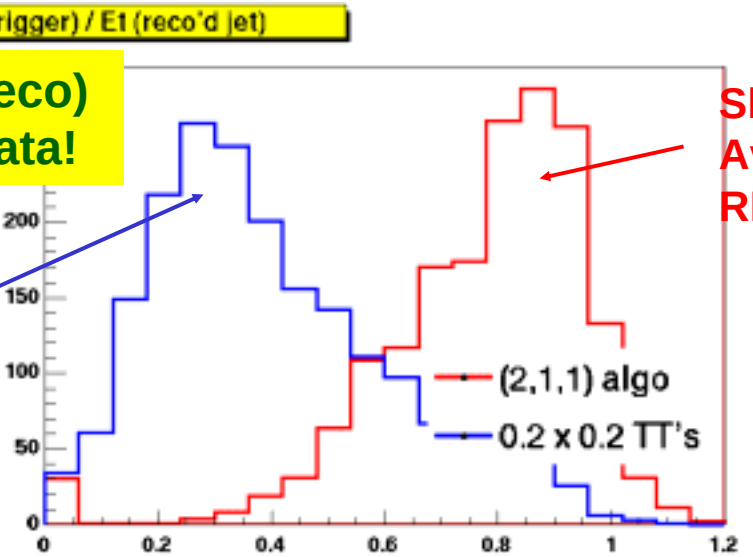
Fermilab — **Test Waveform Generator**
- Engineers: G.Cancelo, V.Pavlicek, S.Rapisarda

Room for Help (actively discussing with several groups)
- Commissioning, Analog Signal Studies, Simulation

*** L1Cal Project Leaders**

Algorithm Studies with Data

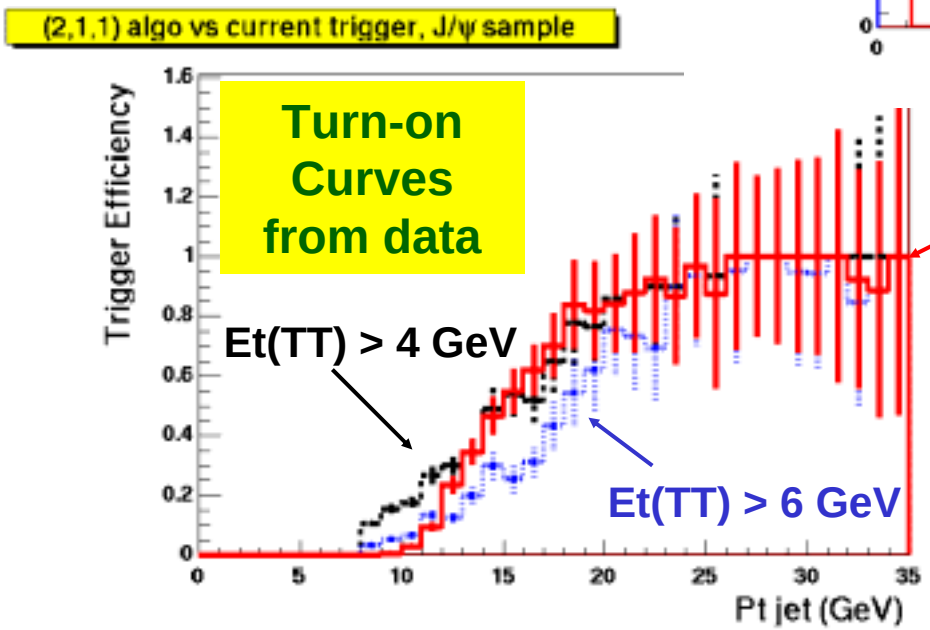
Et(trig) / Et(reco) w/ Run IIa Data!



Sliding Windows
Ave = 0.8
RMS/Ave = 0.2

Run IIa TTs
Ave = 0.4
RMS/Ave = 0.5

Turn-on Curves from data



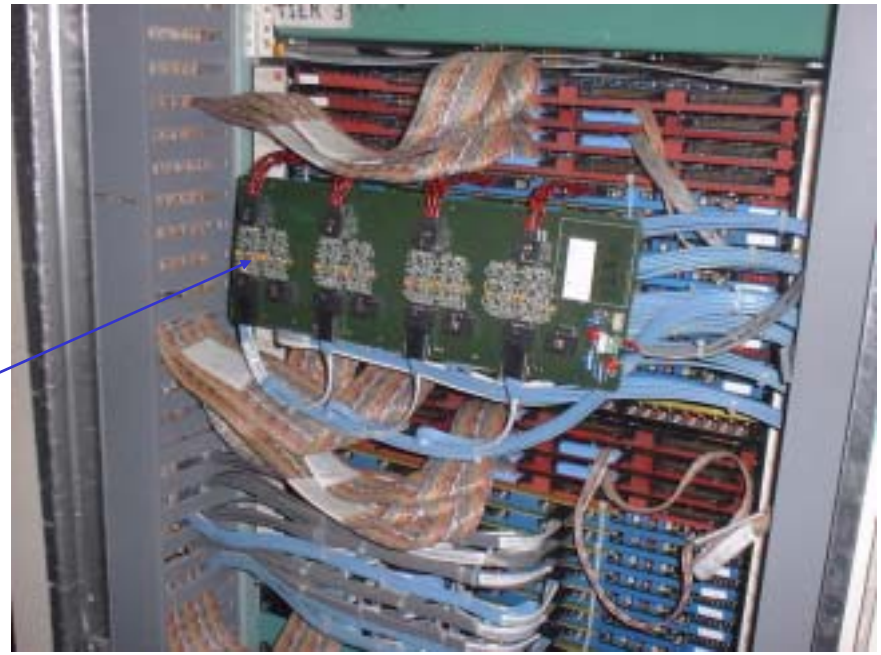
Sliding Windows

Et(TT) > 4 GeV

Et(TT) > 6 GeV

Signal Splitter

- **Access to Real TT Data using "Splitter" Boards**
  - designed/built by Saclay
  - active split of analog signals at CTFE input
  - 4 TTs per board
  - installed: Jan. 2003

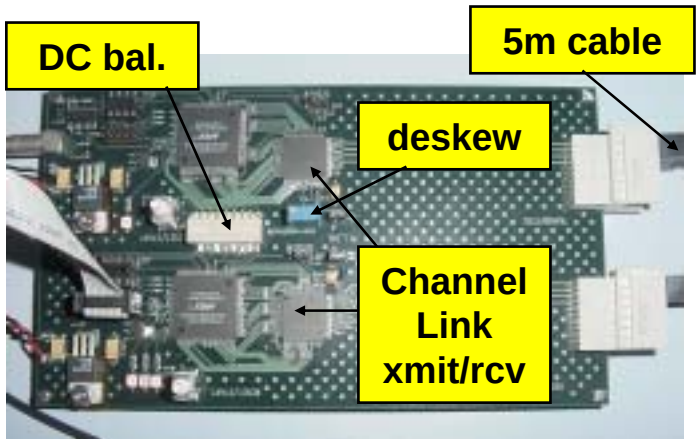


- **Splitter Data**
  - no perturbation of Run IIa L1Cal signals
  - allows tests of digital filter algorithm with real data

splitter data plot here

ADF-to-TAB Signal Xmit

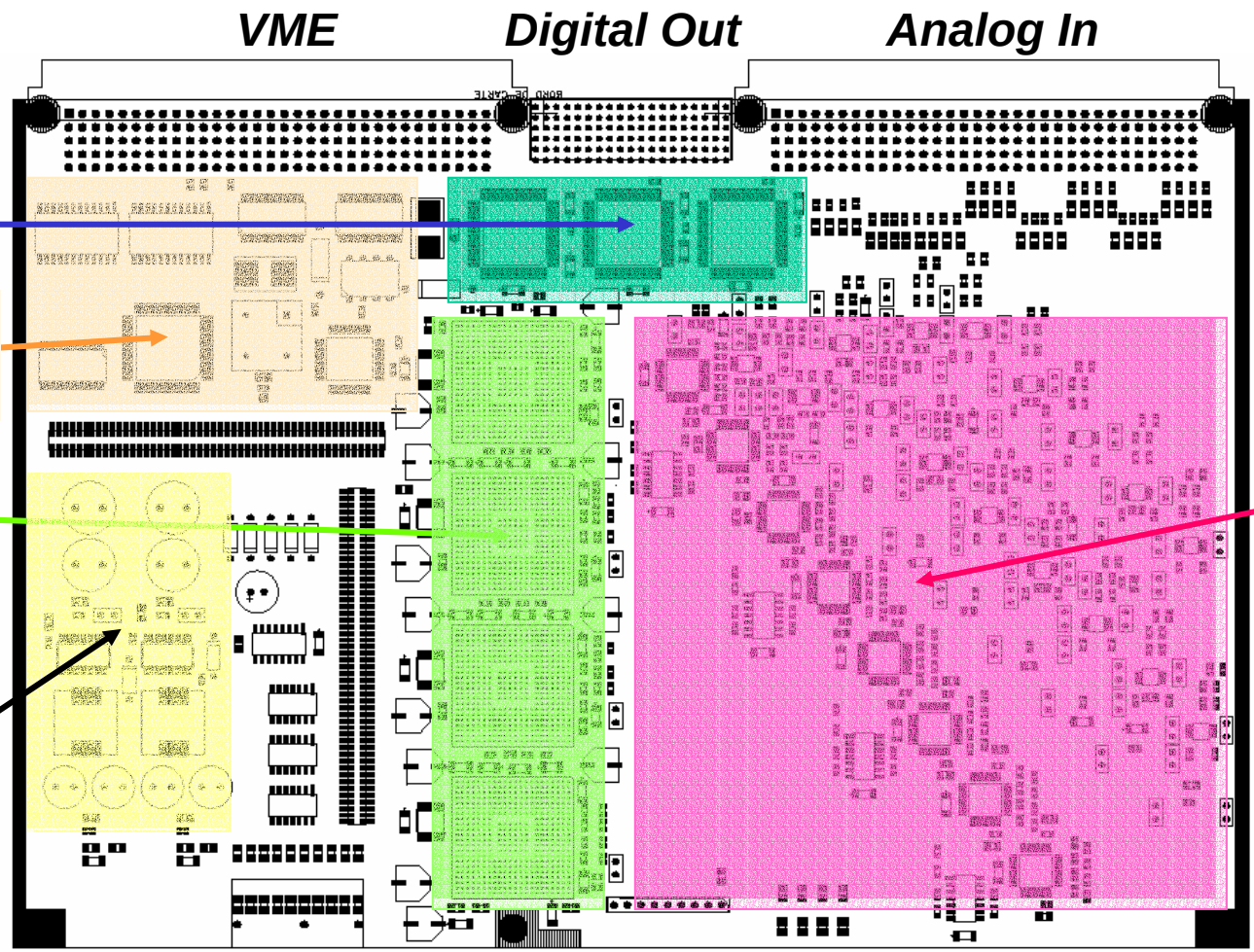
- System Design driven by Data Sharing requirments of Sliding Windows Algorithm
  - 1 Local Max search requires data from 6×6 TTs
  - Minimize Data Duplication ⇒ 30 ADFs (960 TTs) → 1 TAB
- Data Transmitted Serially using LVDS
  - 3 identical copies per ADF
  - Use National Channel Link Chipset (48:8 mux)
    - Links run at 424 Mbit/s (rated to 5.3 Gbit/s)
  - Compact Cables: AMP with 2mm HM connectors



Cable Tester (designed/built at Nevis)

- tests done in fall 2002
- vary param's & clock speeds
- ber's<10^{-14} for 1.5×standard speed

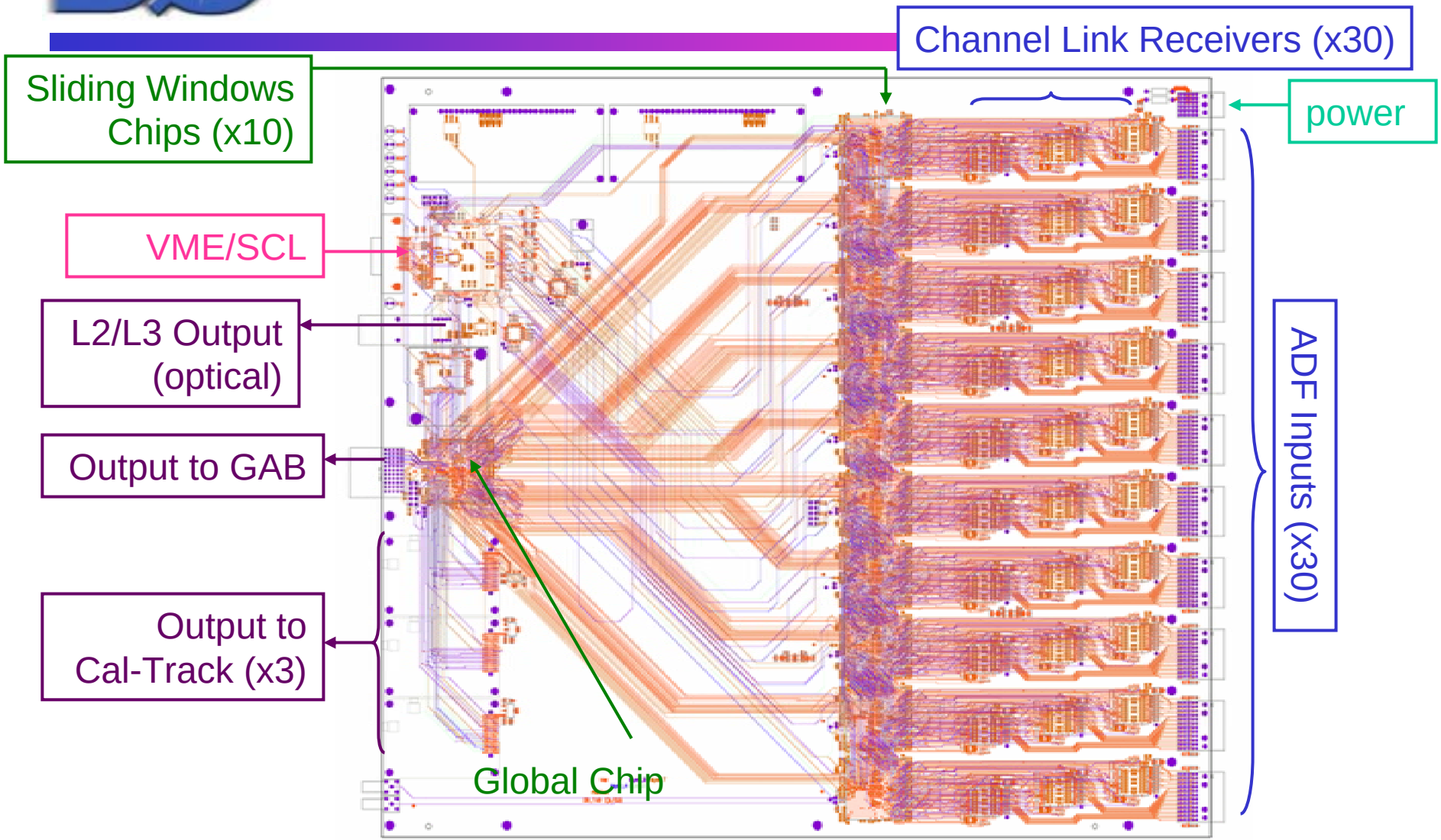
ADF Prototype



~1300 components on both sides of a 14-layer class 6 PCB

Prototype in Fabrication/Assembly: expected at Saclay end-June

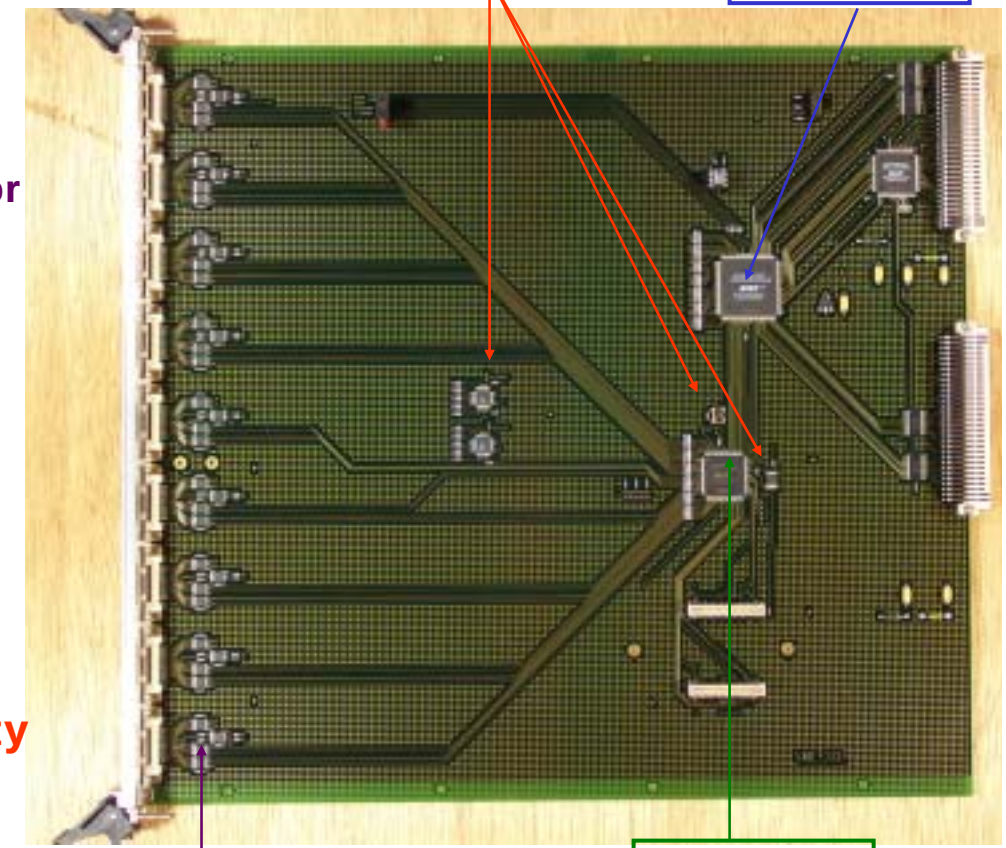
TAB Prototype



Prototype in Fabrication/Assembly: expected at Nevis mid-June

VME/SCL Prototype

- New Comp. of TAB/GAB system
  - proposed: Feb 03
  - change control: Mar 03
- Interfaces to
  - VME (custom protocol)
    - not enough space on TAB for standard VME
  - D0 Trigger Timing (SCL)
  - (previously part of GAB)
- Why Split off from GAB
  - simplifies system design & maintenance
  - allows speedy testing of prototype TAB
- Prototype at Nevis: May 12
  - main VME & SCL functionality tested & working



Prototype Integration Tests

- **Want to start "System Tests" asap**
  - need to check cross-group links early
- **First Tests with Prototypes: Summer/Fall**
  - SCL → VME/SCL → TAB, ADF
  - BLS Data (split) → ADF → TAB
  - Flexible, staged schedule allows components to be included as they become available
- **Setting up semi-permanent Test Area**
  - outside of Movable Counting House
  - connection to SCL, split data signals
  - allows L1Cal tests without disturbing Run IIa data taking
  - infrastructure being set up by J.Anderson's group (Fermilab)
  - power connected to test area during down time last week

Schedule Progress

	Schedule End Dates (Δt from Oct-02 aggressive schedule)			
Prototype	**Design**	**Layout**	**Fab/Assemb**	**Bench Test**
Splitter	3/28/02	8/26/02		1/17/03 (+18w)
ADF	1/24/03 (+9w)	5/16/03 (+19w)	6/30/03 (+18w)	8/26/03 (+17w)
ADF Timing	6/10/03 (+38w)	7/9/03 (+33w)		8/6/03 (+31w)
ADF Crate	6/12/03 (+29w)	8/8/03 (+27w)	10/6/03 (+27w)	12/3/03 (+27w)
ADF-TAB Cables	10/18/02			11/1/02
TAB	1/28/03 (+17w)	5/9/03 (+31w)	6/23/03 (+24w)	7/22/03 (+10w)
GAB	6/24/03 (+31w)	7/23/03 (+31w)	8/20/03 (+22w)	10/16/03 (+14w)
VME/SCL	4/11/03		5/13/03	5/23/03
Prototype Integr.	7/16/03 – 10/8/03			
P.R.R.'s	1/21/04 (ADF…)	11/5/03 (TAB…)	7/16/04 (System)	
Pre-Production	10/30/03 – 7/23/04 (ADF…)		10/9/03 – 4/7/04 (TAB…)	
Pre-Prod Integr.	6/11/04 – 7/9/04			
Production	7/26/04 – 2/21/05 (ADF…)		7/19/04 – 4/11/05 (TAB…)	

What Have We Learned?

- **Schedule Successes**
  - Splitter — crucial for realistic L1Cal tests
  - Cables — demonstration of system viability
  - VME/SCL — modular functions is a wise move simplifies of design/test/mainten.
  - Waveform Gen. — useful card for ADF testing involvement of Fermilab group very helpful
- **Schedule Slips**
  - Main Source of Delays: ADF & TAB Layouts
    - much more complicated than anticipated
    - layout tools stressed by new, large FPGAs
  - Ripple Effect causes Delays in Other Areas
  - Plans in Place to Minimize Effects of Delays
- **What to Watch**
  - Prototype Integration Test is an Important Milestone
  - Need to make sure other boards are fully Integrated
    - GAB, ADF Timing,…
  - Integration of Saclay/Nevis/D0 Online Control Software
  - Need to get More Groups involved in Project
    - commissioning, data studies, simulation

Alphabet Soup

- **ADF: ADC & Digital Filter Card**
  - Run IIb L1Cal card that digitizes and filters analog signals from BLS
- **ADF Timing (aka SCL Interface)**
  - Run IIb L1Cal card that distributes SCL signals to ADFs
- **BLS: BaseLine Subtractor Card**
  - Run IIa/IIb card that constructs analog TT signals from calorimeter cell signals (in collision hall)
- **CTFE: Calorimeter Trigger Front End Card**
  - Run IIa card that digitizes BLS signals, counts TTs over threshold and does first stage of Et summing (in MCH1)
- **GAB: Global Algorithm Board**
  - Run IIb card that collects TAB outputs, constructs trigger terms and transmits them to the TFW
- **LVDS: Low Voltage Differential Signal**
  - Serial data transmission protocol used for communication between Run IIb L1Cal components
- **MCH: Movable Counting House**
  - MCH-1 (1st floor) houses L1Cal. This is accessible during data taking.
- **SCL: Serial Command Link**
  - Means of communicating D0 TFW timing and control signals to all parts of D0 Trigger/DAQ
- **Splitter**
  - Splits analog signals from BLS (at CTFE) for Run IIb L1Cal studies
- **TAB: Trigger Algorithm Board**
  - Run IIb card that performs sliding windows and Et summing algorithms on ADF outputs
- **TFW: Trigger Framework**
  - System that collects trigger terms from all D0 trigger systems, makes final trigger decisions and distributes timing and control
- **TT: Trigger Tower**
  - 0.2x0.2 ($\eta x \phi$) region of calorimeter cells (EM or Hadronic) used as input to L1Cal
- **VME/SCL Card**
  - Run IIb card that interfaces TABs/GABs to VME using a custom serial protocol and distributes SLC signals to the TABs/GABs