First Integration Tests

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- on July 30/31, we successfully performed first phase of Integration Tests of new L1CAL trigger at FNAL
  - VMESCL board was successfully installed and integrated

- thanks to Dan for his support before and during the tests
Integration Tasks

**Infrastructure installation on platform next to MCH**
- Installed rack with 9U (TAB) and 6U (ADC/FIR) VME crates
- Installed Linux-based PC for DAQ, and Windows-based PC for firmware development
- Installed Bit3 VME card in 9U crate
- Installed VMESCL card in 9U crate
- Installed SCL Receiver daughtercard on VMESCL card

**“Offline tests” (using CLK from VMESCL on-board oscillator)**
- Verified can reset VME bus
- Verified communication with VMESCL card
  - Read VMESCL status register
  - Write/read VMESCL scratch registers
  - Switch between Offline and Online modes
Integration Tasks (cont’d)

- **Online tests**
  - Verified proper reception and locking onto SCL CLK in Online mode
  - Verified proper reception and response to SCL signals:
    1. **Initialization**
       - SCL INIT recognized and sent on to TABS (checked with scope since TAB was not installed)
       - VMESCL local bunch crossing counter properly reset by first Turn signal after INIT, and then counts in agreement with lower bits of SCL BCID
    2. **Triggering**
       - L1Periods and L1Accepts recognized
       - L1 trigger properly sent on to TABS for (L1Period AND L1Accept)

- **After successful completion of tests, Bit3 + VMESCL were sent back to Nevis**
  - Will need to be re-installed for next stage of integration tests, including one TAB