ADF PROTOTYPE
MEASUREMENTS ON ADC CHANNELS

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PEDESTAL NOISE - CHANNEL 8 TO 15

Digital output of ADC (logic analyzer); no source connected to ADF analog inputs
Significant noise observed on 4 channels of FPGA#1

Digital output of ADC (logic analyzer); no source connected to ADF analog inputs
Significant noise observed on 4 channels of FPGA#2
**Digital output of ADC (logic analyzer); no source connected to ADF analog inputs**

Significant noise observed on 5 channels of FPGA#3

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**Pulse Response - Channel 0 to 7**

ADF channel input: trigger pickoff-like shape; amplitude: 2.5V (~ 1:2 full scale)

ADC sampling frequency: 32 MHz (8 MHz on-board oscillator x 4) - 31.25 ns period

All channels are satisfactory
PULSE RESPONSE - CHANNEL 8 TO 15

Cabling defect found on channel #14
Some noisy channels

PULSE RESPONSE - CHANNEL 16 TO 23

A couple of noisy channels are found
~half of channels are noisy
Channel #28: improved with bandwidth limiting capacitor (cutoff 7.3 MHz)
Noise introduced by logic analyzer? -> remove it and read ADC data over VME

Limiting Bandwidth - Channel 30

Noise did not come from logic analyzer
Noise significantly reduced without damaging signal
...but should anyway try to improve the situation
**SUMMARY**

**Electrically and logically**
- All 32 channels and ADC's working
- ADC clocks, power-up pin and outputs correctly connected to FPGA’s

**Pedestal noise**
- low on 16 channels; poor on 8 channels; unacceptable on 8 channels
- *Need to understand the cause of the noise and find ways to reduce it*

**Trigger pickoff-like pulse response**
- As expected on all channels (1 cabling defect found)
- but noisy channels are an issue

**Bandwidth limitation**
- Tested: limit to 6 MHz or less bandwidth of 1st order cell on ADC driver feedback loop
- To try: change cutoff of 1st order cell in front of ADC from 15 MHz to 7.5 MHz

*Schematics and logic validated, but improvements needed to reduce noise on some channels (in addition to tuning anti-aliasing filter parameters)*