Measurements on single channel ADF Mezzanine card

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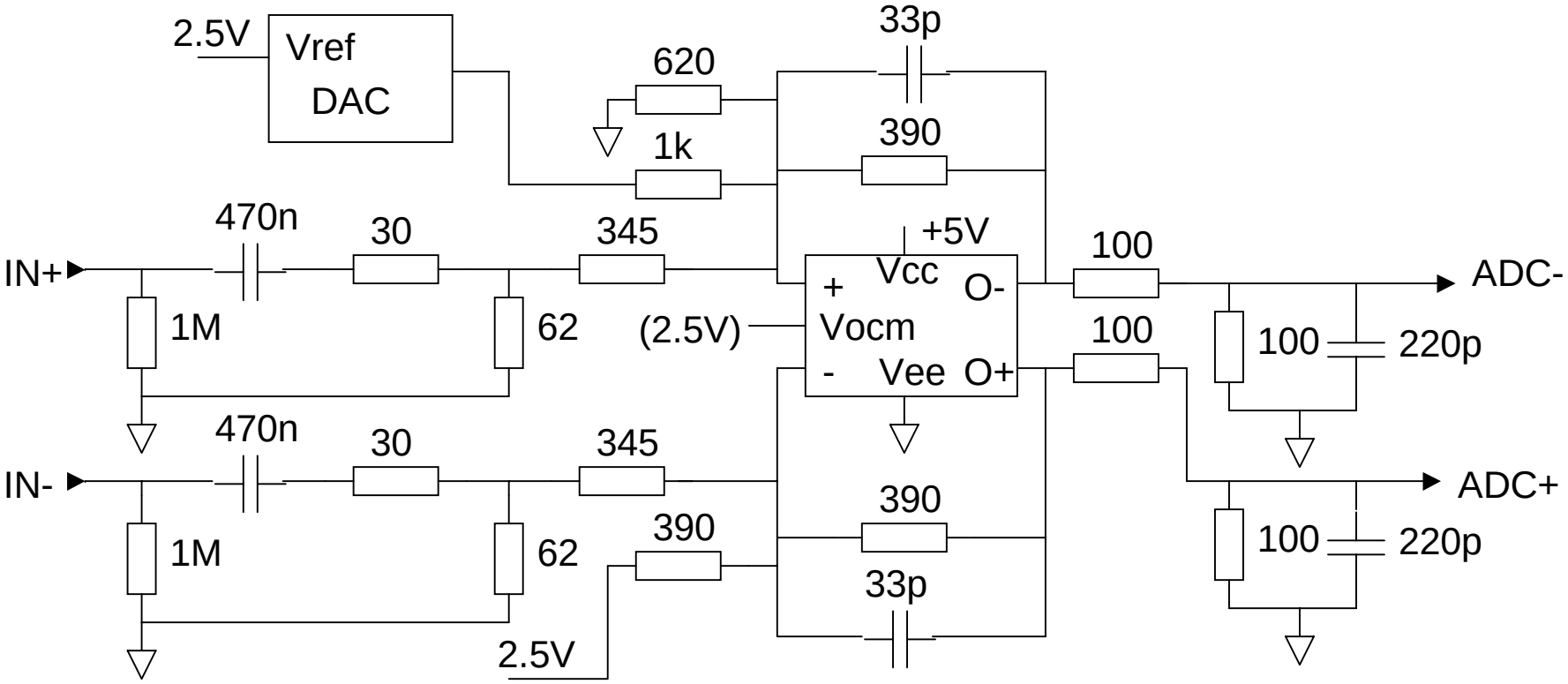
Outline

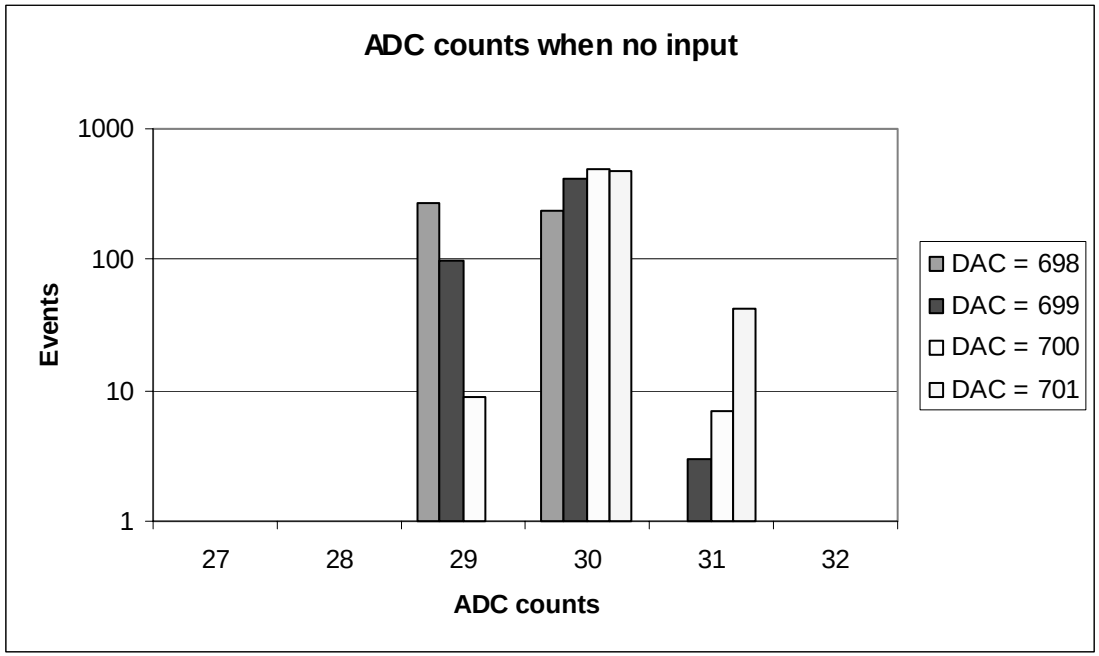
- Schematics of analog section
- Noise measurements
- Common mode rejection test
- Tests with trigger pickoff-like signals

Schematics of Analog Section



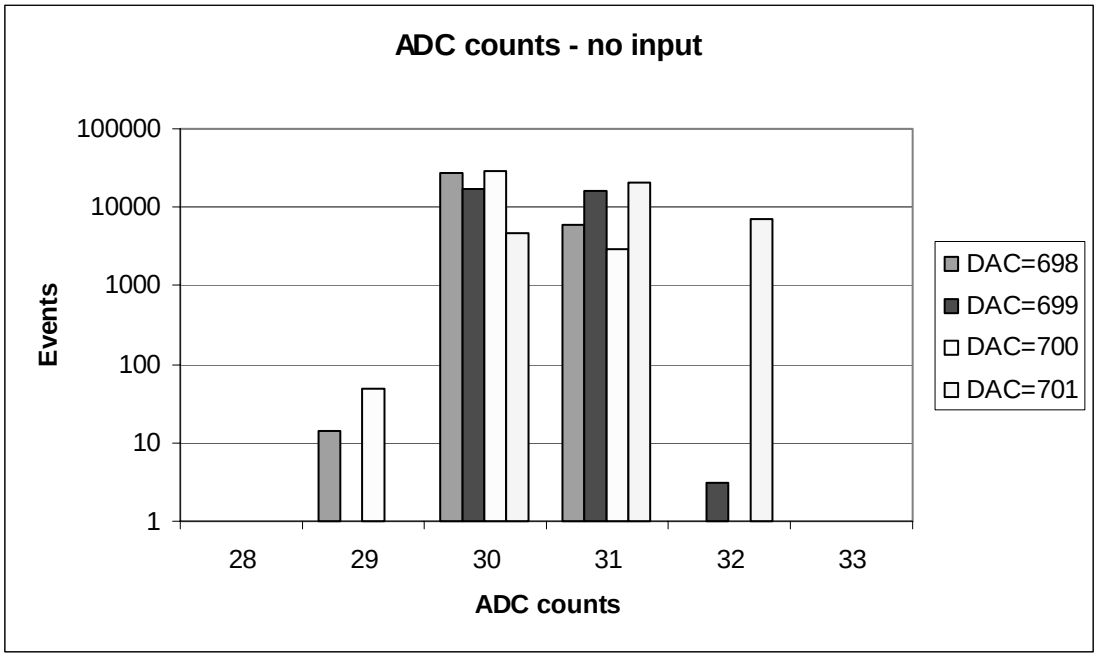
AOP: THS4141
ADC: AD9218 dual 3V3 10 bit 40 Msps (clocked @ 24MHz) 2Vpp dynamic
DAC: MAX 5308
2.5V ref.: on-board regulator now - AOP gain 2 on 1.25V ref out of ADC soon

Noise measurements (con't)



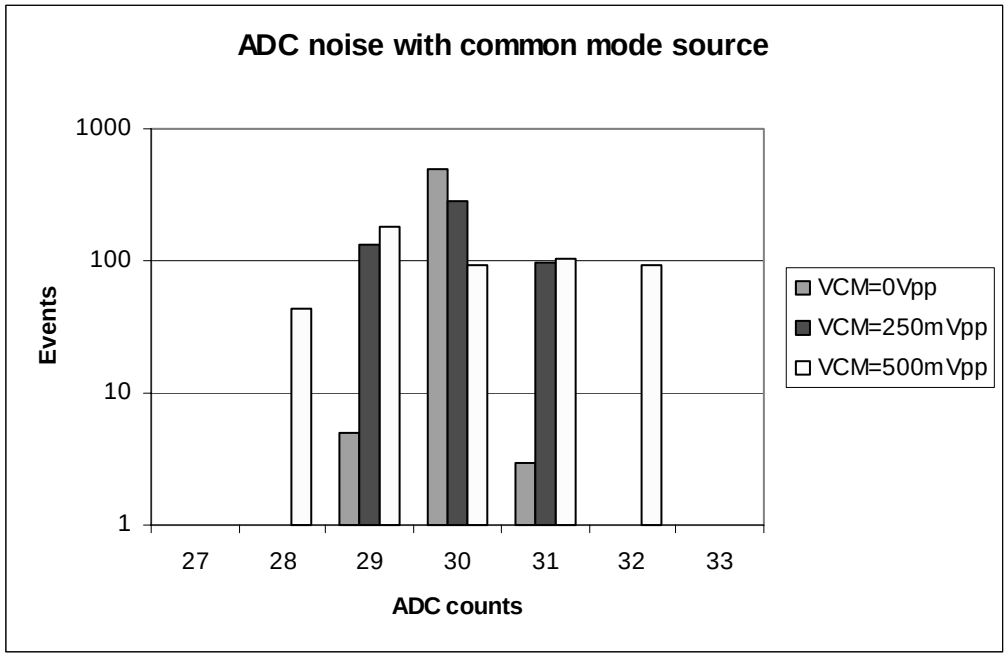
- Measurements without external test equipment - 512 ADC samples captured in on-board history buffer
- Input source unconnected
- ~97% of samples with noise less than +-1LSB

Noise measurements



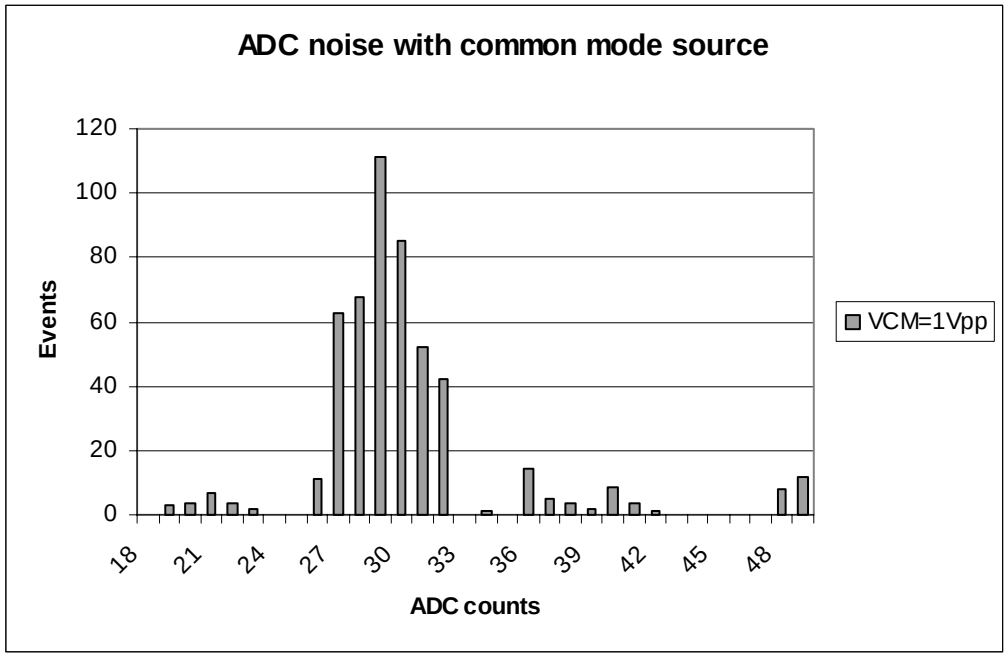
- Measurements with logic analyzer on 32k ADC samples
- Noise added by logic analyzer – but more statistics
- ~90% of samples with noise less than +-1LSB

Common mode input rejection



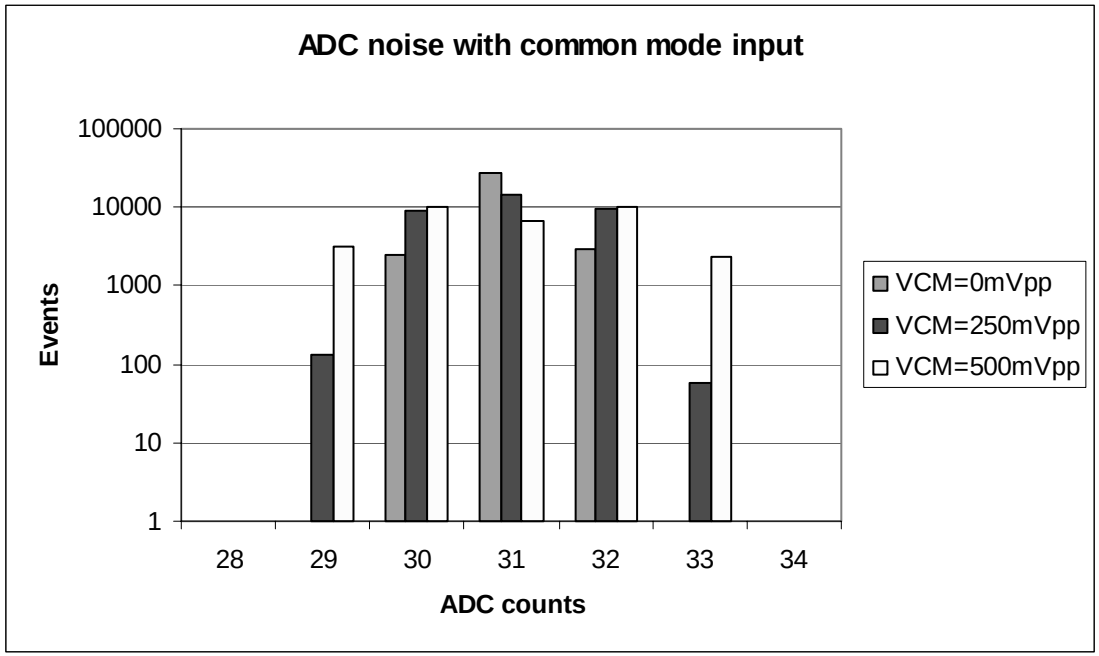
- Measurements without external test equipment - 512 ADC samples captured in on-board history buffer
- Common mode source: sinusoidal , 1MHz

Common mode input rejection



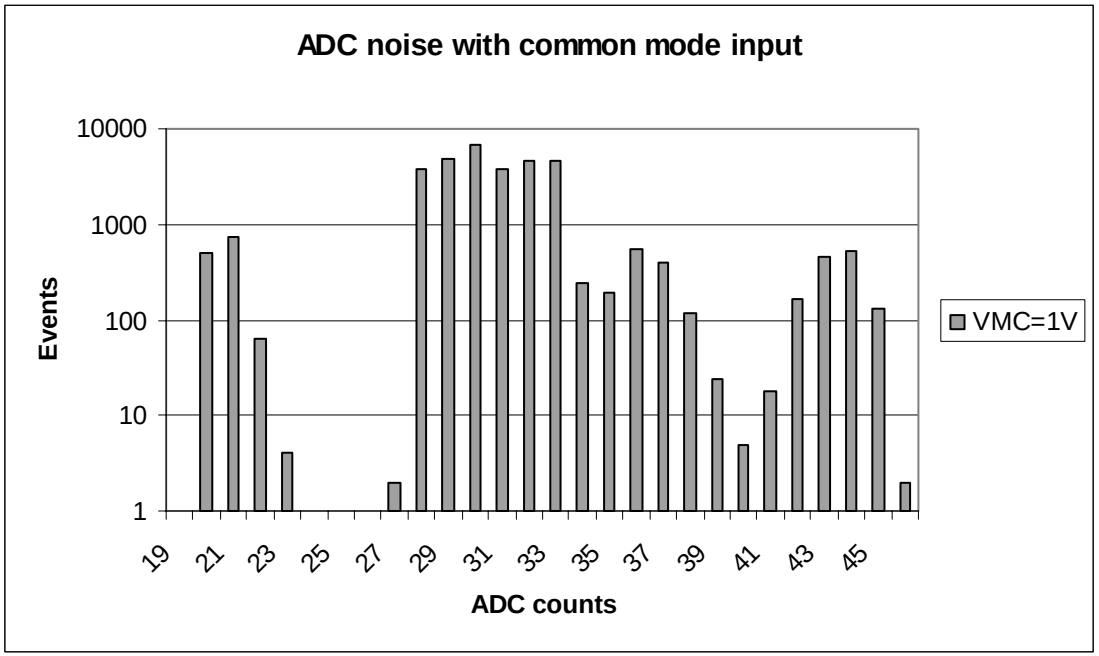
- Measurements without external test equipment - 512 ADC samples captured in on-board history buffer
- Common mode source: sinusoidal , 1MHz
- Large common-mode voltage causes problems

Common mode input rejection



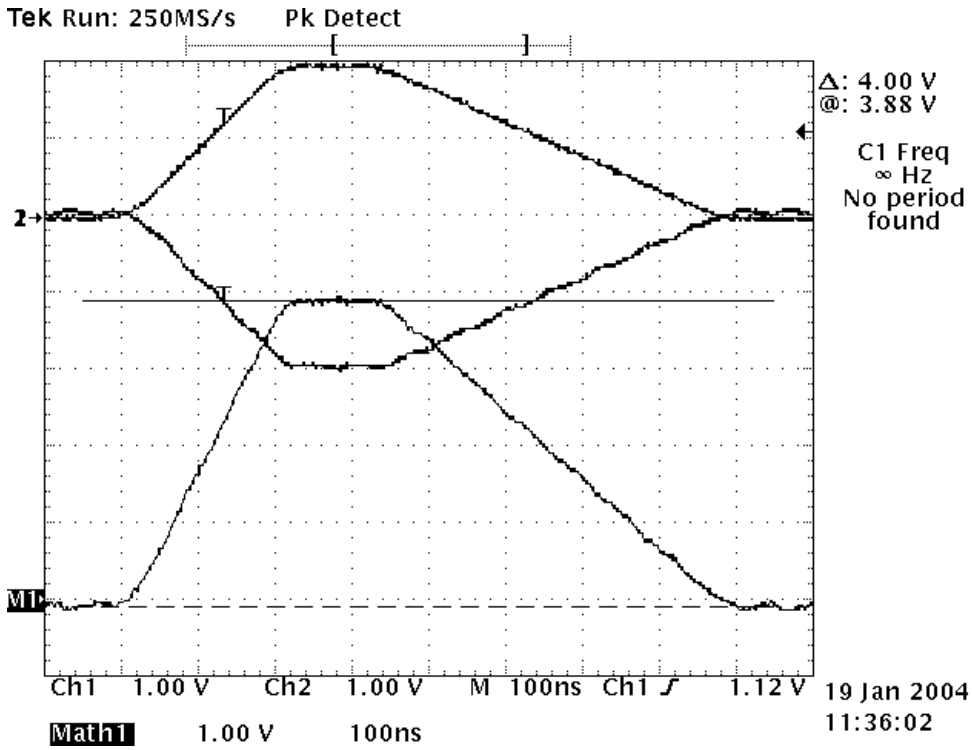
- Measurements with logic analyzer on 32k ADC samples
- Common mode source: sinusoidal , 1MHz
- With Vcm=250mVpp : ~50% of samples have +1 or –1LSB

Common mode input rejection



- Measurements with logic analyzer on 32k ADC samples
- Common mode source: sinusoidal , 1MHz

Trigger pickoff-like input



- Differential source uses 12-bit DAC 40 MHz programmable waveform generator

ADC input to E_T Scale

Eta Index	E (GeV) for Vdiff=2V	E_T (GeV) for Vdiff=2V	Vdiff (V) for 62 GeV ET	ADC LSB (E_T GeV)	LSBs for 0.25 GeV E_T
1	62	62	2	0.18	1.4
8		26	4.7	0.078	3.2
9	175	62	2	0.18	1.4
14		23.3	5.32	0.07	3.6
15	560	62	2	0.18	1.4
19		23	5.4	0.07	3.6

Notes:

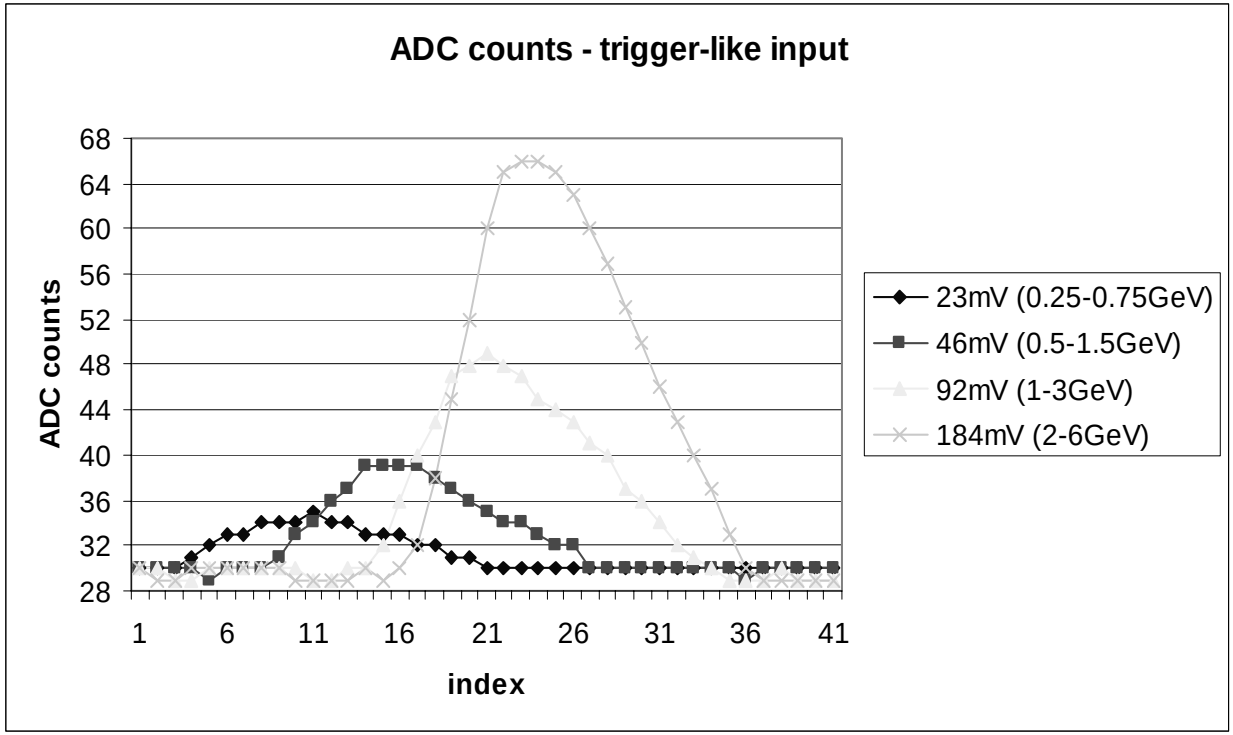
Vdiff : BLS differential peak output voltage with adapted loads connected

Dynamic range for Vdiff: 0 to +6V

Attenuation from BLS output loads to ADC inputs: 3

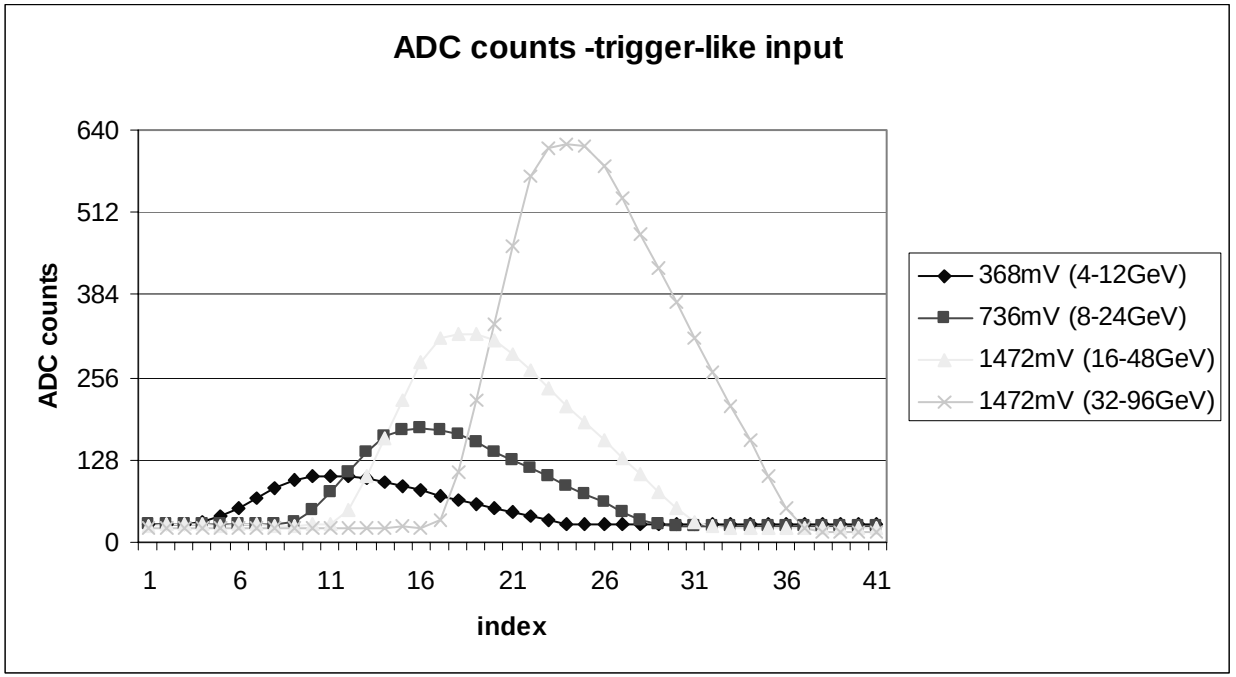
ADC dynamic range: 2Vpp (-1V to +1V) precision: 10-bit

Trigger pickoff-like input



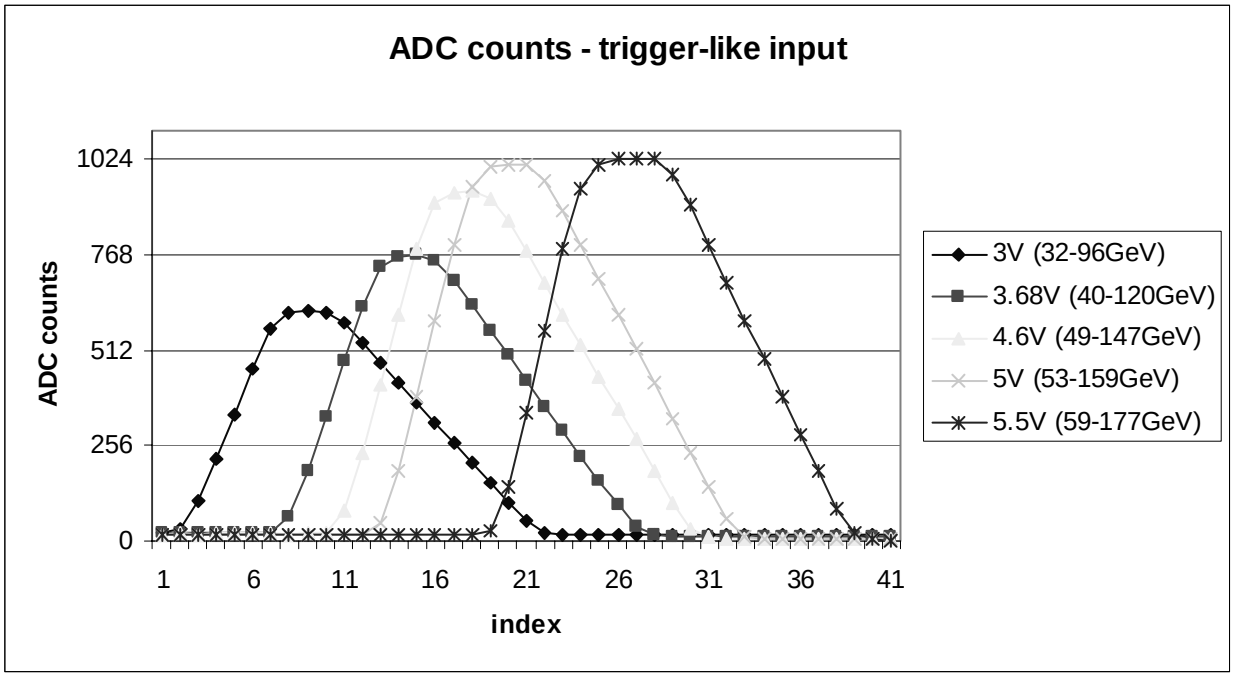
- Measurements without external test equipment - 512 ADC samples captured in on-board history buffer
- 62 GeV E_T = 2 to 6V diff peak at ADF inputs (depending on eta)
  - 0.25 GeV E_T = 8mV to 24 mV ADF input = 2.6mV to 8 mV input of ADC = ~1.3 to 4 LSBs of ADC

Trigger pickoff-like input



- Mid-range measurements

Trigger pickoff-like input



- Setting of 0 level to 30 ADC counts causes saturation ~59 GeV E_T
- Note baseline shifts down when input is increased
- Rather « clean » outputs even at low level:
  - Down to ~1 GeV E_T for the smallest eta of each range
  - Down to ~0.25 GeV E_T for the largest eta of each range

Summary

- Is level of noise acceptable?
- Is common mode input rejection sufficient?
- Is baseline shift an issue?
- Need to repeat measurements on ADF prototype