Channel Link Performance Measurements on ADF board

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Measurement Setup

- ADFv1 board in standalone
- Channel Link Tester board controlled by PC through // I/O board
- High-end oscilloscope
- Bit rate per differential pair: 8 x 8 x 7 = 448 Mbps
Measurement Setup
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Channel Link Tester

- Custom-made Mezzanine board plugged on a commercial Xilinx Virtex II evaluation board
- Control software on PC
- Firmware dedicated to ADF links:
  - 36 bit receive data-path
  - 37-bit ternary trigger pattern (1 external input)
- Data mode:
  - capture up to 2048-frames
  - Deserialize data on each line using FRAME
  - Check received parity
- Error counting mode:
  - Generate pseudo-random sequence similar to that generated by ADF
  - Make bit to bit comparison of data pattern
  - Accumulate bit errors and statistics
Clock at cable end closed on Resistor
Data at cable end closed on Resistor
Link #0 Pair #2 at Tester end
Link #1 Pair #3 at Tester end
Link #2 Pair #5 at Tester end
Non DC Balanced Mode
No DC Balance and No Deskew
DC Balanced – Send fixed data=0x3
No DC Balance – Send fixed data=0x3
DC Bal & DESKEW – Send ADC data
### Explanations on Measurements

- **Channel Link Chipset Configuration**
  - DC balanced mode with DESKEW (unless otherwise specified); no pre-emphasis
  - data rate: 64 MHz x 36 bit = 2.304 Gbps; pseudo-random data; ADC’s enabled

- **End of cable connected to passive resistor termination**
  - Measure skew/eye introduced by ADF board and cable
  - Reference Clock recovered by oscilloscope « golden PLL » from input signal
  - wide-opened eye on clock pair, a bit less on data pairs

- **Cable connected to Channel Link tester board**
  - Adds the degradation introduce by the Channel Link Receiver board circuitry
  - Cannot access clock pair with probe for mechanical reasons
  - Slight degradation of eye pattern but:
    - Wide opening: 1.7 ns of 2.5 ns period (68%); 280 mV vertical opening
    - BER predicted from eye: from $\sim 10^{-24}$ to $\sim 10^{-15}$ depending on pair and cable
  - Correct operation w/wo DC Balance / DESKEW
  - BER influenced by data pattern: random is worst case

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*Other data pairs and the 3 output links of the ADF give comparable results*
Bit Error Rate Measurements

- Validate the operation of the Channel Link Tester
  - Program ADF to generate pseudo-random pattern with e.g. pattern « 000…0 » occurring only once per repetition period (65535 frames)
  - Program tester to record 2K frames after triggering on pattern « 000…0 »
  - Compare received data with expected data off-line
  - Force errors on the ADF side to see if these are detected
  - Re-run all tests in error counting mode

- Make the measurements
  - Program ADF as in previous test and tester to trigger on pattern « 000…0 »
  - Make tester compare received data with expected data on the fly
  - Run for many hours and check error counters

- Results
  - Stopped run after 40 hours on Link #2; $3.10^{14}$ bit transmitted with no error
  - Shorter runs (~15 hours) on others links show correct transmission without error

Stable and reliable operation of ADF links in these test conditions
Suggested Path for Validation of Links

- Operate 1 ADF with clock supplied by SCLD board (on-board oscillator then D0 clock recovered via SCLR Mezzanine)
  - Make sure that clock distribution from D0 to 1 ADF works fine
- Operate 2nd ADF in the same crate
  - Make sure that local clock fanout within a crate works fine

- Measure signals on TAB side
  - See the influence of TAB termination on signals sent by the ADF
  - Investigate cable type/length (ERNI 4 m here; AMP 5 m for final system)
  - Determine if pre-emphasis is needed; determine the level

- Check received data on TAB side
  - ADF can send constant, pseudo-random or pre-stored data patterns
  - TAB must be able to check exactness of data automatically during extended test run periods.

All tests must complete with success before producing final boards