Interim version of the ADF board

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Interim Analog Section

- ADF board prototype: 2 PCBs manufactured
- 1st board now at MSU/Fermilab; 2nd board at Saclay assembled with:
  - Same digital section
  - Analog section: added -5V; changed component values shown in red
Pedestal Adjustment

- Correct range for adjustment of pedestal
- Serial DAC can swing ADC input ~1:2 full range
Noise Measurements

• Importance of de-coupling capacitor clearly visible
• ~70% of samples in 1 bin; 94% of samples in 3 adjacent bins

Cd : de-coupling capacitor on ~5V supply
1 capacitor per 4 Op.Amp. Located ~3 cm from devices
Noise Measurements

Channel #6 - no input

Channel #7 - no input

Cd : de-coupling capacitor on –5V supply
1 capacitor per 4 Op.Amp. Located ~3 cm from devices

• ~40-50% of samples in 1 bin; 70-90% of samples in 3 adjacent bins
Trigger pickoff-like input

- Lower range input signals
- ~1 LSB of noise

Scale: 25 mV diff. Input = 8 mV diff. at ADC = 4 LSBs of ADC = 0.25 GeV to 1 GeV Et (depending on eta)
- Measurements made on Channel #2
Trigger pickoff-like input (2)

- Mid-range input signals
- Correct behavior

Sample index vs. ADC counts

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Saclay 3 June 2004
Trigger pickoff-like input (3)

- Upper-range input signals – saturation due to source
- Globally, correct operation over the tested range
Digital Filter in action

- Impulsion narrowed by digital filter
- Peak detector turned off, but peak would be correctly identified

Filter coefficients: 2 13 23 34 40 29 6 2
Digital Filter in action (2)

- Most of the input noise cleaned up
- Results not very sensitive to coefficient values (i.e. easy to tune)

Filter coefficients: 2 13 23 34 40 29 6 2
## AD 8139 versus THS 4141

<table>
<thead>
<tr>
<th></th>
<th>AD 8139</th>
<th>THS 4141</th>
</tr>
</thead>
<tbody>
<tr>
<td>-3 dB Bandwidth (MHz)</td>
<td>410</td>
<td>160</td>
</tr>
<tr>
<td>Slew rate (V/µs)</td>
<td>800</td>
<td>450</td>
</tr>
<tr>
<td>Noise (nV/Hz$^{1/2}$)</td>
<td>1.85</td>
<td>6.5</td>
</tr>
<tr>
<td>Output swing (V)</td>
<td>0.15 – 4.85</td>
<td>1.3 – 3.7</td>
</tr>
<tr>
<td>+5V single supply</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Vocm range (V)</td>
<td>1 - 4</td>
<td>1 – 4.5 (?)</td>
</tr>
<tr>
<td>Power supply for ADF</td>
<td>Single +5V</td>
<td>+5V –5V</td>
</tr>
<tr>
<td>Package</td>
<td>8 pin SOIC (1.27 mm pitch)</td>
<td>8 pin SOIC or MSOP (0.65 mm)</td>
</tr>
<tr>
<td>Price ($/1k unit)</td>
<td>3.59</td>
<td>3.4</td>
</tr>
</tbody>
</table>

- AD 8139 now in full production
- 2 samples mounted on ADF using wires (1.27 mm pitch -> 0.65 mm PCB)
Noise Measurements

- Channel #10: ~50% of samples in 3 bins – Noise picked-up by cabling? : 98% of samples in 2 bins for this channel in first ADF board
- Channel #14: ~95% of samples in 3 bins – suppressed the ~40 LSBs peak-peak oscillations (mis-interpreted as « noise ») of the THS 4141 powered from single +5V on first ADF board

- Test not possible in optimal conditions
- Noise level to be improved – but is much lower than announced earlier because of erroneous interpretation of measurements on first ADF board
Trigger pickoff-like input

- Scale: 25 mV diff. Input = 8 mV diff. at ADC = 4 LSBs of ADC = 0.25 GeV to 1 GeV $E_t$ (depending on $\eta$)
- Measurements made on Channel #14

- Lower range input signals
- ~2 LSBs of noise

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Trigger pickoff-like input (2)

- Measurements made on Channel #14

- Mid-range input signals
Trigger pickoff-like input (3)

- Saturation of the source ~5.5V
- Measurements made on Channel #14

- Upper-range input signals
- Correct operation with single +5V supply

Should reconsider the choice of dual supply THS 4141 vs. single supply AD 8139 for ADFv2
ADF latency – sending raw ADC data

Trace 2: analog input signal (not synchronized with clock of ADF board)
Trace 1: MSB of data after de-serialization on Channel Link Tester board

Subtract from measurement: Channel Link Receiver latency + Tester latency = 125 + 50 ns = 175 ns

• ADF sending raw ADC outputs: end-to-end latency = 400 ns (from peak of analog input to MSB of data present at end of output cable)
ADF latency – with digital filter

ADF latency projected in 2002: 1 µs for typical coefficients
Measured: 1.055 µs – Difference with projection: 55 ns
Reason: 2 extra pipeline stages in ADF (31 ns); extra 24 ns not clearly explained

• With digital filter: end-to-end latency = 0.87 µs to 1.23 µs (depends on coeff.)
ADF latency adjustment

- Per channel coarse latency adjust: add 0, 1, 2, 3 BC period(s)
- Per 8 channel fine latency setting to add 0 to 7/8\textsuperscript{th} of BC period

Trace 2: analog input signal (not synchronized with clock of ADF board)
Trace 1: MSB of data after de-serialization on Channel Link Tester board
Filter coefficients: 63 63 0 0 0 0 0 0 – Coarse latency set to 0, 1, 2 and 3
## Power Consumption per ADF board

<table>
<thead>
<tr>
<th>Power Supply</th>
<th>I power-up (A)</th>
<th>I standby (A)</th>
<th>I active (A)</th>
<th>I estimated (A)</th>
</tr>
</thead>
<tbody>
<tr>
<td>+5V</td>
<td>0.4</td>
<td>0.8</td>
<td>1.4</td>
<td>2.6</td>
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<tr>
<td>+3.3V</td>
<td>0.4</td>
<td>0.28</td>
<td>1.43</td>
<td>2.1</td>
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<tr>
<td>-5V*</td>
<td>0.45 (56 mA)**</td>
<td>0.45 (56 mA)**</td>
<td>0.45 (56 mA)**</td>
<td>0.64</td>
</tr>
</tbody>
</table>

I power-up: DC current when board not configured
I standby: DC current when board is configured but main logic is disabled
I active: DC current with all ADC’s and logic active
I estimated: DC current estimated during design (datasheets, Xilinx power estimation tool…)
*: power supply not used if AD 8139 are used instead of THS 4141
**: value measured with 4 THS 4141 ADC drivers on-board (32 on the complete board)

• Total dissipation per board: 14 W
Bit Error Rate Measurements

- Continued tests with Channel Link Tester board
  - ADF board uses 8 MHz beam crossing clock derived from 64 MHz local oscillator
  - Test made on link at the farthest end of the connector
  - Stopped run after 4.5 days without any error
  - Transferred ~9 x 10^{14} bit
  - BER < 3 x 10^{-14} with 95% confidence level

Stable and reliable operation of ADF links

Longer tests not planned in this configuration
# Project Documentation

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<th>Software</th>
<th>Test report</th>
<th>User’s guide</th>
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<td>Single channel ADF</td>
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<td>SCLD Board</td>
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<td>Single Channel SCLD</td>
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<td>Channel Link tester</td>
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<td>Cable harness</td>
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</tbody>
</table>

Legend: ■: completed  ★★★: in progress  ★★★★: planned

- 3 documents completed among 9 planned
- Minimal/detailed documentation depending on usefulness
Summary

• All tests now done for single standalone ADF board configuration
  • Firmware/software debugged; all functionality tested and verified
  • All known problems either solved or understood
• Minimum required changes on ADF:
  • Replace the now obsolete VME bridge by equivalent CPLD logic,
  • Make safer distribution of 7.57 MHz clock over backplane (currently 24 mA buffer from FPGA),
  • Simplify analog section (suppress 2 resistors per channel, replace voltage follower Op amps by DC reference chips, etc.)
  • Replace THS 4141 by AD 8139 (after validation in-situ)
  • Re-design analog section to reduce noise; re-layout the board
  • Many minor changes: resistor values, change elements placed for prototyping (remove VME interface debug connector, replace through hole capacitors on anti-aliasing filters by surface mount devices, etc.

• Next contributions: complete documentation and work on SCLD board