TAB & GAB Production Readiness Review

Hal Evans **for the Nevis Group**

In a Nutshell

- We have the components, the boards, the money…
- Should we assemble the TABs and GABs?

Concentrate on

- Hardware Design & Testing ⇒ Production Readiness

Less Emphasis

- Project Justification, Algorithm Devel, Install/Commission

The Nevis Team

Students

Chad Johnson, Jovan Mitrevski

Postdocs

Sabine Lammers, TBA

Engineers

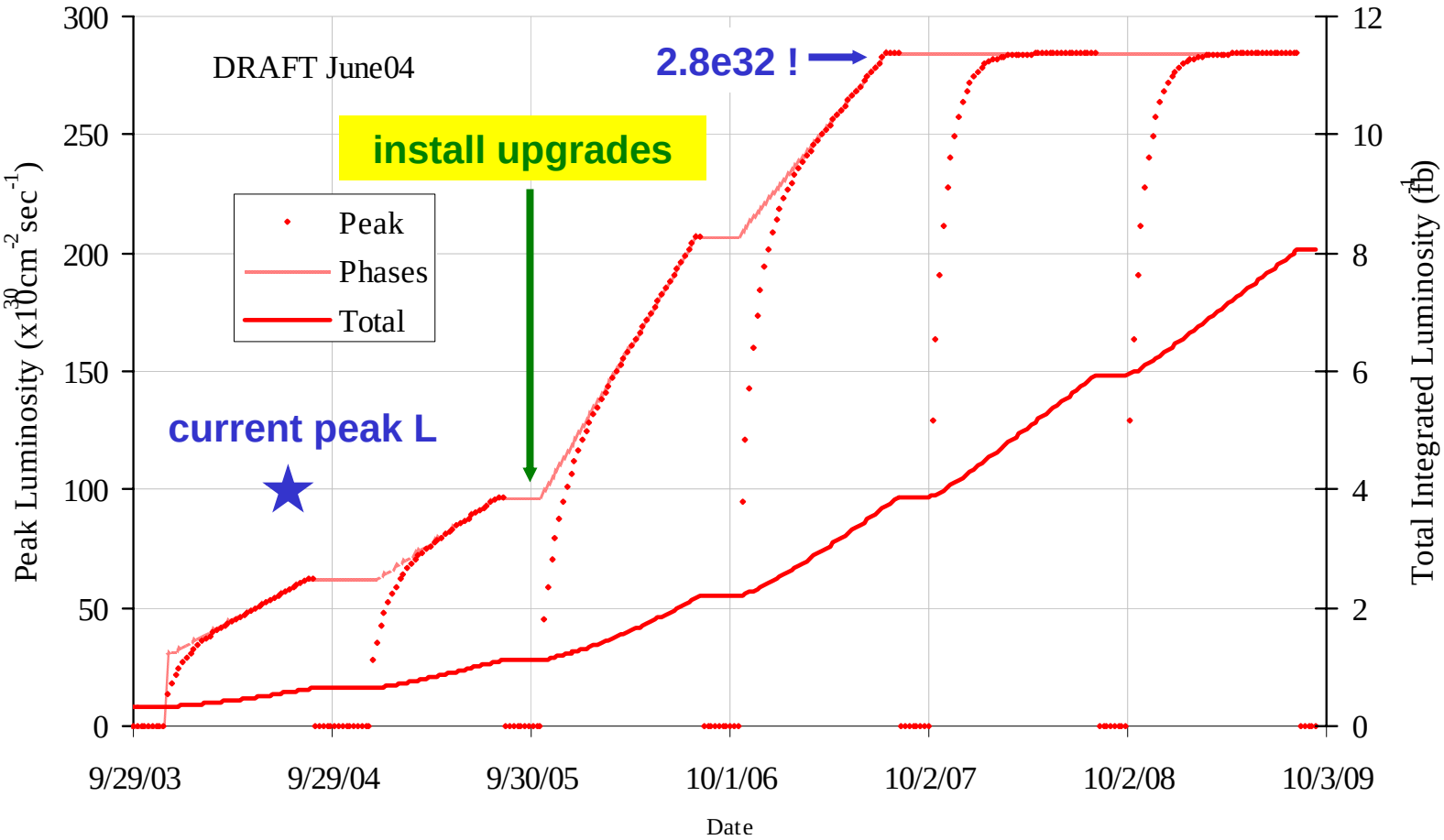
Jaro Ban, Bill Sippach + Nevis Tech's

Faculty

Hal Evans, John Parsons

The Tevatron Landscape

Accelerator Plan: FY 05-09



Trigger Challenges

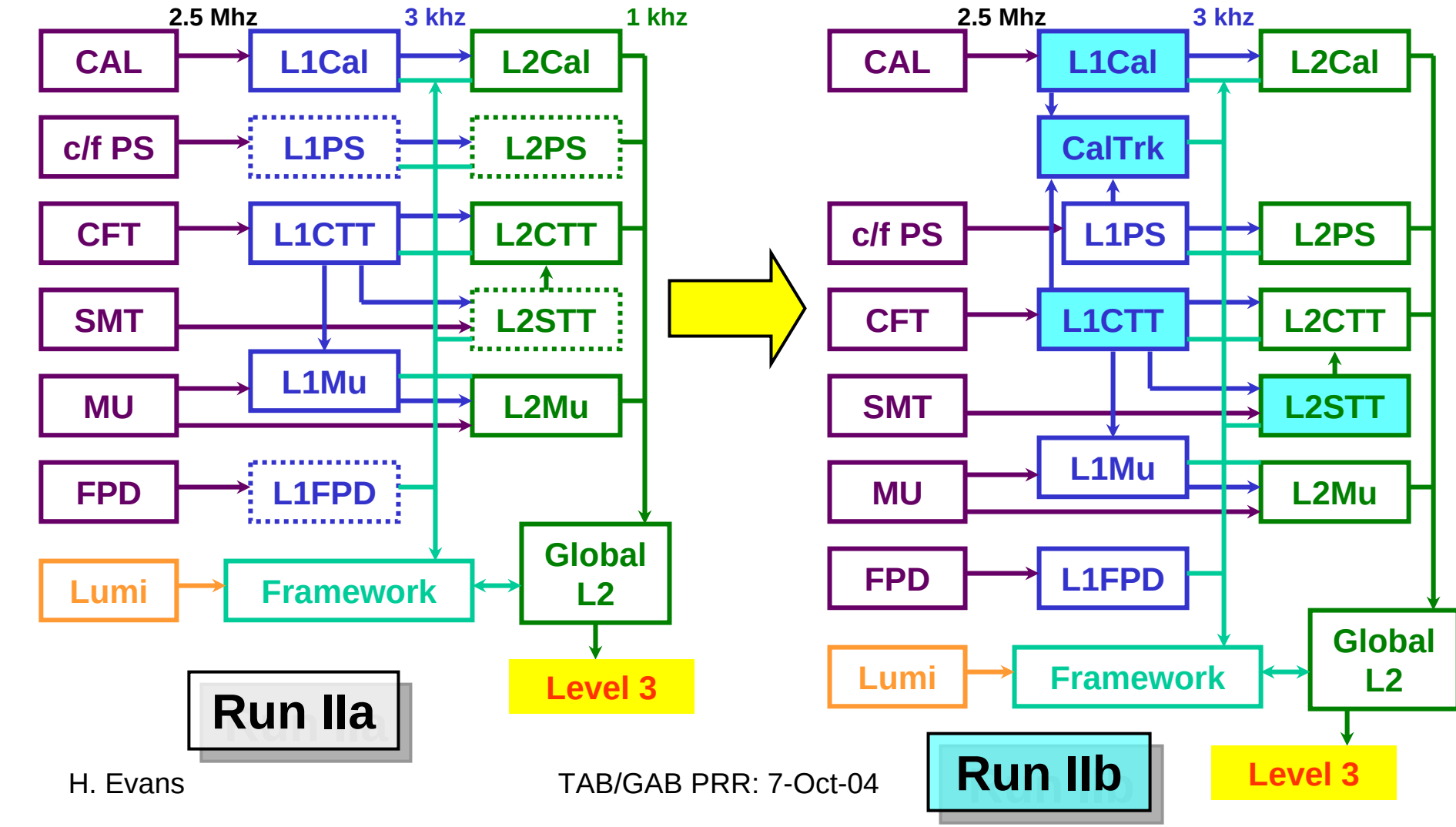
Trigger	Run IIa Definition	Example Channel	L1 Rate [kHz] (no upgrade)	L1 Rate [kHz] (w/ upgrade)
EM	1 EM TT > 10 GeV	$W \to e\nu$ $WH \to e\nu jj$	1.3	0.7
DiEM	1 EM TT > 7 GeV 2 EM TT > 5 GeV	$Z \to ee$ $ZH \to eejj$	0.5	0.1
Muon	1 Mu Pt > 11 GeV CFT Track	$W \to \mu\nu$ $WH \to \mu\nu jj$	6	1.1
Di-Mu	2 Mu Pt > 3 GeV CFT Tracks	$Z/\psi \to \mu\mu$ $ZH \to \mu\mu jj$	0.4	<0.1
e + Jets	1 EM TT > 7 GeV 2 Had TT > 5 GeV	$WH \to e\nu jj$ $tt \to e\nu$+jets	0.8	0.2
Mu + Jet	1 Mu Pt > 3 GeV 1 Had TT > 5 GeV	$WH \to \mu\nu jj$ $tt \to \mu\nu$+jets	<0.1	<0.1
Jet+MEt	2 TT > 5 GeV MEt > 10 GeV	$ZH \to \nu\nu bb$	2.1	0.8
Mu+EM	1 Mu Pt > 3 GeV + Trk 1 EM TT > 5 GeV	$H \to WW, ZZ$	<0.1	<0.1
Iso Trk	1 Iso Trk Pt > 10 GeV	$H \to \tau\tau$, $W \to \mu\nu$	17	1.0
Di-Trk	1 Iso Trk Pt > 10 GeV 2 Trk Pt > 5 GeV 1 Trk matched w/ EM	$H \to \tau\tau$	0.6	<0.1
Total Rate			~30	3.9

Luminosity
2×10^{32}

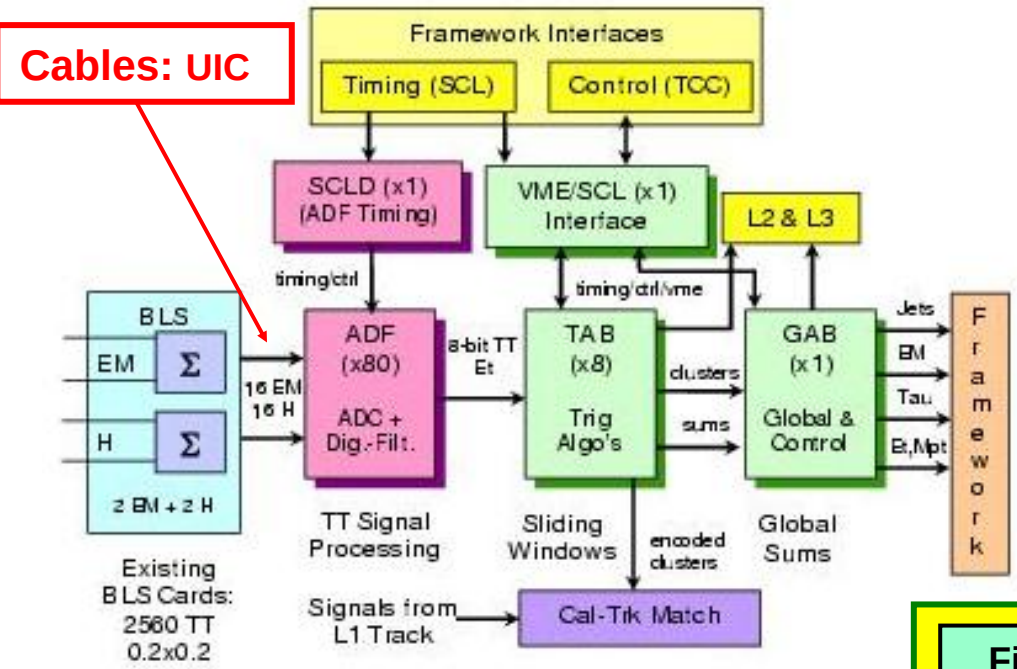
BC
396 ns

L1 Limit
~3 kHz

Meeting the Challenge



L1Cal Overview



Cables: UIC

Cal-Track Match: Arizona

Digitize → **Filter + E → Et**

ADF: Saclay, MSU

Find EM LMs → **Build EM**

Find EM+H LMs → **Build JETs**

Build TAUs

Et, Ex, Ey Sums

TAB: Nevis

Construct And/Or's

GAB: Nevis

Board Rundown

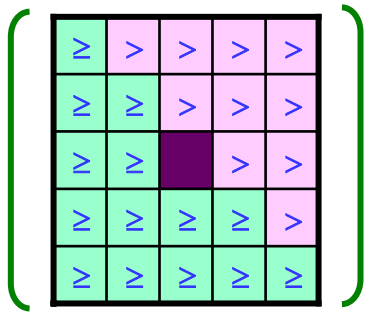
Custom Board	No	Purpose	$\eta \times \phi$: In / Out
ADF: ACD/Dig. Filt.	80	digitize, filter, E-to-Et	4×4 / 4×4
SCLD: ADF Timing F'out	4	ADF control/timing	all
TAB: Trig Algo Board	8	algo's, Cal-Trk out, sums	40×9 / 31×4
GAB: Global Algo Board	1	sums, trigs to FWK	all
VME/SCL Board	1	VME & timing to TAB/GAB	all
Splitter	4	Collect data in parallel w/ IIa System	4 TTs (8 chan's)
BLS-ADF Cables & Patch Panels, etc.		Match BLS cables to ADF inputs w/out rerunning	8×4 / 2×4×4

Algorithm Flow

TT Input
(corrected w/ ICR)

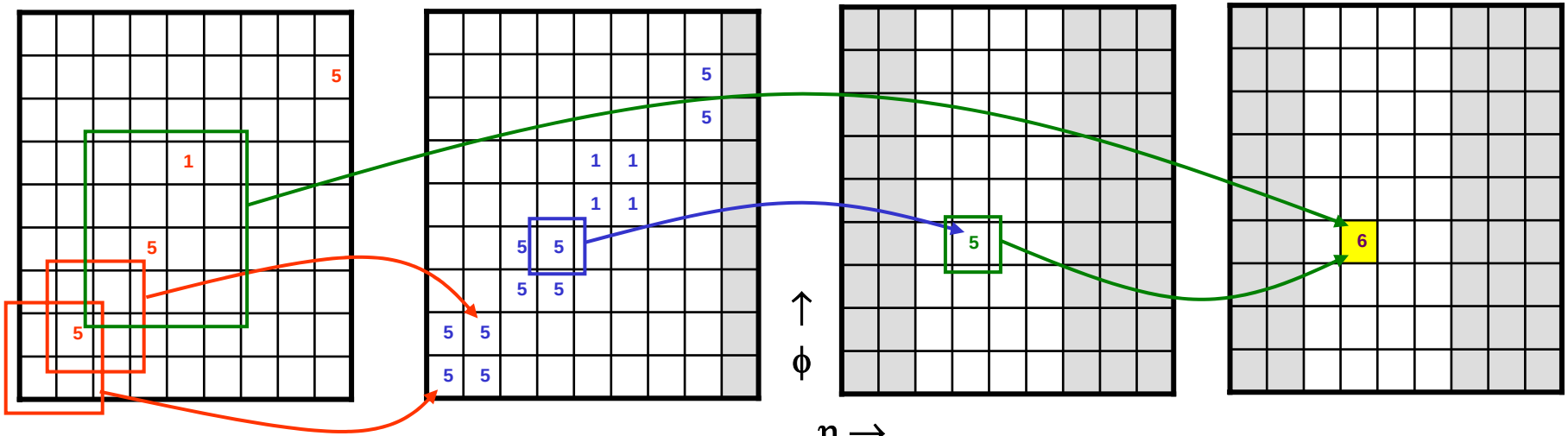
Make Regions of Interest

Find Local Maxima



Construct Objects

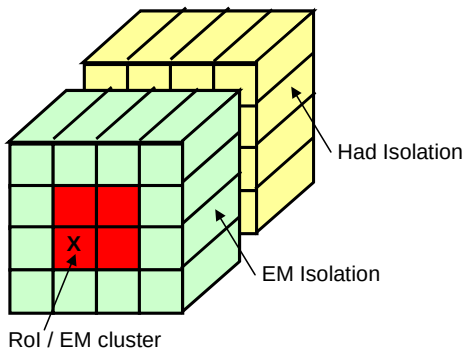
Compare to Thresholds



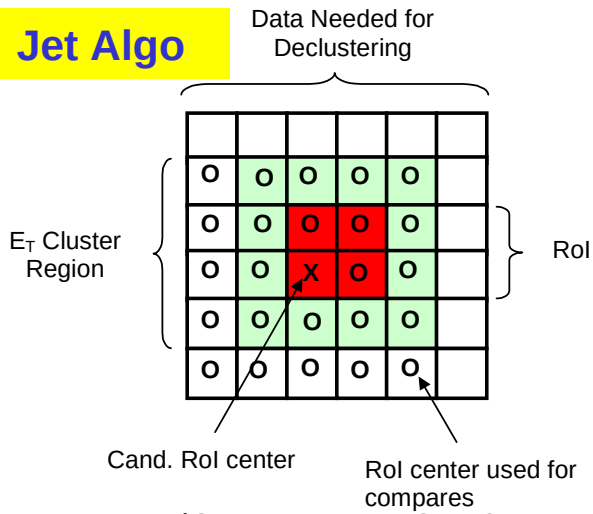
Objects

Object	Outputs	Cuts during Construction	Thresholds (*i* = 1-7)
EM	E_T EM(2x2)	• HD(4x4) < EM(2x2) / 2^3 • EM(ring) < cut (adc cnts)	E_T > EM Thr-i
Jet	E_T EM+HD(4x4)	• none	E_T > Jet Thr-i
Tau	E_T EM+HD(2x2) R = EM+HD(2x2) / (4x4)	• $[(2x2) \times (1/4x4)_{LUT}^{8\text{-bit}}]^{8\text{-bit}}$ = R	E_T & R vs Thr (t.b.d.)
Sums	Σ EM+HD(4x1) for ϕ = 2,3,4,5	• currently none • (TT > thr, |η| < cut,…)	none

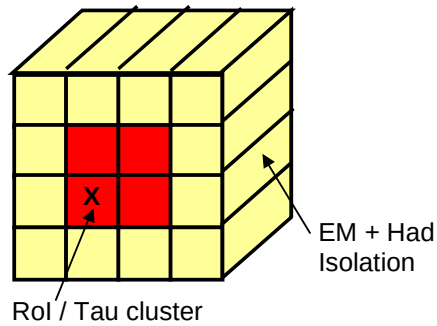
EM Algo



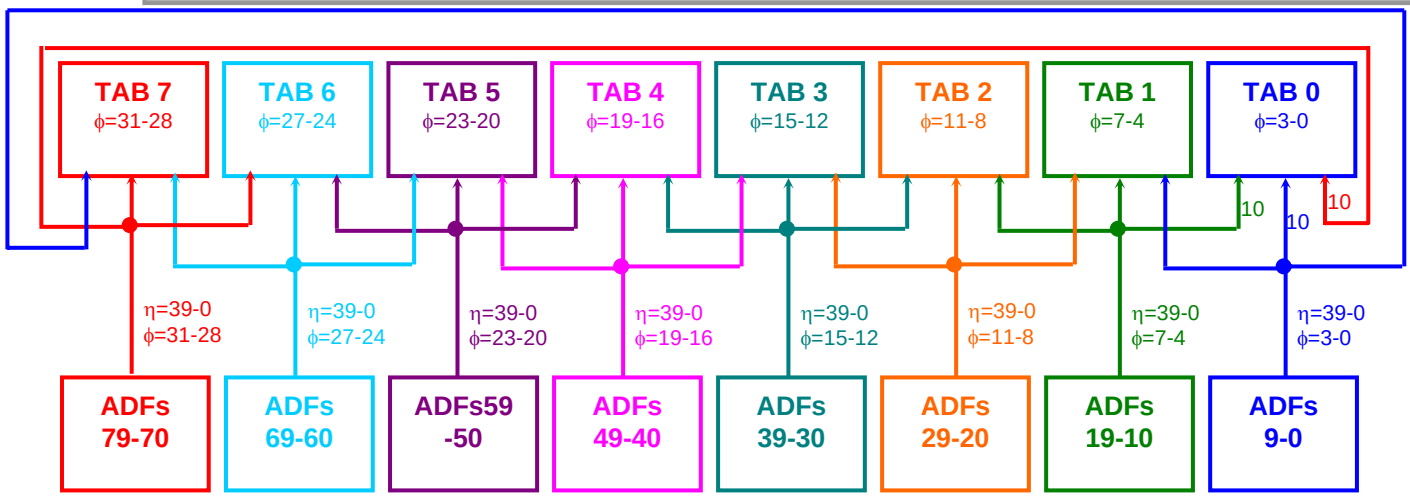
Jet Algo



Tau Algo



Algo's vs Architecture



1. **Use ICR in Jets + Data to Cal-Track**
   ⇒ **All eta to each TAB**

2. **Minimize Data Sharing**
   ⇒ **3 Identical outputs from each ADF (4x4x2 TTs)**

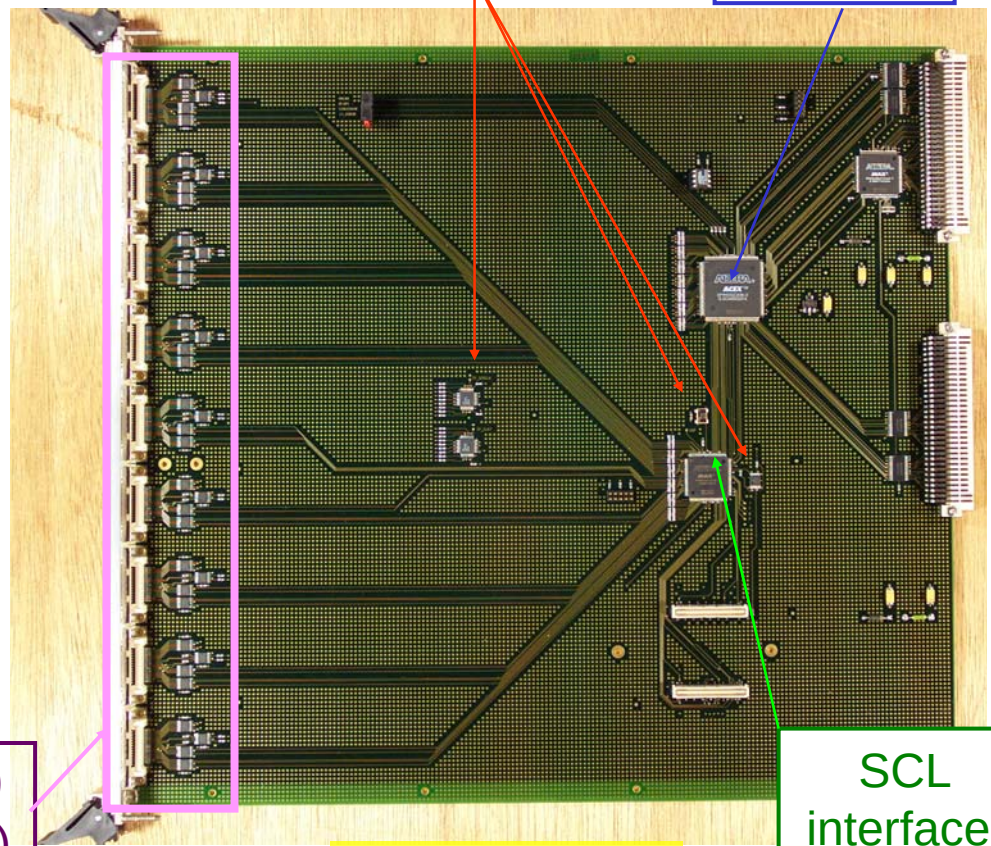
Each TAB:
40x9 inputs & 31x4 outputs

3. **Construct Local Maxima**
   ⇒ **SW Chip input 9x9**
   ⇒ **SW Chip output 4x4**

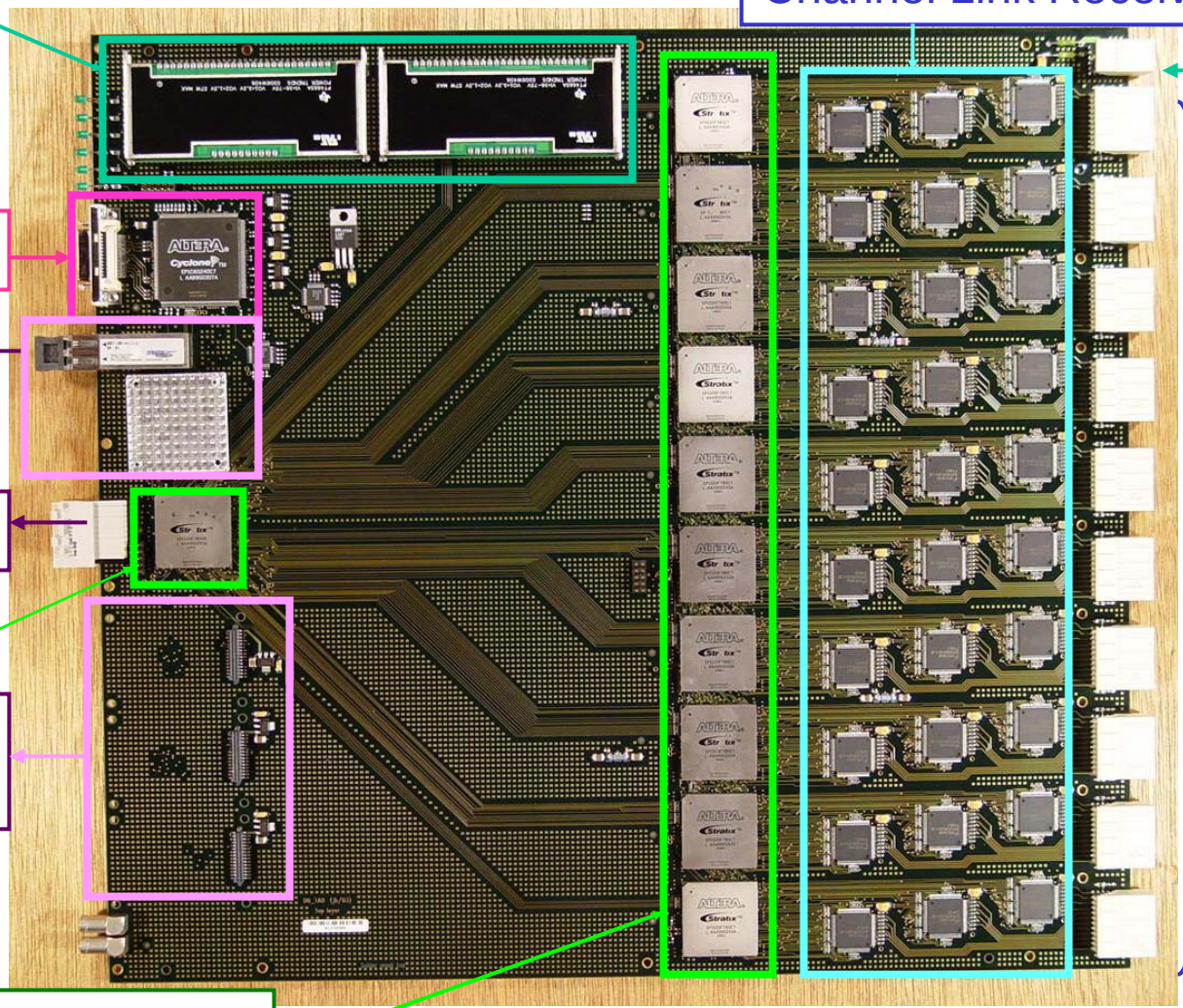
Algo	TTs for 1 LM	LMs / SW
2,0,1	4x4	6x6
2,1,1	6x6	4x4
2,2,1	8x8	2x2
3,-1,1	5x5	5x5
3,0,1	7x7	3x3

VME/SCL Board

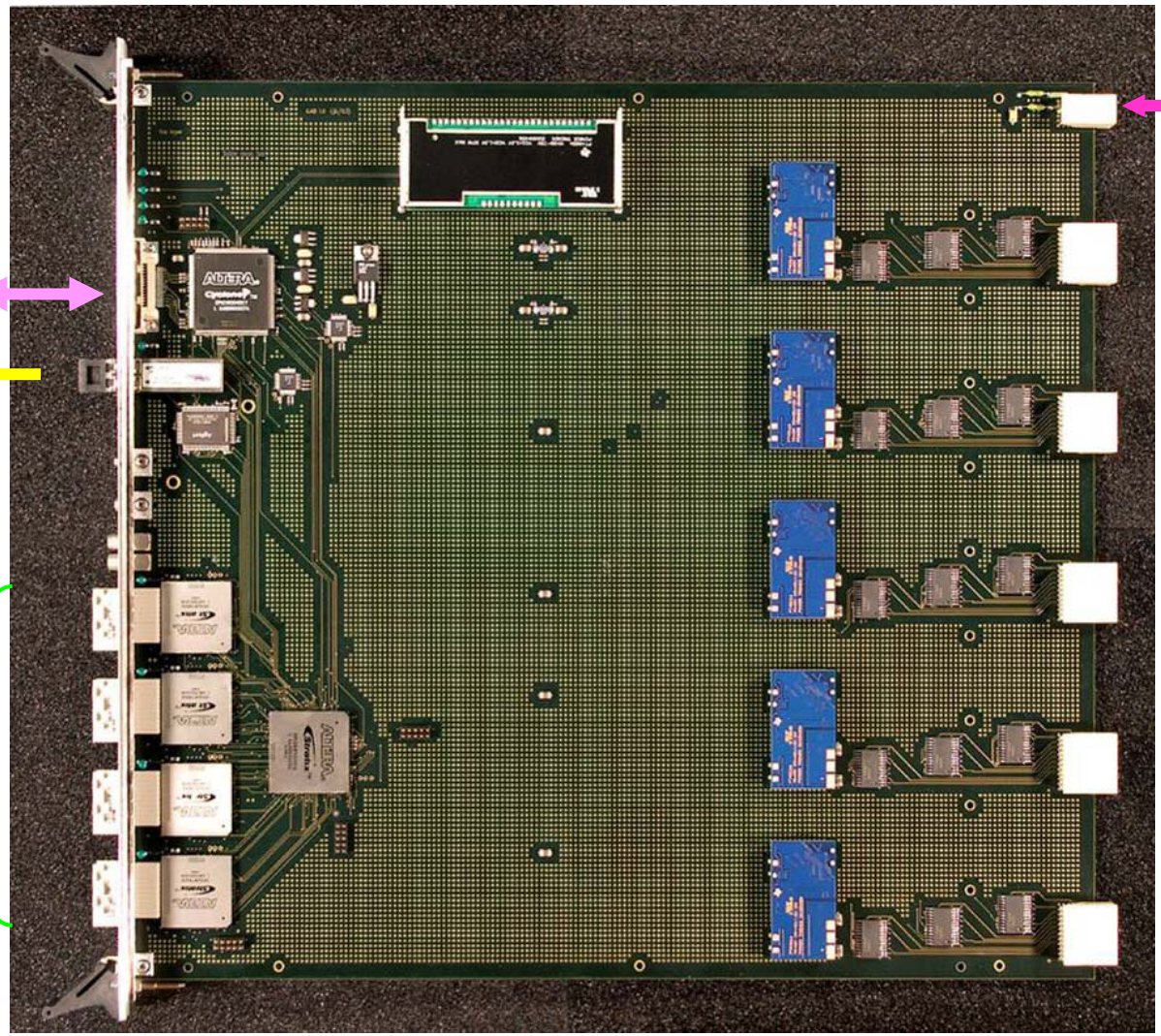
- New Comp. of TAB/GAB system
  - proposed: Feb 03
  - change control: Mar 03
- Interfaces to
  - VME (custom protocol)
    - not enough space on TAB for standard VME
  - D0 Trigger Timing (SCL)
  - (previously part of GAB)
- Why Split off from GAB
  - simplifies system design & maintenance
  - allows speedy testing of prototype TAB
- Fully Tested: Jun 03



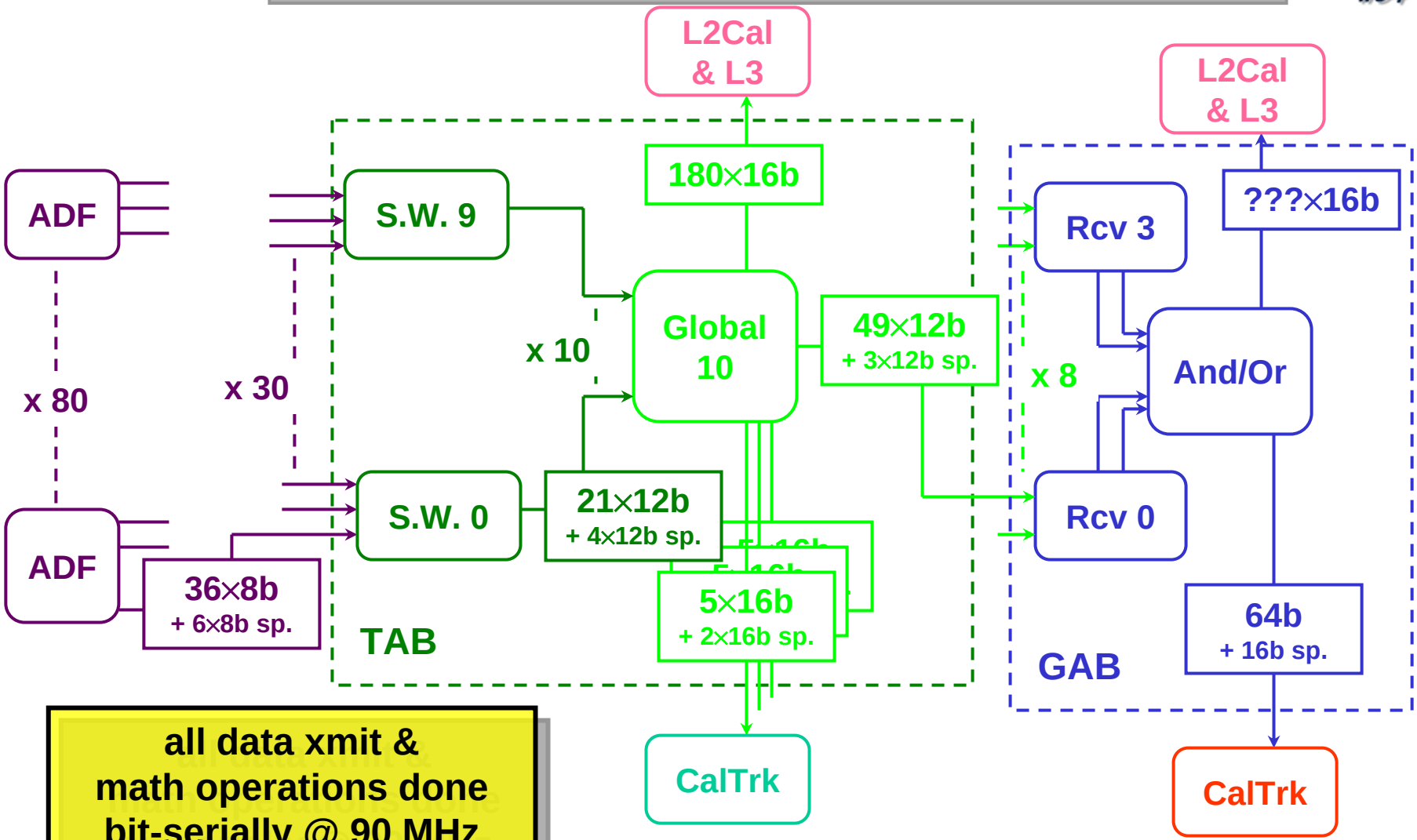
TAB


DC/DC conv
Channel Link Receivers (x30)
power
VME/SCL
L2/L3 Output (optical)
Output to GAB
Global Chip
Output to Cal-Track (x3)
ADF Inputs (x30) thru custom b'plane
Sliding Windows Chips (x10)

GAB



Data-Eye View of L1Cal



all data xmit & math operations done bit-serially @ 90 MHz

TAB to GAB Data Path

Intra-TAB: SW→Global

- Clusters 12 lines
  - 16-EM + 16-H+ 16-TAU
  - each clust = 3-bits (highest of 7 thr's pass)
- Sum(EM+H Et) 4 lines
  - sum over η for each ϕ
- Data for L2/L3 2 lines
  - on L1 Accept
- Stat/BX/Frame 3 lines
- Spare 4 lines

TAB to GAB: Global→Rcv

- EM Counts 12 words
- H Counts 12 words
- TAU Counts 12 words
  - 6 thr's – 2 bit counts
  - S,C,N regions
- Sum(EM+H) 3 words
  - Et, Ex, Ey
- Stat/Ctrl/… 7 words
- Spare 3 words

All Formats: www.nevis.columbia.edu/~evans/l1cal/hardware/tab/tab_gab_comm.html

Data Transmission

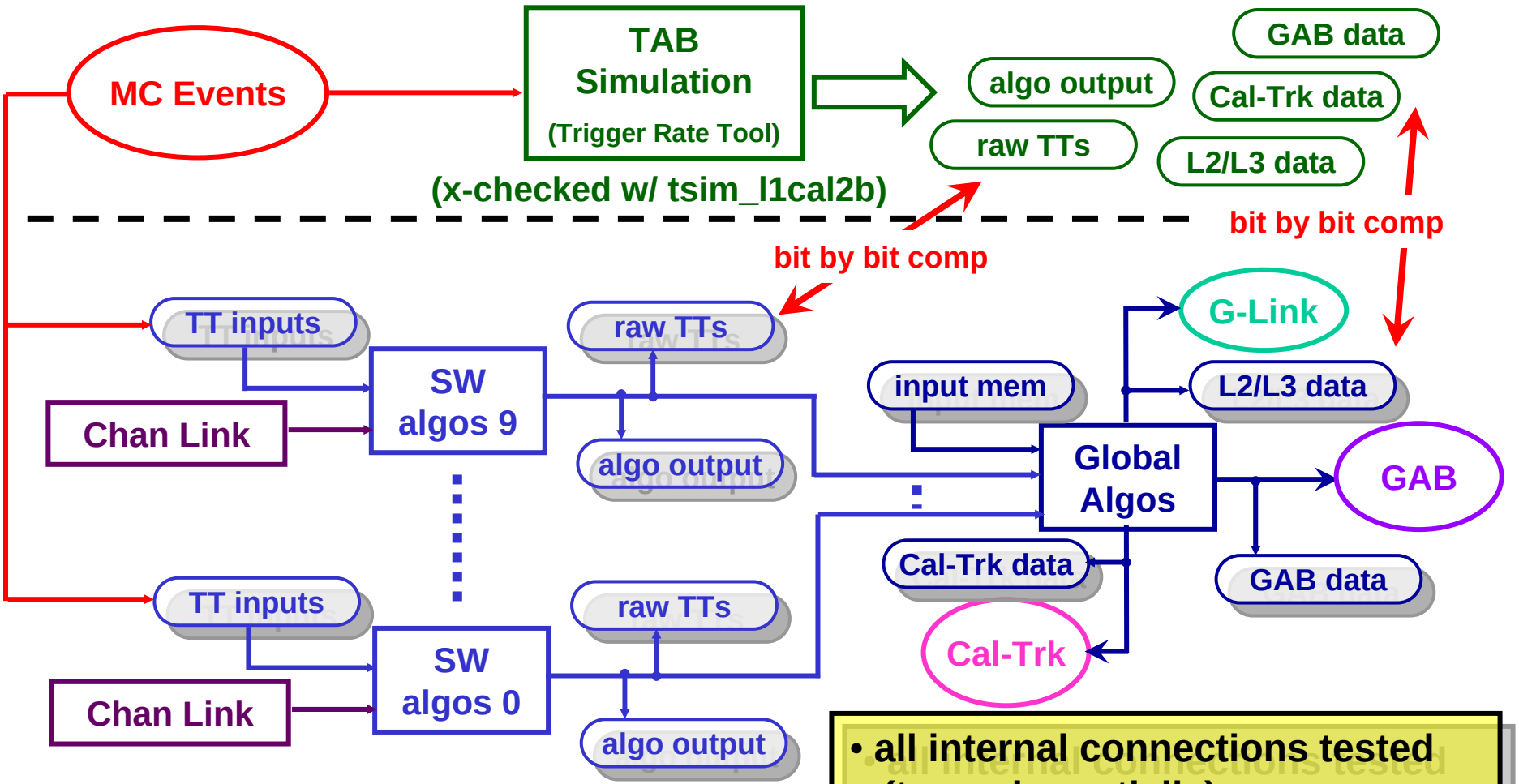
Link	Method	Clock
ADF to TAB	LVDS – Channel Link xmit/rcvr	424 MHz
TAB to GAB	LVDS – Stratix xmit/rcvr	636 MHz
TAB to Cal-Track	Gbit Cu Coax – Arizona SLDB xmit/rcvr	950 MHz
TAB/GAB to L2/L3	G-Link Optical xmit Optical split for L2/L3 branch	
GAB to TFW	ECL Ribbon Cable	7.6 MHz
SCL to TAB/GAB	Simple Serial Protocol via VME/SCL *clk7, init, turn, l1_accept, pulse, l1_error*	
VME to TAB/GAB	Simple Serial Protocol via VME/SCL *clk, frame, addr, data, frame-out, data-out*	

TAB/GAB Timeline

May 03	• VME/SCL prototype received
Jun 03	• TAB prototype received
Jul 03	• VME/SCL prototype testing complete (receives SCL signals at DØ)
Aug 03	• TAB prototype testing complete
Oct 03	• 1st prototype integration test SCL→ADF,TAB; ADF→TAB; TAB→Cal-Track
Feb 04	• GAB prototype received
Mar 04	• 2nd prototype integration test TAB → existing L1Cal VRB
Apr 04	• 2 TABs → GAB test
May 04	• TAB/GAB crate custom backplane received, installed, tested • GAB prototype testing complete (TAB to GAB & internal)

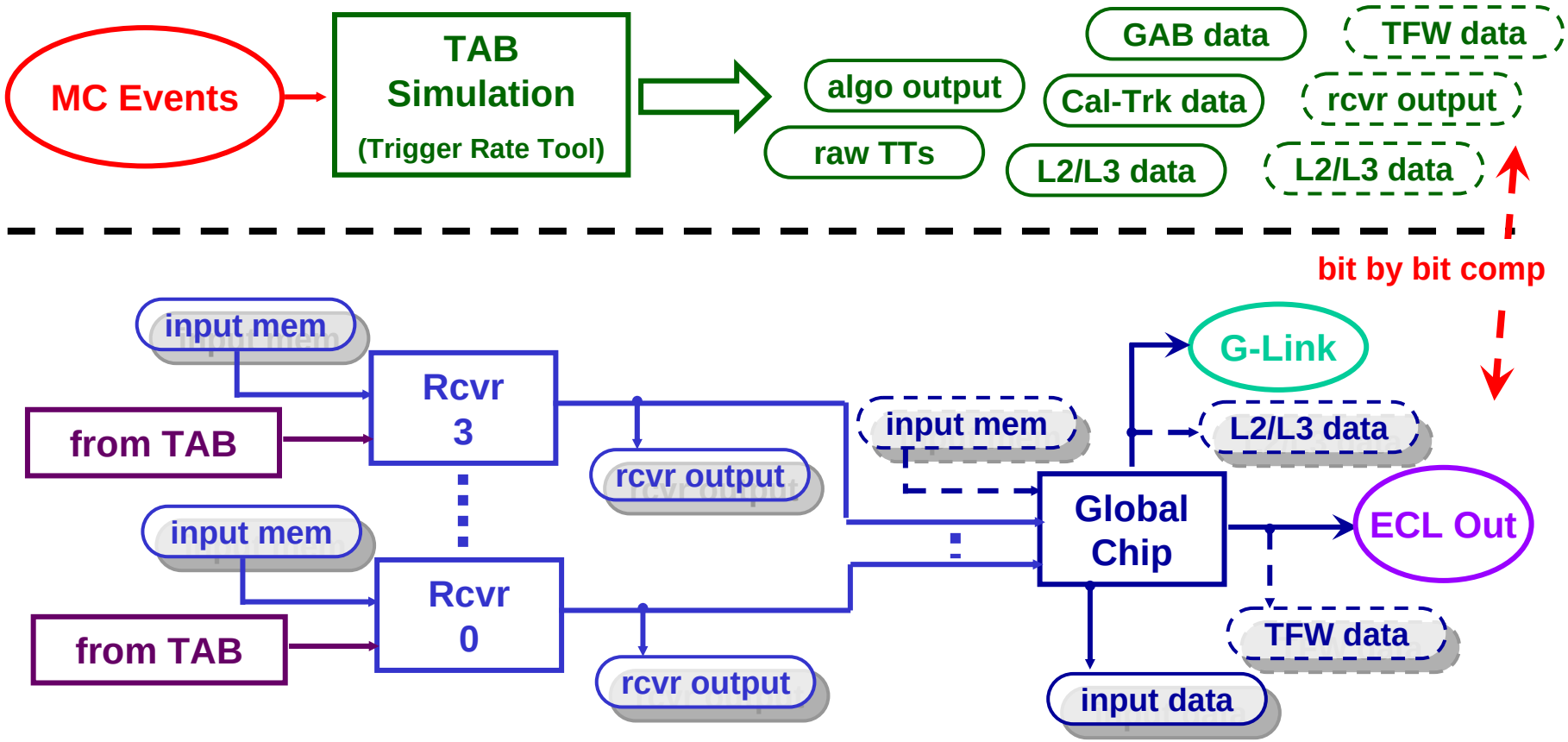
No Layout Problems found with any of the Boards

Internal TAB Testing



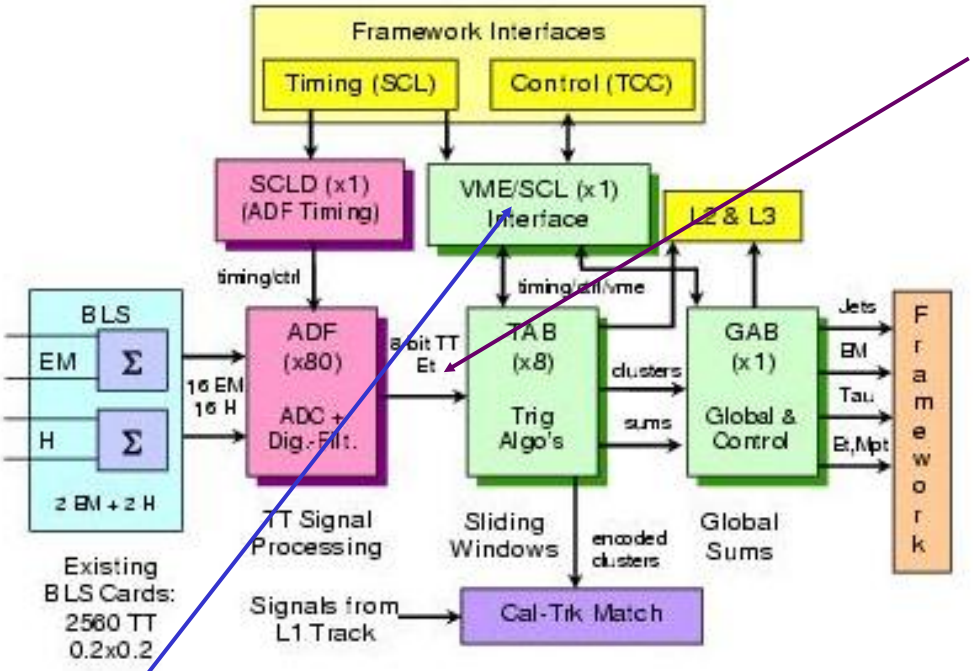
- all internal connections tested (tau only partially)
- using compare's to debug firmware & simulation

Internal GAB Testing



- $O(10^{??})$ events tested (rcvr → Global) ⇒ those lines tested
- Global → ECL Xmit signals tested with ECL Test Card

TAB/GAB I/O



☑ **SCL Timing & VME**

- extensively exercised at Nevis and DØ
- used in ADF→TAB tests

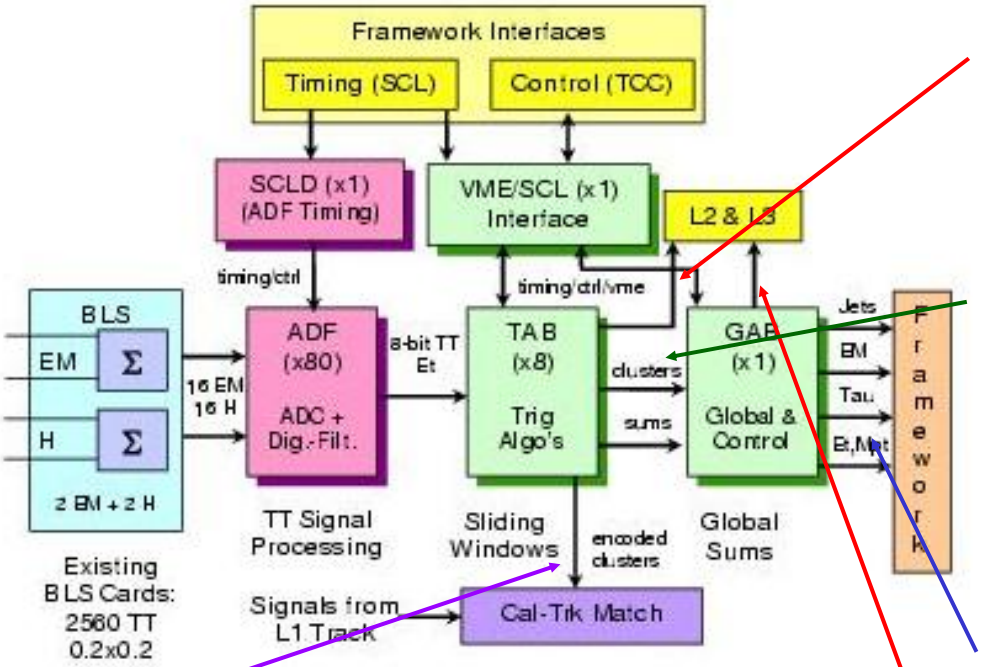
☑ **ADF → TAB**

- **Channel Link Parameters**
  - probed w/ Test Card
  - insensitive to: PLL range, deskew, DC balance, pre-emphasis

Clock (MHz)	BER Limit
50	<1.1e-14
60	<2.2e-15
75	<3.0e-15
90	<3.7e-15

- **At DØ w/ ADF**
  - error free (parity) xmit for >15 minutes
  - working on bit-by-bit check
- **Use of Channel Link provides clear spec !**

TAB/GAB I/O (cont)



☑ **TAB → L2/L3**
- several events sent to L1Cal VRB under DØ timing
- TAB events to tape soon

☑ **TAB → GAB**
- LVDS transmission checked w/ Test Card
  - safety margin of >400 ps
- $>10^9$ events TAB→GAB
- *O*(10^6) events 2 TABs→GAB

☐ **GAB → TFW**
- Signal paths checked using ECL Test Card

☐ **GAB → L2/L3**
- identical to TAB

☑ **TAB → Cal-Track**
- sync'ed TAB output w/ L1Muon board at DØ
- varied TAB output & saw corr. variation in L1Muon Trigger rate

☐ **Latency: SW inp → SLDB in = ~630 ns**

All Internal & External Hardware Paths Checked

H. Evans

Remaining Firmware

TAB

- Tau algorithm to be verified
- Change to Atlas EM algo ?
- Finalize L2 output
- Finalize monitoring
- Simulation of full TAB

GAB

- Only skeleton of Global chip firmware exists
  Need to add
  - Trigger Terms
  - Monitoring
  - L2 output

What's Next ?

- **If we're given the Green Light – produce:**
  - **10 TABs**
  - **3 GABs**

Task	Dur	Start	End
Delivery of rest of components	2w	10/11/04	10/22/04
Assemble boards (mainly Columbia administration)	6w	10/11/04	11/19/04
Test TABs/GABs at Nevis • goal: run fully populated TAB/GAB crate • some dependence of availability of engineers	12w	11/22/04	02/11/05

- **Testing at Fermilab**
  - **Have (nearly) enough hardware now for Nevis + DØ Tests**
    - **2 VME/SCLs; 2 TABs; 1 GAB; 2 TAB/GAB crates**
  - **Can send out some new boards as they pass tests**

Conclusions

We believe that we're ready to assemble

- **hardware has been checked**
  - **no changes from prototype**
- **all components ordered (most arrived) + PCBs here**
- **money is in hand (Hal's CAREER grant)**

Risks of Going Forward

- **TAB: essentially none**
- **GAB: some hardware paths not yet fully tested**

Risks of Delay

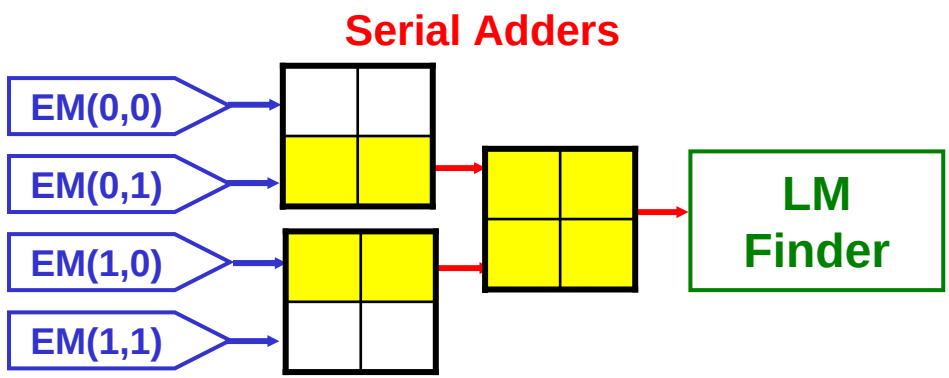
- **PCBs are aging (produced ~1 year ago)**
- **Atlas efforts intensifying**

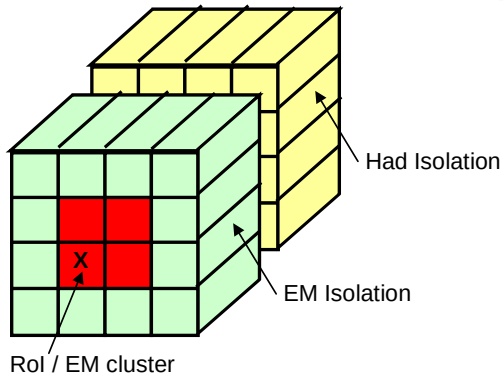
THANKS to the Committee for their Help !

Extra Slides

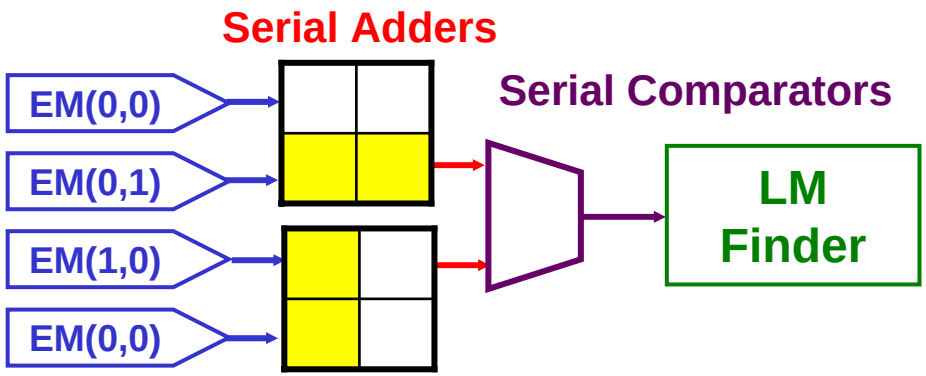
Simple "1x2 or 2x1" Algorithm

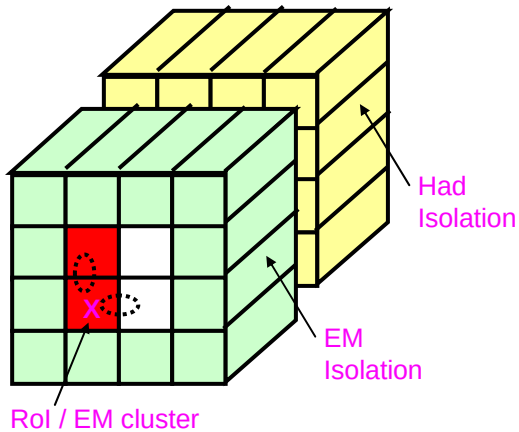
"2x2" EM Algo





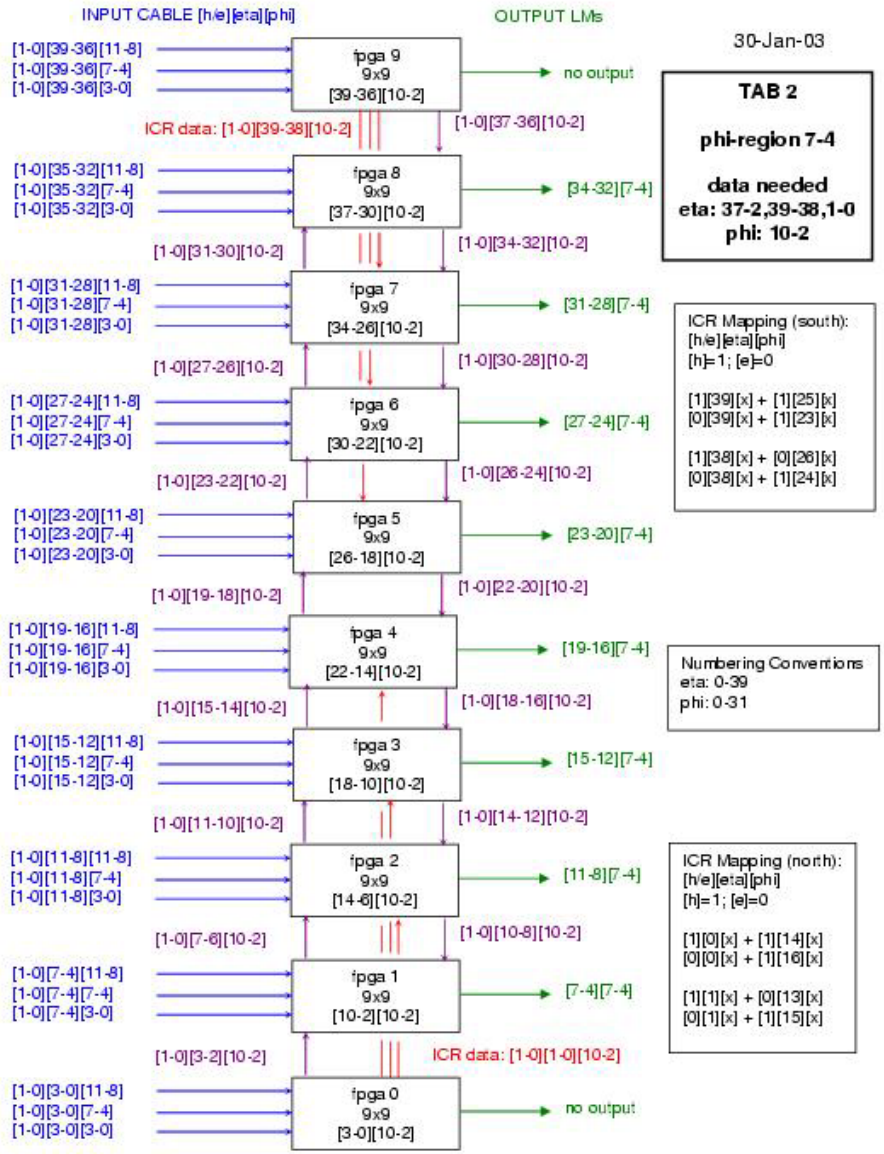
"1x2 or 2x1" EM Algo





- No extra latency
- Chosen cluster still indexed by LL corner of 2x2 region

Data in the TAB



SW to Global Chip Data

EM/Jet/Tau Results — 12 words

- for each algo & ϕ = 2,3,4,5 send out 12-bit word encoding highest threshold (7-1 or 0=none) passed by each of the four η's in that ϕ

ϕ	11 09	08 06	05 03	02 00
i	highest thr η=5	highest thr η=4	highest thr η=3	highest thr η=2

Global Sums — 4 words

- for each ϕ = 2,3,4,5 send out 12-bit word containing ΣEM+HD over four η's in that ϕ

ϕ	11 00
i	Σ E_T (EM+HD) over η = 2,3,4,5

Simulation Code for all this

1. tsim_l1cal2b — relies on DØ software environ.
2. standalone — being tested w/ hardware

TAB to GAB Data

- **EM/Jet/Tau Results** — **36 words**
  - for each algo & ϕ = 2,3,4,5 send out encoded 12-bit words for η = S,C,N containing 2-bit counts of no. of objects passing each of 6 thresholds

ϕ	η	11 10	09 08	07 06	05 04	03 02	01 00
i	*j*	cnt thr-6	cnt thr-5	cnt thr-4	cnt thr-3	cnt thr-2	cnt thr-1
i = 2,3,4,5 ; *j* = S,C,N							

- **Global Sums** — **3 words**

ϕ	η	11 00
2-5	0-39	ΣE_T (EM+HD)
2-5	0-39	ΣE_x (EM+HD)
2-5	0-39	ΣE_y (EM+HD)

Data to Cal-Track Match

Output from TAB Global Chip (10)		
No.	**Bits 15 – 08**	**Bits 07 – 00**
1	JET Mask: ϕ = i+3	EM Mask: ϕ = i+3
2	JET Mask: ϕ = i+2	EM Mask: ϕ = i+2
3	JET Mask: ϕ = i+1	EM Mask: ϕ = i+1
4	JET Mask: ϕ = i	EM Mask: ϕ = i
5	0	0
6	0	0
7	Longitudinal Parity	

Mask Definition:

- Bit 07 unused
- Bits 06 – 00 set if threshold *j* is passed

www.nevis.columbia.edu/~evans/l1cal/hardware/tab/tab_to_caltrack.html

Short Term Plans

Task	Comments	Timescale
Simulation	Shift studies into high gear	now
TAB → L2/L3	Write data to tape (test unpacking)	Oct
ADFv1 → TAB	Long Term Data Transfer Tests	Oct
TAB/GAB	Fully Automated Event Verification	Nov
GAB	Implement 1st And/Or terms	End 04
ADFv2 → TAB	First Integration	End 04

Road to Installation (Jul 05)

1. **Operations & Stability** — **run test system**
   - a. crashes/deadtime — meas. in test syst.
   - b. reliable downloading — use in test syst.
   - c. monitoring tools — software in place
   - d. param determination — software in place
   - e. unpacker/reco stable — data from test syst

2. **Trigger Quality** — **data & MC**
   - a. rates & efficiencies — pred w/ MC – verify w/ data
   - b. trigger definitions (L1,L2,L3) — in place well beforehand
     - filter coeff's, thresholds, and/or terms, trigger list

Note: all of these must be Documented

Testing Trigger Quality

Splitters ⇒ Data Available before Installation

- **at most 16-EM + 16-H ⇒ cannot test Sliding Windows**

Possible Chain to Rate/Eff Estimates

1. **Define Triggers**
   - **trig-list, and/or, thresh, filt. coeff's**
2. **Using Splitter Data derive TT response**
   - **compare ADF Et(TT) output w/ Precision Readout ⇒ correct MC modeling of Et(TT)**
   - **probe pathological cases using TWG**
3. **MC models TAB Algorithms**
   - **sliding windows algorithm is deterministic**
   - **use standalone MC to look for algorithm pathologies**
4. **MC models And/Or terms & Trigger List ⇒ Rates & Eff's**
   - **need to test QCD MC vs. Data w/ Run IIa Trigger**