In a Nutshell
- We have the components, the boards, the money…
- Should we assemble the TABs and GABs?

Concentrate on
- Hardware Design & Testing ⇒ Production Readiness

Less Emphasis
- Project Justification, Algorithm Devel, Install/Commission
The Nevis Team

Students
Chad Johnson, Jovan Mitrevski

Postdocs
Sabine Lammers, TBA

Engineers
Jaro Ban, Bill Sippach + Nevis Tech’s

Faculty
Hal Evans, John Parsons
The Tevatron Landscape

Accelerator Plan: FY 05-09

- Peak
- Phases
- Total

install upgrades

current peak L

2.8e32!

Date

9/29/03 9/29/04 9/30/05 10/1/06 10/2/07 10/2/08 10/3/09

Peak Luminosity (x10^30 cm^-2 sec^-1)

Total Integrated Luminosity (fb)
## Trigger Challenges

<table>
<thead>
<tr>
<th>Trigger</th>
<th>Run Ila Definition</th>
<th>Example Channel</th>
<th>L1 Rate [kHz] (no upgrade)</th>
<th>L1 Rate [kHz] (w/ upgrade)</th>
</tr>
</thead>
<tbody>
<tr>
<td>EM</td>
<td>1 EM TT &gt; 10 GeV</td>
<td>W→ee</td>
<td>1.3</td>
<td>0.7</td>
</tr>
<tr>
<td></td>
<td></td>
<td>WH→evjj</td>
<td></td>
<td></td>
</tr>
<tr>
<td>DiEM</td>
<td>1 EM TT &gt; 7 GeV</td>
<td>Z→ee</td>
<td>0.5</td>
<td>0.1</td>
</tr>
<tr>
<td></td>
<td>2 EM TT &gt; 5 GeV</td>
<td>ZH→eejj</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Muon</td>
<td>1 Mu Pt &gt; 11 GeV</td>
<td>W→μν</td>
<td>6</td>
<td>1.1</td>
</tr>
<tr>
<td></td>
<td>CFT Track</td>
<td>WH→μνjj</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Di-Mu</td>
<td>2 Mu Pt &gt; 3 GeV</td>
<td>Z/ψ→μμ</td>
<td>0.4</td>
<td>&lt;0.1</td>
</tr>
<tr>
<td></td>
<td>CFT Tracks</td>
<td>ZH→μμjj</td>
<td></td>
<td></td>
</tr>
<tr>
<td>e + Jets</td>
<td>1 EM TT &gt; 7 GeV</td>
<td>WH→evjj</td>
<td>0.8</td>
<td>0.2</td>
</tr>
<tr>
<td></td>
<td>2 Had TT &gt; 5 GeV</td>
<td>tt→ev+jets</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Mu + Jet</td>
<td>1 Mu Pt &gt; 3 GeV</td>
<td>WH→μνjj</td>
<td>&lt;0.1</td>
<td>&lt;0.1</td>
</tr>
<tr>
<td></td>
<td>1 Had TT &gt; 5 GeV</td>
<td>tt→μν+jets</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Jet+MEt</td>
<td>2 TT &gt; 5 GeV</td>
<td>ZH→vvbb</td>
<td>2.1</td>
<td>0.8</td>
</tr>
<tr>
<td></td>
<td>MEt &gt; 10 GeV</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Mu+EM</td>
<td>1 Mu Pt &gt; 3 GeV + Trk</td>
<td>H→WW,ZZ</td>
<td>&lt;0.1</td>
<td>&lt;0.1</td>
</tr>
<tr>
<td></td>
<td>1 EM TT &gt; 5 GeV</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Iso Trk</td>
<td>1 Iso Trk Pt &gt; 10 GeV</td>
<td>H→ττ , W→μν</td>
<td>17</td>
<td>1.0</td>
</tr>
<tr>
<td>Di-Trk</td>
<td>1 Iso Trk Pt &gt; 10 GeV</td>
<td>H→ττ</td>
<td>0.6</td>
<td>&lt;0.1</td>
</tr>
<tr>
<td></td>
<td>2 Trk Pt &gt; 5 GeV</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1 Trk matched w/ EM</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Total Rate</td>
<td></td>
<td></td>
<td>~30</td>
<td>3.9</td>
</tr>
</tbody>
</table>

**Luminosity**

\[2 \times 10^{32}\]

BC 396 ns

**L1 Limit**

\(~3 \text{ kHz}\)
Meeting the Challenge

Detector | Level 1 | Level 2
---|---|---
CAL | L1Cal | L2Cal
C/f PS | L1PS | L2PS
CFT | L1CTT | L2CTT
SMT | L1Mu | L2Mu
MU | L1FPD | Global L2
FPD | Luzi |
Framework

Level 3

Run IIa

Global L2

Level 3

Run IIb

Global L2

Detector | Level 1 | Level 2
---|---|---
CAL | L1Cal | L2Cal
C/f PS | L1PS | L2PS
CFT | L1CTT | L2CTT
SMT | L1Mu | L2Mu
MU | L1FPD | Global L2
FPD | Luzi |
Framework

Level 3

Run IIa

Global L2

Level 3

Run IIb

Global L2

2.5 Mhz | 3 khz | 1 khz

H. Evans

TAB/GAB PRR: 7-Oct-04
L1Cal Overview

Cables: UIC

Digitize

Filter + E → Et

ADF: Saclay, MSU

Find EM LMs

Build EM

Find EM+H LMs

Build JETs

Et, Ex, Ey Sums

Build TAU's

TAB: Nevis

TAB/GAB: Nevis

Construct And/Or's

Cal-Track Match: Arizona

H. Evans
<table>
<thead>
<tr>
<th>Custom Board</th>
<th>No</th>
<th>Purpose</th>
<th>$\eta \times \phi$: In / Out</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADF: ACD/Dig. Filt.</td>
<td>80</td>
<td>digitize, filter, E-to-Et</td>
<td>$4\times4 / 4\times4$</td>
</tr>
<tr>
<td>SCLD: ADF Timing F’out</td>
<td>4</td>
<td>ADF control/timing</td>
<td>all</td>
</tr>
<tr>
<td>TAB: Trig Algo Board</td>
<td>8</td>
<td>algo’s, Cal-Trk out, sums</td>
<td>$40\times9 / 31\times4$</td>
</tr>
<tr>
<td>GAB: Global Algo Board</td>
<td>1</td>
<td>sums, trigs to FWK</td>
<td>all</td>
</tr>
<tr>
<td>VME/SCL Board</td>
<td>1</td>
<td>VME &amp; timing to TAB/GAB</td>
<td>all</td>
</tr>
<tr>
<td>Splitter</td>
<td>4</td>
<td>Collect data in parallel w/ Ila System</td>
<td>$4$ TTs (8 chan’s)</td>
</tr>
<tr>
<td>BLS-ADF Cables &amp; Patch Panels, etc.</td>
<td></td>
<td>Match BLS cables to ADF inputs w/out rerunning</td>
<td>$8\times4 / 2\times4\times4$</td>
</tr>
</tbody>
</table>
Algorithm Flow

- TT Input (corrected w/ ICR)
- Make Regions of Interest
- Find Local Maxima
- Construct Objects
- Compare to Thresholds

<table>
<thead>
<tr>
<th>TT Space</th>
<th>ROI Space</th>
<th>LM Space</th>
<th>Jet Space</th>
</tr>
</thead>
<tbody>
<tr>
<td>H. Evans</td>
<td>TAB/GAB PRR: 7-Oct-04</td>
<td>η →</td>
<td>θ →</td>
</tr>
</tbody>
</table>

Symbols:
- ≥
- >

Notes:
- Find Local Maxima
- Construct Objects
- Compare to Thresholds
# Objects

<table>
<thead>
<tr>
<th>Object</th>
<th>Outputs</th>
<th>Cuts during Construction</th>
<th>Thresholds ($i = 1\text{&quot;}-7$)</th>
</tr>
</thead>
</table>
| EM     | $E_T \text{ EM}(2x2)$ | • HD(4x4) < EM(2x2) / 2^3  
• EM(ring) < cut (adc cnts) | $E_T > \text{ EM Thr-}i$ |
| Jet    | $E_T \text{ EM+HD}(4x4)$ | • none | $E_T > \text{ Jet Thr-}i$ |
| Tau    | $E_T \text{ EM+HD}(2x2)$  
$R = \text{ EM+HD}(2x2) / (4x4)$ | • $[(2x2) \times (1/4x4)_{\text{LUT}}^{8\text{-bit}}]_{\text{8-bit}} = R$ | $E_T \text{ & } R \text{ vs Thr}$  
(t.b.d.) |
| Sums   | $\sum \text{ EM+HD}(4x1)$ for $\phi = 2,3,4,5$ | • currently none  
• (TT > thr, $|\eta| < \text{cut,}...$) | none |

**EM Algo**

**Jet Algo**

**Data Needed for Declustering**

**Tau Algo**

![](image1.png)
Algo’s vs Architecture

1. Use ICR in Jets + Data to Cal-Track ⇒ All eta to each TAB

2. Minimize Data Sharing ⇒ 3 Identical outputs from each ADF (4x4x2 TTs)

Each TAB: 40x9 inputs & 31x4 outputs

3. Construct Local Maxima ⇒ SW Chip input 9x9 ⇒ SW Chip output 4x4

<table>
<thead>
<tr>
<th>Algo</th>
<th>TTs for 1 LM</th>
<th>LMs / SW</th>
</tr>
</thead>
<tbody>
<tr>
<td>2,0,1</td>
<td>4x4</td>
<td>6x6</td>
</tr>
<tr>
<td>2,1,1</td>
<td>6x6</td>
<td>4x4</td>
</tr>
<tr>
<td>2,2,1</td>
<td>8x8</td>
<td>2x2</td>
</tr>
<tr>
<td>3,-1,1</td>
<td>5x5</td>
<td>5x5</td>
</tr>
<tr>
<td>3,0,1</td>
<td>7x7</td>
<td>3x3</td>
</tr>
</tbody>
</table>
VME/SCL Board

- **New Comp. of TAB/GAB system**
  - proposed: Feb 03
  - change control: Mar 03

- **Interfaces to**
  - VME (custom protocol)
    - not enough space on TAB for standard VME
  - D0 Trigger Timing (SCL)
  - (previously part of GAB)

- **Why Split off from GAB**
  - simplifies system design & maintenance
  - allows speedy testing of prototype TAB

- **Fully Tested:** Jun 03

- local osc’s & f’out (standalone runs)

- serial out x9 (VME & SCL)

- VME interface

- SCL interface

DONE
DC/DC conv

VME/SCL

L2/L3 Output (optical)

Output to GAB

Global Chip

Output to Cal-Track (x3)

Sliding Windows Chips (x10)

Channel Link Receivers (x30)

power

ADF Inputs (x30) thru custom b'plane

H. Evans

TAB/GAB PRR: 7-Oct-04
GAB

- Power
- Out to TFW
- VME/SCL
- L2/L3
- TAB Inputs (x8)
Data-Eye View of L1Cal

ADF

36×8b + 6×8b sp.

x 80

S.W. 0

21×12b + 4×12b sp.

S.W. 9

180×16b

Global 10

49×12b + 3×12b sp.

x 10

5×16b + 2×16b sp.

CalTrk

Rcv 0

And/Or

Rcv 3

L2Cal & L3

L2Cal & L3

64b + 16b sp.

TAB

GAB

all data xmit & math operations done bit-serially @ 90 MHz

H. Evans

TAB/GAB PRR: 7-Oct-04
**TAB to GAB Data Path**

**Intra-TAB: SW → Global**
- Clusters: 12 lines
  - 16-EM + 16-H + 16-TAU
  - Each cluster = 3-bits (highest of 7 thr’s pass)
- Sum(EM+H Et): 4 lines
  - Sum over η for each φ
- Data for L2/L3: 2 lines
  - On L1 Accept
- Stat/BX/Frame: 3 lines
- Spare: 4 lines

**TAB to GAB: Global → Rcv**
- EM Counts: 12 words
- H Counts: 12 words
- TAU Counts: 12 words
  - 6 thr’s – 2 bit counts
  - S, C, N regions
- Sum(EM+H): 3 words
  - Et, Ex, Ey
- Stat/Ctrl/…: 7 words
- Spare: 3 words

All Formats: www.nevis.columbia.edu/~evans/l1cal/hardware/tab/tab_gab_comm.html
## Data Transmission

<table>
<thead>
<tr>
<th>Link</th>
<th>Method</th>
<th>Clock</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADF to TAB</td>
<td>LVDS – Channel Link xmit/rcvr</td>
<td>424 MHz</td>
</tr>
<tr>
<td>TAB to GAB</td>
<td>LVDS – Stratix xmit/rcvr</td>
<td>636 MHz</td>
</tr>
<tr>
<td>TAB to Cal-Track</td>
<td>Gbit Cu Coax – Arizona SLDB xmit/rcvr</td>
<td>950 MHz</td>
</tr>
<tr>
<td>TAB/GAB to L2/L3</td>
<td>G-Link Optical xmit</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Optical split for L2/L3 branch</td>
<td></td>
</tr>
<tr>
<td>GAB to TFW</td>
<td>ECL Ribbon Cable</td>
<td>7.6 MHz</td>
</tr>
<tr>
<td>SCL to TAB/GAB</td>
<td>Simple Serial Protocol via VME/SCL</td>
<td></td>
</tr>
<tr>
<td></td>
<td>clk7, init, turn, l1_accept, pulse, l1_error</td>
<td></td>
</tr>
<tr>
<td>VME to TAB/GAB</td>
<td>Simple Serial Protocol via VME/SCL</td>
<td></td>
</tr>
<tr>
<td></td>
<td>clk, frame, addr, data, frame-out, data-out</td>
<td></td>
</tr>
</tbody>
</table>
# TAB/GAB Timeline

<table>
<thead>
<tr>
<th>Month</th>
<th>Event</th>
</tr>
</thead>
<tbody>
<tr>
<td>May 03</td>
<td>VME/SCL prototype received</td>
</tr>
<tr>
<td>Jun 03</td>
<td>TAB prototype received</td>
</tr>
<tr>
<td>Jul 03</td>
<td>VME/SCL prototype testing complete (receives SCL signals at DØ)</td>
</tr>
<tr>
<td>Aug 03</td>
<td>TAB prototype testing complete</td>
</tr>
<tr>
<td>Oct 03</td>
<td>1\textsuperscript{st} prototype integration test</td>
</tr>
<tr>
<td></td>
<td>SCL $\rightarrow$ ADF, TAB; ADF $\rightarrow$ TAB; TAB $\rightarrow$ Cal-Track</td>
</tr>
<tr>
<td>Feb 04</td>
<td>GAB prototype received</td>
</tr>
<tr>
<td>Mar 04</td>
<td>2\textsuperscript{nd} prototype integration test</td>
</tr>
<tr>
<td></td>
<td>TAB $\rightarrow$ existing L1Cal VRB</td>
</tr>
<tr>
<td>Apr 04</td>
<td>2 TABs $\rightarrow$ GAB test</td>
</tr>
<tr>
<td>May 04</td>
<td>TAB/GAB crate custom backplane received, installed, tested</td>
</tr>
<tr>
<td></td>
<td>GAB prototype testing complete (TAB to GAB &amp; internal)</td>
</tr>
</tbody>
</table>

No Layout Problems found with any of the Boards
Internal TAB Testing

- all internal connections tested (tau only partially)
- using compare’s to debug firmware & simulation
Internal GAB Testing

- **MC Events** → TAB Simulation (Trigger Rate Tool) → algo output, Cal-Trk data, raw TTs, L2/L3 data → Global Chip → ECL Out
  - **Rcvr 3** → input mem from TAB
  - **Rcvr 0** → input mem from TAB

- **O(10??) events tested (rcvr → Global) ⇒ those lines tested**
- **Global → ECL Xmit signals tested with ECL Test Card**

- **Global** → ECL Xmit signals tested with ECL Test Card
**SCL Timing & VME**
- extensively exercised at Nevis and DØ
- used in ADF → TAB tests

**ADF → TAB**
- Channel Link Parameters
  - probed w/ Test Card
  - insensitive to: PLL range, deskew, DC balance, pre-emphasis

**Use of Channel Link provides clear spec!**

<table>
<thead>
<tr>
<th>Clock (MHz)</th>
<th>BER Limit</th>
</tr>
</thead>
<tbody>
<tr>
<td>50</td>
<td>&lt;1.1e-14</td>
</tr>
<tr>
<td>60</td>
<td>&lt;2.2e-15</td>
</tr>
<tr>
<td>75</td>
<td>&lt;3.0e-15</td>
</tr>
<tr>
<td>90</td>
<td>&lt;3.7e-15</td>
</tr>
</tbody>
</table>

**At DØ w/ ADF**
- error free (parity) xmit for >15 minutes
- working on bit-by-bit check
TAB/GAB I/O (cont)

☑️ TAB → L2/L3
  - several events sent to L1Cal VRB under DØ timing
  - TAB events to tape soon

☑️ TAB → GAB
  - LVDS transmission checked w/ Test Card
    - safety margin of >400 ps
  - $>10^9$ events TAB→GAB
  - $O(10^6)$ events 2 TABs→GAB

☐ GAB → TFW
  - Signal paths checked using ECL Test Card

☐ GAB → L2/L3
  - identical to TAB

☑️ TAB → Cal-Track
  - sync’ed TAB output w/ L1Muon board at DØ
  - varied TAB output & saw corr. variation in L1Muon Trigger rate

☐ Latency: SW inp → SLDB in = ~630 ns

All Internal & External Hardware Paths Checked
Remaining Firmware

**TAB**

- Tau algorithm to be verified
- Change to Atlas EM algo ?
- Finalize L2 output
- Finalize monitoring
- Simulation of full TAB

**GAB**

- Only skeleton of Global chip firmware exists
  - Need to add
    - Trigger Terms
    - Monitoring
    - L2 output
What’s Next?

• If we’re given the Green Light – produce:
  ◆ 10 TABs
  ◆ 3 GABs

<table>
<thead>
<tr>
<th>Task</th>
<th>Dur</th>
<th>Start</th>
<th>End</th>
</tr>
</thead>
<tbody>
<tr>
<td>Delivery of rest of components</td>
<td>2w</td>
<td>10/11/04</td>
<td>10/22/04</td>
</tr>
<tr>
<td>Assemble boards (mainly Columbia administration)</td>
<td>6w</td>
<td>10/11/04</td>
<td>11/19/04</td>
</tr>
<tr>
<td>Test TABs/GABs at Nevis</td>
<td>12w</td>
<td>11/22/04</td>
<td>02/11/05</td>
</tr>
</tbody>
</table>

• Testing at Fermilab
  ◆ Have (nearly) enough hardware now for Nevis + DØ Tests
    ◆ 2 VME/SCLs; 2 TABs; 1 GAB; 2 TAB/GAB crates
  ◆ Can send out some new boards as they pass tests
Conclusions

We believe that we’re ready to assemble

- hardware has been checked
  - no changes from prototype
- all components ordered (most arrived) + PCBs here
- money is in hand (Hal’s CAREER grant)

Risks of Going Forward

- TAB: essentially none
- GAB: some hardware paths not yet fully tested

Risks of Delay

- PCBs are aging (produced ~1 year ago)
- Atlas efforts intensifying

THANKS to the Committee for their Help!
Extra Slides
Simple “1x2 or 2x1” Algorithm

- Serial Adders
- EM(0,0)
- EM(0,1)
- EM(1,0)
- EM(1,1)
- LM Finder

- Serial Adders
- EM(0,0)
- EM(0,1)
- EM(1,0)
- EM(0,0)
- LM Finder

- “2x2” EM Algo
- “1x2 or 2x1” EM Algo

- No extra latency
- Chosen cluster still indexed by LL corner of 2x2 region
Data in the TAB

INPUT CABLE [h[e][e][e][e][e][e][e]]

OUTPUT LHS

ICR data: [1-0][28-39][10-2]

Tab 2
phi-region 7-4
data needed
cia: 37-2, 33-30, 1-0
phi: 10-2

ICR Mapping (source):
[he][e][e][e][e][e][e][e]

Numbering Conventions:
phi: 0.3, 0.1
p: 0.30

H. Evans
EM/Jet/Tau Results

- for each algo & $\phi = 2,3,4,5$ send out 12-bit word encoding highest threshold (7-1 or 0=none) passed by each of the four $\eta$’s in that $\phi$

<table>
<thead>
<tr>
<th>$\phi$</th>
<th>11</th>
<th>09</th>
<th>08</th>
<th>06</th>
<th>05</th>
<th>03</th>
<th>02</th>
<th>00</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$i$</td>
<td>highest thr $\eta=5$</td>
<td>highest thr $\eta=4$</td>
<td>highest thr $\eta=3$</td>
<td>highest thr $\eta=2$</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Global Sums

- for each $\phi = 2,3,4,5$ send out 12-bit word containing $\Sigma EM+HD$ over four $\eta$’s in that $\phi$

<table>
<thead>
<tr>
<th>$\phi$</th>
<th>11</th>
<th>00</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$i$</td>
<td>$\Sigma E_T (EM+HD)$ over $\eta = 2,3,4,5$</td>
<td></td>
</tr>
</tbody>
</table>

Simulation Code for all this

1. tsim_l1cal2b relies on DØ software environ.
2. standalone being tested w/ hardware
**TAB to GAB Data**

- **EM/Jet/Tau Results**
  - for each algo & $\phi = 2,3,4,5$ send out encoded 12-bit words for $\eta = S,C,N$ containing 2-bit counts of no. of objects passing each of 6 thresholds

<table>
<thead>
<tr>
<th>$\phi$</th>
<th>$\eta$</th>
<th>11</th>
<th>10</th>
<th>09</th>
<th>08</th>
<th>07</th>
<th>06</th>
<th>05</th>
<th>04</th>
<th>03</th>
<th>02</th>
<th>01</th>
<th>00</th>
</tr>
</thead>
<tbody>
<tr>
<td>$i$</td>
<td>$j$</td>
<td>cnt thr-6</td>
<td>cnt thr-5</td>
<td>cnt thr-4</td>
<td>cnt thr-3</td>
<td>cnt thr-2</td>
<td>cnt thr-1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

$i = 2,3,4,5$ ; $j = S,C,N$

- **Global Sums**

<table>
<thead>
<tr>
<th>$\phi$</th>
<th>$\eta$</th>
<th>11</th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th>00</th>
</tr>
</thead>
<tbody>
<tr>
<td>2-5</td>
<td>0-39</td>
<td>$\Sigma E_T$ (EM+HD)</td>
<td></td>
<td></td>
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<td></td>
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<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2-5</td>
<td>0-39</td>
<td>$\Sigma E_x$ (EM+HD)</td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2-5</td>
<td>0-39</td>
<td>$\Sigma E_y$ (EM+HD)</td>
<td></td>
<td></td>
<td></td>
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</tbody>
</table>
## Data to Cal-Track Match

### Output from TAB Global Chip (10)

<table>
<thead>
<tr>
<th>No.</th>
<th>Bits 15 – 08</th>
<th>Bits 07 – 00</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>JET Mask: $\phi = i+3$</td>
<td>EM Mask: $\phi = i+3$</td>
</tr>
<tr>
<td>2</td>
<td>JET Mask: $\phi = i+2$</td>
<td>EM Mask: $\phi = i+2$</td>
</tr>
<tr>
<td>3</td>
<td>JET Mask: $\phi = i+1$</td>
<td>EM Mask: $\phi = i+1$</td>
</tr>
<tr>
<td>4</td>
<td>JET Mask: $\phi = i$</td>
<td>EM Mask: $\phi = i$</td>
</tr>
<tr>
<td>5</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>6</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>7</td>
<td>Longitudinal Parity</td>
<td></td>
</tr>
</tbody>
</table>

### Mask Definition:

- **Bit 07** unused
- **Bits 06 – 00** set if threshold $j$ is passed

www.nevis.columbia.edu/~evans/l1cal/hardware/tab/tab_to_caltrack.html
## Short Term Plans

<table>
<thead>
<tr>
<th>Task</th>
<th>Comments</th>
<th>Timescale</th>
</tr>
</thead>
<tbody>
<tr>
<td>Simulation</td>
<td>Shift studies into high gear</td>
<td>now</td>
</tr>
<tr>
<td>TAB → L2/L3</td>
<td>Write data to tape (test unpacking)</td>
<td>Oct</td>
</tr>
<tr>
<td>ADFv1 → TAB</td>
<td>Long Term Data Transfer Tests</td>
<td>Oct</td>
</tr>
<tr>
<td>TAB/GAB</td>
<td>Fully Automated Event Verification</td>
<td>Nov</td>
</tr>
<tr>
<td>GAB</td>
<td>Implement 1st And/Or terms</td>
<td>End 04</td>
</tr>
<tr>
<td>ADFv2 → TAB</td>
<td>First Integration</td>
<td>End 04</td>
</tr>
</tbody>
</table>
1. Operations & Stability
   a. crashes/deadtime
   b. reliable downloading
   c. monitoring tools
   d. param determination
   e. unpacker/reco stable

2. Trigger Quality
   a. rates & efficiencies
      ♦ filter coeff’s, thresholds, and/or terms, trigger list
   b. trigger definitions (L1,L2,L3)
      in place well beforehand

Note: all of these must be Documented
Testing Trigger Quality

Splitters ⇒ Data Available before Installation
  ◆ at most 16-EM + 16-H ⇒ cannot test Sliding Windows

Possible Chain to Rate/Eff Estimates

1. Define Triggers
   ◆ trig-list, and/or, thresh, filt. coeff’s

2. Using Splitter Data derive TT response
   ◆ compare ADF Et(TT) output w/ Precision Readout ⇒ correct MC modeling of Et(TT)
   ◆ probe pathological cases using TWG

3. MC models TAB Algorithms
   ◆ sliding windows algorithm is deterministic
   ◆ use standalone MC to look for algorithm pathologies

4. MC models And/Or terms & Trigger List ⇒ Rates & Eff’s
   ◆ need to test QCD MC vs. Data w/ Run Ila Trigger