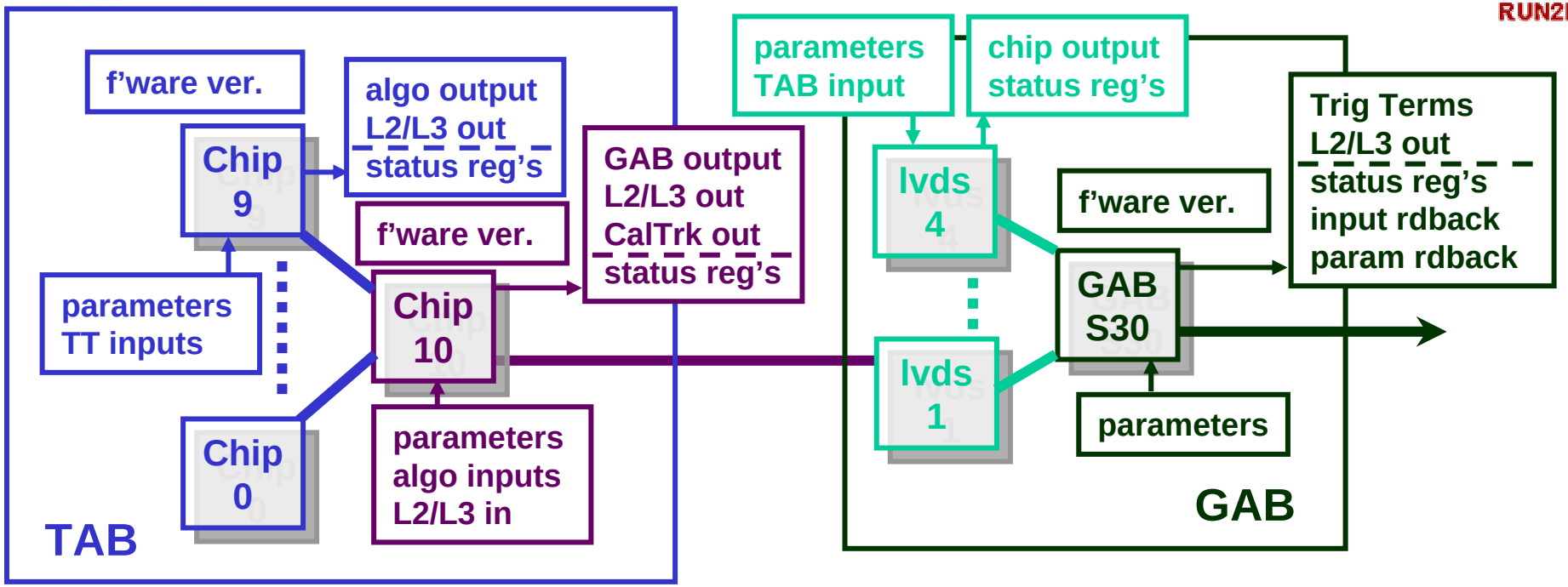
TAB & GAB Algorithms Hardware vs Simulation

Hal Evans **(based on work by Chad Johnson)** **Indiana U.**

1. **Hardware Testing of Algorithms at Nevis**
2. **Data Transmission in the TAB/GAB System**
3. **Hardware vs Simulation**

Test Memories in the TAB & GAB



Nevis Test Setup same as Fermilab

- 1 VME/SCL, 8 TABs, 1 GAB
- SCL timing from VME/SCL
  - Init, CLK7, TURN, L1Accept
- BC,Turn #'s gen internally on TAB and GAB
  - as in normal running

All Test Memories: 32 events deep

- except GAB lvds "TAB input" memories (1 evt)

Out Mem's filled on VME/SCL Pulse

- except stat reg's (every evt)
- by VME cmd on specific BC

Test Modes

1. TAB→GAB: cycle continuously through same 32 test events at 132 ns per events
   - monitor GAB status register parity error counts
   - allows TAB-to-GAB BER measurements

2. Generate Input Files By Hand
   - check output memories by eye for expected behavior

3. Load Random-Data events
   - check that output results agree w/ parallel simulation of each event's data
     - parallel simulation = standalone code
     - but synchronized with Trigger Rate Tool Code
   - much slower than input rate – but tests algorithms

4. Load MC Generated Events
   - same checking code as for random events
   - uses ancient *l1cal2b_analyze* root-tuples: needs updating

Data Xmit & Algo Checks

8 TABs → GAB Transmission

Events Sent	Checking Done	BER Limit
10^8	parity only	$< 1.7 \times 10^{-11}$
2.56×10^6	parity and data received=sent	$< 6.6 \times 10^{-10}$

Algorithm Tests

Algo	Data Used	Data Source	Checked at	# Events
EM (old)	random	Chips 0-9	Chips 0-9	1.6×10^7
Jet	random	Chips 0-9	Chips 0-9	1.6×10^7
Tau	by hand	Chips 0-9	Chips 0-9	few
Et(miss)	random	Chips 0-9	Chips 0-9	1.6×10^7
TAB Data for GAB	random	Chips 0-9	Chip 10	1.6×10^7
TAB data for L2/L3	by hand	Chips 0-9	Chip 10	few
CSWEM Trig Terms	by hand	Chips 0-9	GAB S30	~100
Other Trig Terms	by hand	Chips 0-9	GAB S30	few