A Brief Description of FRC Interrupt Processing

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■ Interrupt Source

There are two interrupt sources in the FRC, one is SCL Initialization Request Interrupt, it's called as SCL_REQ Interrupt; other is Monitor Data Collection Request Interrupt. It's called as Mon_REQ Interrupt.

• SCL_REQ Interrupt
SCL_REQ Interrupt signal is connected with the INTA pin of PCIBUS 3 in the FRC, and the INTA pin is routed to the LINT0 input of Universe II chip in the motherboard.

• Mon_REQ Interrupt
Mon_REQ Interrupt signal is connected with the INTB pin of PCIBUS 3 in the FRC, and the INTB pin is routed to the LINT1 input of Universe II chip in the motherboard.

■ Initialization of Universe II

There are two steps of FRC interrupt initialization for Universe II chip:

• Enable Two Interrupt Sources (LINT0, LINT1)
Any FRC interrupt source must be individually enabled in VINT_EN register (Table A.61, Universe II User manual: App A-71). Writing a data (0x03) to VINT_EN register to set LINT0 (bit 0) and LINT1 (bit 1) to one.

• Mapping LINT0 and LINT1 to the particular VMEBUS interrupt level.
Any FRC interrupt source can be mapped to any one of seven VMEBUS interrupt level in the VINT_MAP0 register (Table A.63, Universe II User manual: App A-75). Writing a data to VINT_MAP0 register to set LINT0 (bits 2~0) and LINT1 (bits 6~4) to the particular VMEBUS interrupt level.
For example: For SCL_REQ interrupt (LINT0), A value of B"001" (bits 2~0) maps it to IRQ*[1], a value of B"002" maps it to IRQ*[2], etc. A value of B"000" effectively masks the interrupt since there is no corresponding IRQ*[0].

■ Clear Interrupt Sources

All VMEbus interrupts generated by the Universe II are RORA, except for the software interrupts which are ROAK. For FRC, this means that VMEbus interrupt output remains asserted until cleared by a register access. Writing a "one" to the relevant bit in the VINT_STAT (Table A.62, Universe II User manual: App A-73) register clears that interrupt source. However, since PCI interrupts are level-sensitive, if an attempt is made to clear the VMEbus interrupt while the LINT# pin is still asserted, the VMEbus interrupt remains asserted. This causes a second interrupt to be generated to the VMEbus. For this reason, a VMEbus interrupt handler should clear the source of the PCI interrupt before clearing the VMEbus interrupt. So, there are two steps for clearing the interrupt source in the Interrupt Processing Subroutine of CPU for each interrupt.

- Clear SCL_REQ interrupt
  1. Writing a PCI command (CPU_Clr_SCLInt*) to clear the SCL_REQ source in the FRC board.
  2. Writing a "one" to the bit 0 in the VINT_STAT to clear the VMEbus interrupt output signal.

- Clear Mon_REQ interrupt
  1. Writing a PCI command (CPU_Clr_MonInt*) to clear the Mon_REQ source in the FRC board.
  2. Writing a "one" to the bit 1 in the VINT_STAT to clear the VMEbus interrupt output signal.

*: see the document of "A Description of Bits Definition of Registers"

Appendix: Relevant Registers in Universe II chip

Table A.61 : VMEbus Interrupt Enable Register (VINT_EN)

Register Name: VINT_EN								Offset:310
Bits	**Function**							
31-24	SW_INT7	SW_INT6	SW_INT5	SW_INT4	SW_INT3	SW_INT2	SW_INT1	Reserved
23-16	Reserved				MBOX3	MBOX2	MBOX1	MBOX0
15-08	Reserved			SW_INT	Reserved	VERR	LERR	DMA
07-00	LINT7	LINT6	LINT5	LINT4	LINT3	LINT2	LINT1	LINT0

Table A.62 : VMEbus Interrupt Status Register (VINT_STAT)

Register Name: VINT_STAT	Offset:314

Bits	Function							
31-24	SW_INT7	SW_INT6	SW_INT5	SW_INT4	SW_INT3	SW_INT2	SW_INT1	Reserved
23-16	Reserved				MBOX3	MBOX2	MBOX1	MBOX0
15-08	Reserved			SW_INT	Reserved	VERR	LERR	DMA
07-00	LINT7	LINT6	LINT5	LINT4	LINT3	LINT2	LINT1	LINT0

Table A.63 : VME Interrupt Map 0 Register (VINT_MAP0)

Register Name: VINT_MAP0	Offset: 318

Bits	Function			
31-24	Reserved	LINT7	Reserved	LINT6
23-16	Reserved	LINT5	Reserved	LINT4
15-08	Reserved	LINT3	Reserved	LINT2
07-00	Reserved	LINT1	Reserved	LINT0