STT J3 Backplane

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1. Introduction

This document describes the changes to the standard DØ J3 backplane required for the STT. It is an extension of the information presented in the VRB Subrack J3 Backplane document[1]. Information is also available in the STT Motherboard documentation[2]. A previous version of some of the STT J3 backplane can be found on Eric Hazen's DØ homepage[3] Items highlighted in yellow show changes from information in the VRB J3 Backplane document 1.

2. Crate Layout

Slot	Module	Transition Module	J3 Connector	Pinout
1	CPU	—	DIN	—
2	—	—	DIN	—
3	—	—	DIN	—
4	VBD	—	DIN	Table 3
5	—	—	Terminator?	—
6	—	—	Hard Metric	—
7	—	—	Terminator?	—
8	TFC-1	—	Hard Metric	Table 4
9	STC-1	VTM	Hard Metric	Table 4
10	STC-2	VTM	Hard Metric	Table 4
11	STC-3	VTM	Hard Metric	Table 4
12	STC-4	VTM	Hard Metric	Table 4
13	FRC	VTM	Hard Metric	Table 5
14	STC-5	VTM	Hard Metric	Table 4
15	STC-6	VTM	Hard Metric	Table 4
16	STC-7	VTM	Hard Metric	Table 4
17	STC-8	VTM	Hard Metric	Table 4
18	STC-9	VTM	Hard Metric	Table 4
19	TFC-2	—	Hard Metric	Table 4
20	—	—	Hard Metric	—
21	—	—	Terminator	—

Table 1: STT crate slot assignment

3. J3 Connector Pin Assignments

J3 Pins	Signal Name	Backplane Operation	Signal Type	Direction BM – BC
C1-C8	FRC_MESSAGE[0-7]		TTL	⇒
C9-C12	FRC_COMMAND[0-3]		TTL	⇒
C13	FRC_STROBE		TTL	⇒
C14	PUT_DONE	AND	TTL #	⇐
C15	PUT_DONE*	OR	TTL #	⇐
C16	GET_DONE	AND	TTL #	⇐
C17	GET_DONE*	OR	TTL #	⇐
C18	L1_BUSY*	OR	TTL #	⇐
C19	L2_BUSY*	OR	TTL #	⇐
C20	L1_ERROR*	OR	TTL #	⇐
C21	L2_ERROR*	OR	TTL #	⇐
C22-C23	free		TTL #	⇐
C24-C25	free (reserved in VRB)		TTL #	⇐
# Signal is a TTL input to the FRC. Other modules should provide as a totem-pole TTL/LVTTL output.				

Table 2: Bussed lines on J3

J3 Pin Connections		
VBD (slot 4)	**FRC** (slot 13)	**VBD Name**
C08	C42	SRDY
C09	C43	reserved
C10	C44	DONE

Table 3: VBD - FRC communication lines on J3.

Pin	Row A	Row B	Row C	Row D	Row E
1	L0_D0	GND	MESSAGE[0]	GND	L2_D0
2	L0_D1	L0_D2	MESSAGE[1]	L2_D2	L2_D1
3	GND	L0_D3	MESSAGE[2]	L2_D3	GND
4	L0_D5	L0_D4	MESSAGE[3]	L2_D4	L2_D5
5	L0_D6	GND	MESSAGE[4]	GND	L2_D6
6	L0_D7	L0_D8	MESSAGE[5]	L2_D8	L2_D7
7	GND	L0_D9	MESSAGE[6]	L2_D9	GND
8	L0_D11	L0_D10	MESSAGE[7]	L2_D10	L2_D11
9	L0_D12	GND	COMMAND[0]	GND	L2_D12
10	L0_D13	L0_D14	COMMAND[1]	L2_D14	L2_D13
11	GND	L0_D15	COMMAND[2]	L2_D15	GND
12	L0_D16	L0_D16	COMMAND[3]	L2_D16	L2_D16
13	L0_D17	GND	STROBE	GND	L2_D17
14	L0_D17	L0_D18	PUT_DONE	L2_D18	L2_D17
15	GND	L0_D18	PUT_DONE*	L2_D18	GND
16	L0_D19	L0_D19	GET_DONE	L2_D19	L2_D19
17	L0_CAV*	GND	GET_DONE*	GND	L2_CAV*
18	L0_DAV*	L0_LNKRDY*	SCL_L1BSY*	L2_LNKRDY*	L2_DAV*
19	GND	L0_LNKRDY*	SCL_L2BSY*	L2_LNKRDY*	GND
20	L0_STRBOUT	GND	SCL_L1ERR*	GND	L2_STRBOUT
21	L0_SIG_DETECT	L0_ERROR	SCL_L2ERR*	L2_ERROR	L2_SIG_DETECT
22	GND	L0_ERROR	status[8]	L2_ERROR	GND
23	GND	GND	status[9]	GND	GND
24	GND	GND	status[10]	GND	GND
25	GND	GND	status[11]	GND	GND
26	L1_CAV*	GND	GND	GND	L3_CAV*
27	L1_DAV*	L1_LNKRDY*	GND	L3_LNKRDY*	L3_DAV*
28	GND	L1_LNKRDY*	GND	L3_LNKRDY*	GND
29	L1_STRBOUT	GND	GND	GND	L3_STRBOUT
30	L1_SIG_DETECT	L1_ERROR	GND	L3_ERROR	L3_SIG_DETECT
31	GND	L1_ERROR	GND	L3_ERROR	GND
32	L1_D0	GND	n.c.	GND	L3_D0
33	L1_D1	L1_D2	n.c.	L3_D2	L3_D1
34	GND	L1_D3	n.c.	L3_D3	GND
35	L1_D5	L1_D4	n.c.	L3_D4	L3_D5
36	L1_D6	GND	GND	GND	L3_D6
37	L1_D7	L1_D8	GND	L3_D8	L3_D7
38	GND	L1_D9	GND	L3_D9	GND
39	L1_D11	L1_D10	GND	L3_D10	L3_D11
40	L1_D12	GND	GND	GND	L3_D12
41	L1_D13	L1_D14	n.c.	L3_D14	L3_D13
42	GND	L1_D15	n.c.	L3_D15	GND
43	L1_D16	L1_D16	n.c.	L3_D16	L3_D16
44	L1_D17	GND	n.c.	GND	L3_D17
45	L1_D17	L1_D18	SERIAL	L3_D18	L3_D17
46	GND	L1_D18	RESET*	L3_D18	GND
47	L1_D19	L1_D19	MODID	L3_D19	L3_D19

Table 4: J3 connector pin assignments for STC/TFC slots. Outer rows of connector (Z and F) are all GND.

Pin	Row A	Row B	Row C	Row D	Row E
1	L0_D0	GND	MESSAGE[0]	GND	L2_D0
2	L0_D1	L0_D2	MESSAGE[1]	L2_D2	L2_D1
3	GND	L0_D3	MESSAGE[2]	L2_D3	GND
4	L0_D5	L0_D4	MESSAGE[3]	L2_D4	L2_D5
5	L0_D6	GND	MESSAGE[4]	GND	L2_D6
6	L0_D7	L0_D8	MESSAGE[5]	L2_D8	L2_D7
7	GND	L0_D9	MESSAGE[6]	L2_D9	GND
8	L0_D11	L0_D10	MESSAGE[7]	L2_D10	L2_D11
9	L0_D12	GND	COMMAND[0]	GND	L2_D12
10	L0_D13	L0_D14	COMMAND[1]	L2_D14	L2_D13
11	GND	L0_D15	COMMAND[2]	L2_D15	GND
12	L0_D16	L0_D16	COMMAND[3]	L2_D16	L2_D16
13	L0_D17	GND	STROBE	GND	L2_D17
14	L0_D17	L0_D18	PUT_DONE	L2_D18	L2_D17
15	GND	L0_D18	PUT_DONE*	L2_D18	GND
16	L0_D19	L0_D19	GET_DONE	L2_D19	L2_D19
17	L0_CAV*	GND	GET_DONE*	GND	L2_CAV*
18	L0_DAV*	L0_LNKRDY*	SCL_L1BSY*	L2_LNKRDY*	L2_DAV*
19	GND	L0_LNKRDY*	SCL_L2BSY*	L2_LNKRDY*	GND
20	L0_STRBOUT	GND	SCL_L1ERR*	GND	L2_STRBOUT
21	L0_SIG_DETECT	L0_ERROR	SCL_L2ERR*	L2_ERROR	L2_SIG_DETECT
22	GND	L0_ERROR	status[8]	L2_ERROR	GND
23	GND	GND	status[9]	GND	GND
24	GND	GND	status[10]	GND	GND
25	GND	GND	status[11]	GND	GND
26	L1_CAV*	GND	GND	GND	L3_CAV*
27	L1_DAV*	L1_LNKRDY*	GND	L3_LNKRDY*	L3_DAV*
28	GND	L1_LNKRDY*	GND	L3_LNKRDY*	GND
29	L1_STRBOUT	GND	GND	GND	L3_STRBOUT
30	L1_SIG_DETECT	L1_ERROR	GND	L3_ERROR	L3_SIG_DETECT
31	GND	L1_ERROR	GND	L3_ERROR	GND
32	L1_D0	GND	n.c.	GND	L3_D0
33	L1_D1	L1_D2	n.c.	L3_D2	L3_D1
34	GND	L1_D3	n.c.	L3_D3	GND
35	L1_D5	L1_D4	n.c.	L3_D4	L3_D5
36	L1_D6	GND	GND	GND	L3_D6
37	L1_D7	L1_D8	GND	L3_D8	L3_D7
38	GND	L1_D9	GND	L3_D9	GND
39	L1_D11	L1_D10	GND	L3_D10	L3_D11
40	L1_D12	GND	GND	GND	L3_D12
41	L1_D13	L1_D14	n.c.	L3_D14	L3_D13
42	GND	L1_D15	SRDY (4-C08)	L3_D15	GND
43	L1_D16	L1_D16	res (4-C09)	L3_D16	L3_D16
44	L1_D17	GND	DONE (4-C10)	GND	L3_D17
45	L1_D17	L1_D18	SERIAL	L3_D18	L3_D17
46	GND	L1_D18	RESET*	L3_D18	GND
47	L1_D19	L1_D19	MODID	L3_D19	L3_D19

Table 5: J3 connector pin assignments for FRC slots (VTM compatible). Outer rows of connector (Z and F) are all GND. Pins C42-C44 are connected to pins C08-C10 in slot 4 (the VBD).

References

[1] *VRB Subrack J3 Backplane (Rev. B)*, ESE-SVX-512629 (01/11/00), http://www-ese.fnal.gov/eseproj/svx/j3_bkpln/J3BKPLN_VRB_REVB.pdf see also *VRB/FIB Custom Backplane*, ESE-SVX-960130 (01/05/00), http://www-ese.fnal.gov/kwtemp/j3%26conn.htm
[2] http://ohm.bu.edu/~hazen/my_d0/mb9u/
[3] http://ohm.bu.edu/~hazen/my_d0/