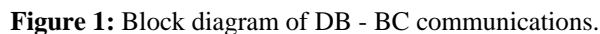


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The current design of the Buffer Controller (BC) makes several requirements on the daughterboards (DB) that supply it with data to be stored in its memory for every L1 Accept. A simplified block diagram of the DB – BC communications is given in Fig. 1.



The life of the BC is made easier if the L3 Data Buffers on the DBs are FIFOs. This allows PCI block reads to always be performed from the same address.

3) Size of the Buffer

The required depth of the L3 Data Buffers on the various DBs is set by PCI-3 occupancy issues. This is discussed in detail in *PCI Bus-3 Use and Data Buffering*¹. To summarize, the minimum depth in 32-bit words required for the L3 Data Buffers on the different DBs is:

FRC	154	words
STC	9216	words
TFC	6267	words

4) Format of the Data

Data in the L3 Data Buffers should be stored in a format as close as possible to that expected by the VBD when it reads out the BC Output FIFO. This way, the BC has to do as little reformatting as possible. There are three requirements imposed on the DB L3 data by the BC. The BC performs checks on all three of these and generates errors if any of them fail.

- 1) BX as received by the DB should be stored in the lowest 8 bits of the first word in the DB's L3 data.
- 2) The total number of 32-bit words in the DB's L3 data, including the final checksum, should be included as the next-to-last word in the L3 data.
- 3) A checksum (vertical parity) should be included as the last word in the DB's L3 data.

The format of the L3 data block from the DBs is shown in Table 1

31	24	23	16	15	8	7	0
<i>unused</i>		<i>unused</i>		reserved for BC		BX	
Data							
....							
Data							
Total Word Count (including checksum)							
32-bit checksum (vertical parity)							

Table 1: Possible format for L3 data from DBs.

5) Transferring Data to the Buffer Controller

Transfer of data from the L3 Data Buffer on the DB to the BC will be done as a PCI block transfer with the BC acting as Master and the DB as Target. (This simplifies the DB PCI-3 interface.) Since the BC knows neither when the L3 Data Buffer is ready with an event's worth of data to transfer nor how much data is present, a standard PCI block transfer cannot be done. Two additional features are necessary:

- 1) The DB must signal the BC that the L3 Data Buffer is ready. This handshaking is done using the *SPARE0* (=DB_L3_DATA) *SPARE1* (=BC_BUSY) lines that are present in the *Updated Motherboard Spec*².
- 2) The DB must signal that it is transferring the last data word in the block to the BC. This is accomplished by having the DB PCI interface use *target-disconnect (without data) mode*.

5.1 Advertising Data Ready

The details of the L3 data transfer between the DB and the BC are driven by the fact that the BC must act as the master in this transaction (the DB is the target), however, the BC knows neither when the DB's L3 data is ready nor how many words are contained in that data. This requires some handshaking between the DB and the BC involving two special purpose lines (*DB_L3_DATA* and *BC_BUSY*, corresponding to *SPARE0* and *SPARE1* respectively on the motherboard – see the *Buffer Controller – Logic Daughterboard Communications* document³) as well as PCI signals involved in *target-disconnect-without-data* block transfers.

The steps in the handshaking are the following.

- 1) The DB indicates to the BC that it has L3 data to be transferred by asserting *DB_L3_DATA*. This can be done as soon as data appears in the DB's L3 FIFO or can wait until all data is present. (In the FRC *DB_L3_DATA* is raised as soon as data enters the FIFO).
- 2) When the BC sees *DB_L3_DATA*, it begins the process of requesting a PCI block transfer, which also requires information from the BM. (See the Altera Megacore manual for PCI details). The BC also asserts *BC_BUSY* as soon as it issues the request.
- 3) The DB signals the BC PCI interface that it is ready to transmit data as soon as all of its L3 data is stored in its L3 FIFO. This is done following standard PCI block transfer protocol. For example, in the FRC, *lt_rdyn* is asserted when the last L3 data word is loaded into the FIFO.
- 4) The BC begins the block transfer.
- 5) The block transfer is terminated by the DB after its last L3 word using the *target-disconnect-without-data* protocol. *DB_L3_DATA* should be deasserted at this time.

References

- ¹ *PCI Bus-3 Use and Data Buffering* http://www.nevis.columbia.edu/~evans/stt/sb_0700/PCI-3.pdf
- ² E. Hazen and S. Wu, *Motherboard Electrical Specification Update* (7 July, 2000)
- ³ *Buffer Controller – Logic Daughterboard Communications*
http://www.nevis.columbia.edu/~evans/stt/sb_0700/BC_DB.pdf