L3 transfers: Buffer Manager-Buffer Controller-VBD

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This document describes the transfer of L3 data from the buffer controller to the VBD. We describe the sequence of actions taken by the buffer manager, the buffer controller and the VBD.

L2 accepts are pipelined on the buffer manager. Once the buffer controllers have completed transferring an event to the output buffers, signaled by the AND of /GET_DONE going high, the buffer manager can initiate the next transfer of L2 data from the memory buffers to the output fifos by sending the next GET_BUFF message to the buffer controllers. The sequence for the buffer manager is:

- Send GET_BUFF message on J3 (number of next buffer in BC control memory)
- Send GET_BX message on J3 (BX for cross_check with L2 data)
- If /GET_DONE (and, first done) going low (polling), set GET_END low
- If GET DONE (and, all done) high, set GET END high
- Check VME status (MON_REQ and SCL_REQ)
- Set SRDY* (on J3)
- POLL DONE* (on J3)
- Clear SRDY*

Communication with the VBD is done using the two J3 signals SRDY and DONEⁱ. The buffer manager initiates a VBD transfer by asserting SRDY*. When the VBD is done, it releases the VME bus and asserts DONE*. The buffer manager has to then drop SRDY* so that the VBD can in turn release DONE*. Since the VBD holds on to the VME bus for the entire event, the buffer manager has to check MON_REQ before asking for a VBD transfer, ensuring that monitoring is finished.

The sequence for the buffer controllers is as follows:

- Receive GET_BUFF (number of next buffer in BC control memory)
- Receive GET_BX (BX for cross_check with L2 data)
- Transfer data from buffer to output fifo
- Count words and store word count in VME register (fifo)
- Check BX (send L2_error if mismatch)

- Upon completion of transfer to output fifo, set GET_DONE high, /GET_DONE low
- Poll GET_END, if GET_END, set GET_DONE low, /GET_DONE high

Note that separate lines for GET_DONE and /GET_DONE are needed on the VME J3 backplane to ensures proper handshaking (see Buffer Manager-Buffer Controller Document). The AND of GET_DONE signals that everyone is done while the AND of /GET_DONE is the OR of GET_DONE, signaling that the first buffer controller is done.

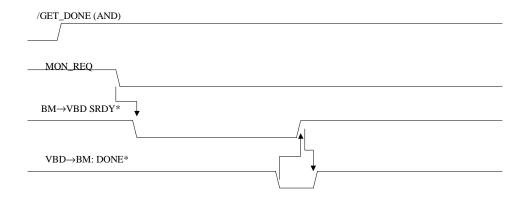


Fig 1: Timing diagram for L3 transfers to the VBD.

31	24	23 16	15	8 7 0
	unused	unused	source*	BX
Data				
•••				
Data				
Total Word Count*				
32-bit checksum				
	unused	unused	unused	errors*

Table 1: Format for L3 data from the Buffer Controllers. Entries that are added or modified by the buffer controllers are marked \ast .

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ⁱ VBD User Manual, G. Briskin et al., available at http://www.pa.msu.edu/hep/d0/12/hardware.html