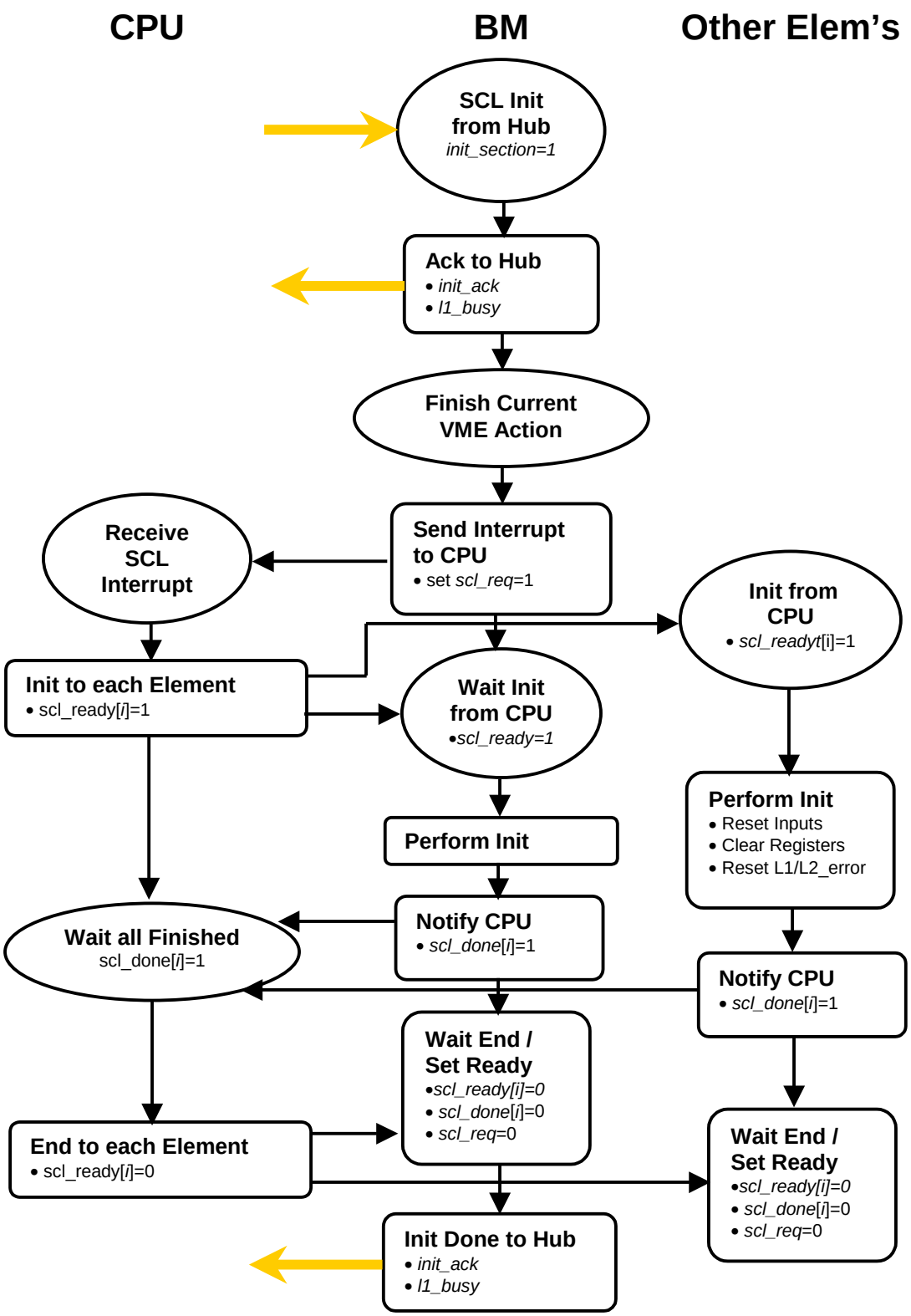
CPU
BM
Other Elem's
SCL Init from Hub
init_section=1
Ack to Hub
• init_ack
• l1_busy
Finish Current VME Action
Receive SCL Interrupt
Send Interrupt to CPU
• set scl_req=1
Init from CPU
• scl_readyt[i]=1
Init to each Element
• scl_ready[i]=1
Wait Init from CPU
•scl_ready=1
Perform Init
Perform Init
• Reset Inputs
• Clear Registers
• Reset L1/L2_error
Notify CPU
• scl_done[i]=1
Wait all Finished
scl_done[i]=1
Notify CPU
• scl_done[i]=1
Wait End / Set Ready
•scl_ready[i]=0
• scl_done[i]=0
• scl_req=0
End to each Element
• scl_ready[i]=0
Wait End / Set Ready
•scl_ready[i]=0
• scl_done[i]=0
• scl_req=0
Init Done to Hub
• init_ack
• l1_busy