Buffer Controller: Messages from BM

code version: 20-May-03
created in: pci3_lm.tdf, b_ctrl.tdf

Same structure used:
- *PCI3*/pci3_lm.tdf  PUT messages
- *buf_Ctrl*/b_ctrl.tdf  GET messages

<table>
<thead>
<tr>
<th></th>
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<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>[11..8] == 3</td>
<td>PUT_END</td>
<td>[11..0] == 0x600</td>
<td>GET_END</td>
</tr>
</tbody>
</table>
Signals for writing to the DPRAM
- Addr_L[16..0]  Address in DPRAM – upper 4 bits mark buffer boundaries
- CE1L           Chip enable
- ADS_Ln         Address strobe – load first address
- CNT_ENn        Counter enable – internal address counter

PCI Signals:
- lm_tsr[6]      target disconnect with data
- lm_ackn        local master acknowledge – asserted during data transfer
- lm_dxfmn       local master data transfer – asserted for successful transfer
- lm_req32n      local master request – asserted for 1 clock
Buffer Controller: Writing to the DPRAM – Addr & Data

code version: 20-May-03
created in: pci3_lm.tdf
Buffer Controller: Reading from the DPRAM

code version: 20-May-03
created in: b_ctrl.tdf

Signals for reading the DPRAM
- **Addr_R[16..0]** Address in DPRAM – upper 4 bits mark buffer boundaries
- **CE1_R** Chip enable – extends 1 clock due to DPRAM internal write delay
- **ADS_Rn** Address strobe – load first address
- **CNT_ENn** Counter enable – internal address counter
Buffer Controller: Buffer Reads – Internal Logic

code version: 13-Jun-03 (in preparation)
created in: b_ctrl.tdf
Buffer Controller: Buffer Reads – Pad Generation

code version: 20-May-03
created in: b_ctrl.tdf

For Block Size = 16 (pabs_bit = 4):
- \( N+1 = \text{No. (data words)} + \text{Checksum} + \text{ChkSumError} \) = No. words in Out FIFO (count from 1)
- \( \text{Buff}_{-}\text{OutD}_{-}\text{WC} = N+1 \) round to next 16 = WC read by SBC
- \( \text{L3}_{-}\text{WC}[5..4] = \text{Buff}_{-}\text{OutD}_{-}\text{WC}[5..4] + 1 \)
  \( \text{L3}_{-}\text{WC}[3..0] = 0 \)
- \( \text{Pad}_{-}\text{Cnt} \) = no. need to add to \( N \) to get \( N+1 \) = multiple of 16

<table>
<thead>
<tr>
<th>Buffer_OutD_WC (from Buffer)</th>
<th>Pad_Cnt</th>
<th>L3_WC (to WC FIFO)</th>
</tr>
</thead>
<tbody>
<tr>
<td>[5..4] [3..0]</td>
<td>[3..0]</td>
<td>[3..0]</td>
</tr>
<tr>
<td>all</td>
<td>[5..4]</td>
<td>[3..0]</td>
</tr>
<tr>
<td>0</td>
<td>00</td>
<td>0000</td>
</tr>
<tr>
<td>1</td>
<td>00</td>
<td>0000</td>
</tr>
<tr>
<td>14</td>
<td>00</td>
<td>1110</td>
</tr>
<tr>
<td>15</td>
<td>00</td>
<td>1111</td>
</tr>
<tr>
<td>16</td>
<td>01</td>
<td>0000</td>
</tr>
<tr>
<td>20</td>
<td>01</td>
<td>0100</td>
</tr>
</tbody>
</table>
Buffer Controller: Writing to FIFO

code version: 20-May-03
created in: b_ctrl.tdf