Proposed changes/refinements to system architecture:

- **Use point-to-point links (i.e. Channel Link) for road bus**
  - availability of 3-channel mezzanine cards makes this practical
  - many advantages for prototyping, modularity, expansion

- **Use standard PCI bus for mezzanine card interfaces**
  - Advantages:
    - no need to re-invent the bus!
    - easy prototyping with commercial hardware
    - guaranteed interchangeability of components
  - Disadvantages:
    - uses more logic
    - overhead in data transfers
    - harder to implement (maybe not true)

- **Existing commercial standards:**
  - **PC-MIP**
    - 47x99mm
    - 32 bit 33MHz PCI
  - **PMC**
    - 150x75 mm
    - 64 bit 66MHz PCI

- **Many commercial motherboards exist**
  - "Intelligent" carriers - VME CPU boards w/ PMC, PC-MIP sites
  - "non-Intelligent" carriers - VME-PCI bridge only
Major Issues for Motherboard/PCI-Based System

- Data formats across links
- LVDS-link receiver functionality - how much error checking?
- Road receiver from TFC -- how to broadcast to mezzanine cards
  This is particularly an issue for the STC
- How much processing to do on the motherboard for the VTM (G-link) inputs?
- Design of Level 3 buffering
- J3 backplane issues (can FRC use a VTM?)
- Hardware support for downloading / monitoring

- Many commercial motherboards exist
  "Intelligent" carriers - VME CPU boards w/ PMC, PC-MIP sites
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L2STT Crate Layout

Backplane connections not shown:
Level 3 buffering (J3 bus)
SCL Init/busy/error (J0 TBUS)
VTM Inputs (CTT, SMT)

24 Sept 1999 - E. Hazen
LVDS Point-to-Point Link Receiver
PC-MIP card with 32 bit 33MHz PCI

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Fiber Road Card (FRC)

- SCL Rx Card
- PC-MIP Card
- LVDS Tx (3)
- PC-MIP Card
- PC-MIP Card
- PC-MIP Card
- JTAG Test/Config
- Local VME Control
- VME-PCI Bridge
- Dual-Port Memory
- M Buffer Control
- Level 3 Buffer Control
- Level 3 Readout
- Initialization, Monitoring
Silicon Track Card (STC)

- SCL Rx Card
- PC-MIP Card
  - LVDS Rx
  - Road Bus
- PC-MIP Card
- PC-MIP Card
- PC-MIP Card
  - LVDS Tx to TFC
  - LVDS Tx to ZVC
- JTAG Test/Config
- Local VME Control
- VME-PCI Bridge
- Dual-Port Memory
- M Buffer Control
- Initialization, Monitoring
- SCL Init Busy, Error
- J0 VIPA TBUS
- VTM
- VIPA TBUS
- J3 AUX Bus
- SMT Data
- Level 3 Readout
- Initialization, Monitoring

E. Hazen - 3 Sept 1999
Track Fit Card (TFC)

E. Hazen - 3 Sept 1999