System Architecture Update

Proposed changes/refinements to system architecture:

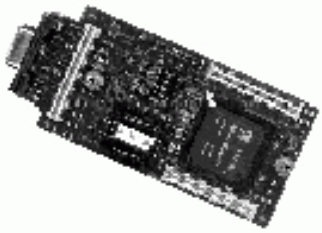
- Use point-to-point links (i.e. Channel Link) for road bus
  availability of 3-channel mezzanine cards makes this practical
  many advantages for prototyping, modularity, expansion

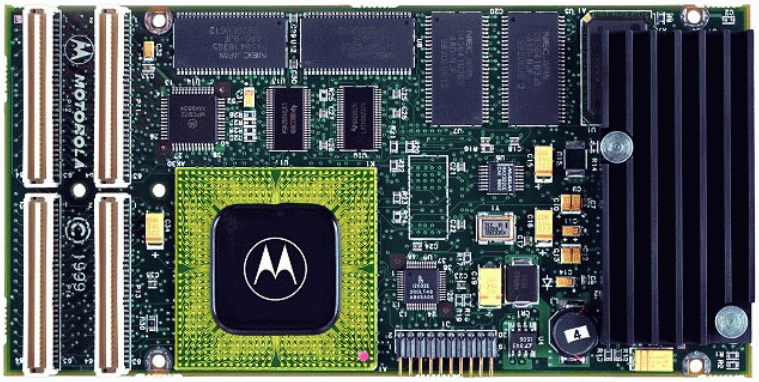
- Use standard PCI bus for mezzanine card interfaces
  Advantages:
  no need to re-invent the bus!
  easy prototyping with commercial hardware
  guaranteed interchangeability of components

  Disadvantages:
  uses more logic
  overhead in data transfers
  harder to implement (maybe not true)

- Existing commercial standards:

PC-MIP
47x99mm
32 bit 33MHz PCI





PMC
150x75 mm
64 bit 66MHz PCI

- Many commercial motherboards exist
  "Intelligent" carriers - VME CPU boards w/ PMC, PC-MIP sites
  "non-Intelligent" carriers - VME-PCI bridge only

System Architecture Update

Major Issues for Motherboard/PCI-Based System

- o Data formats across links
- o LVDS-link receiver functionality - how much error checking?
- o Road receiver from TFC -- how to broadcast to mezzanine cards
  This is particularly an issue for the STC
- o How much processing to do on the motherboard for the VTM (G-link) inputs?
- o Design of Level 3 buffering
- o J3 backplane issues (can FRC use a VTM?)
- o Hardware support for downloading / monitoring

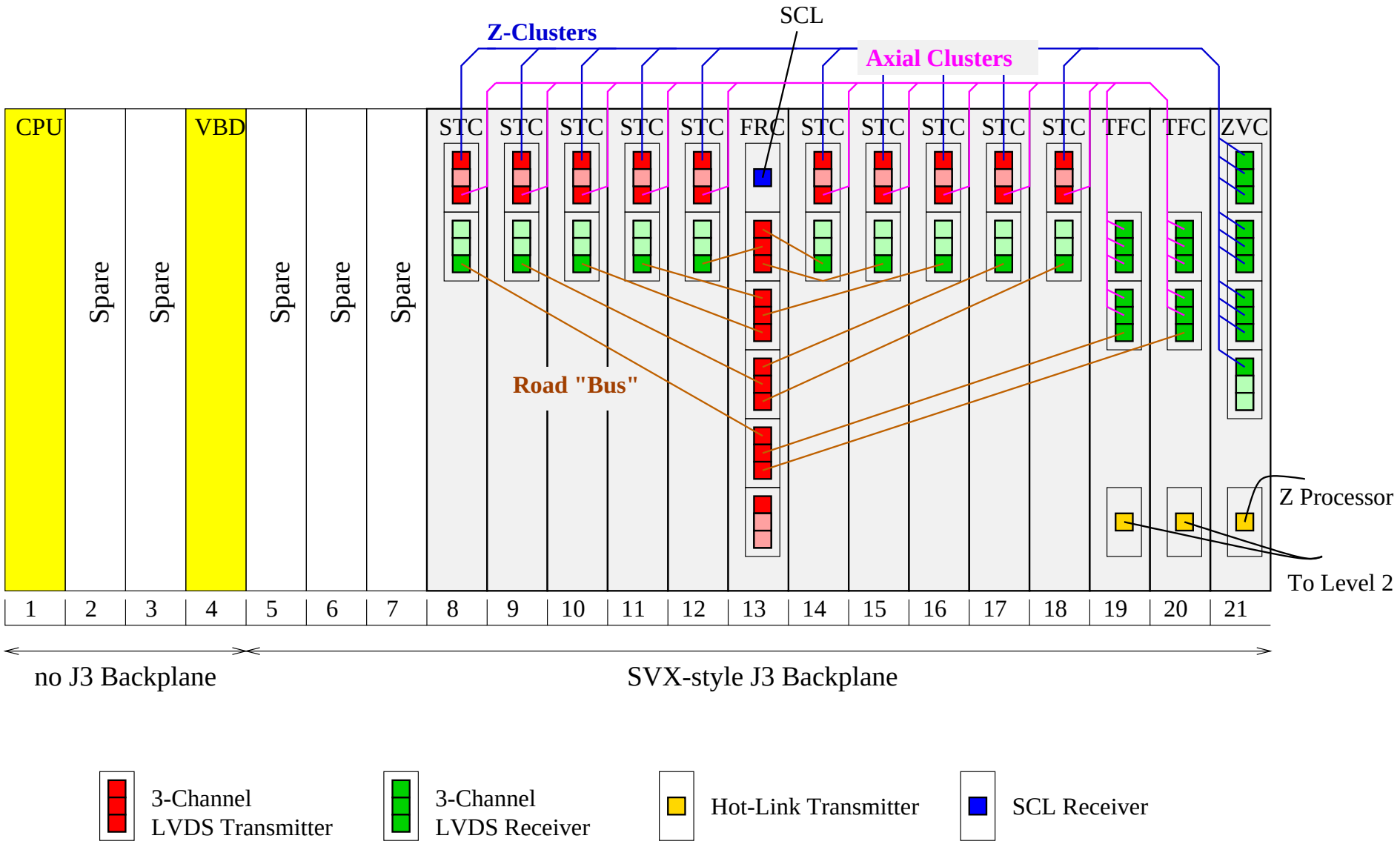
- o Many commercial motherboards exist
  "Intelligent" carriers - VME CPU boards w/ PMC, PC-MIP sites
  "non-Intelligent" carriers - VME-PCI bridge only

L2STT Crate Layout

24 Sept 1999 - E. Hazen

Backplane connections not shown:

- Level 3 buffering (J3 bus)
- SCL Init/busy/error (J0 TBUS)
- VTM Inputs (CTT, SMT)



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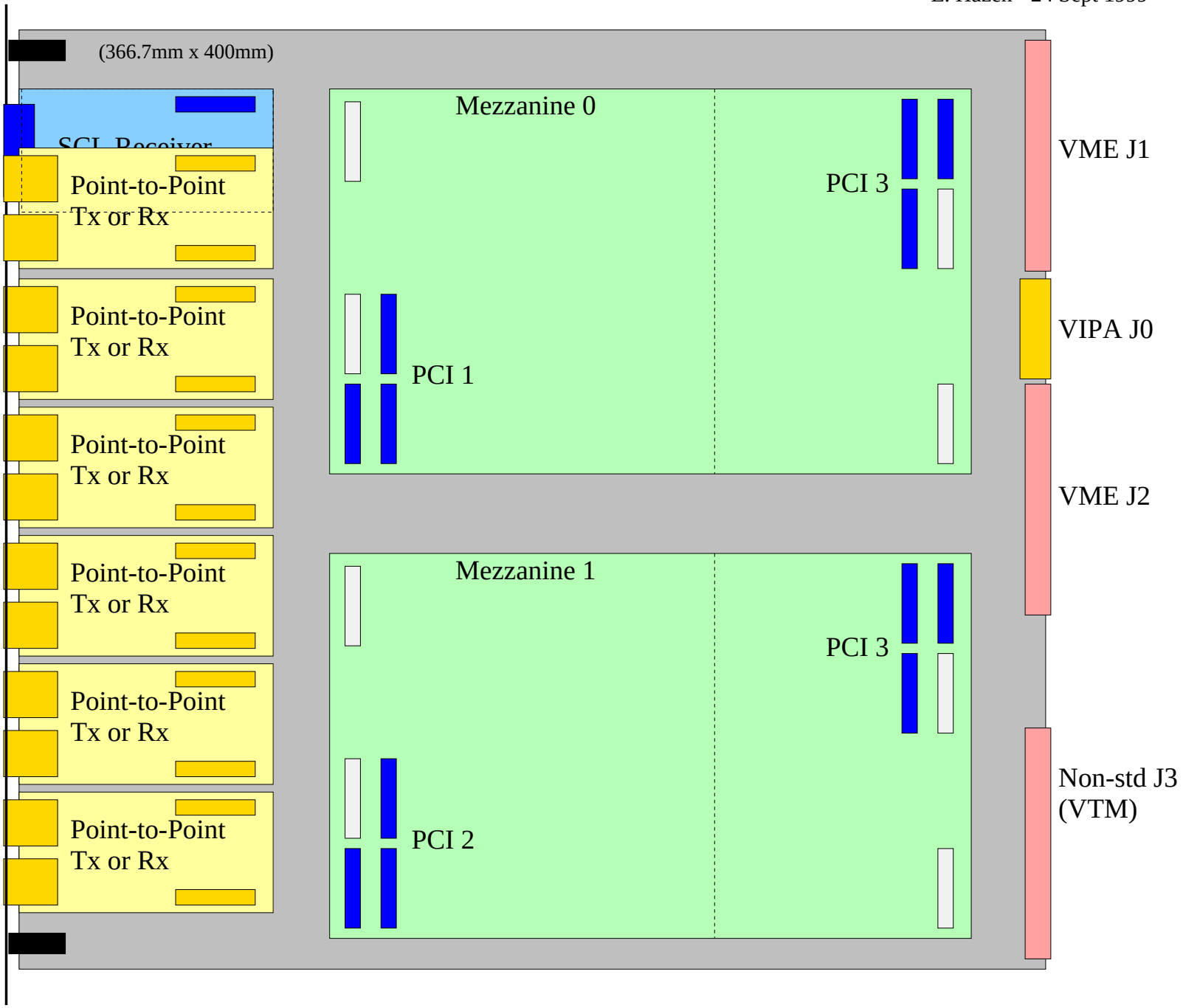

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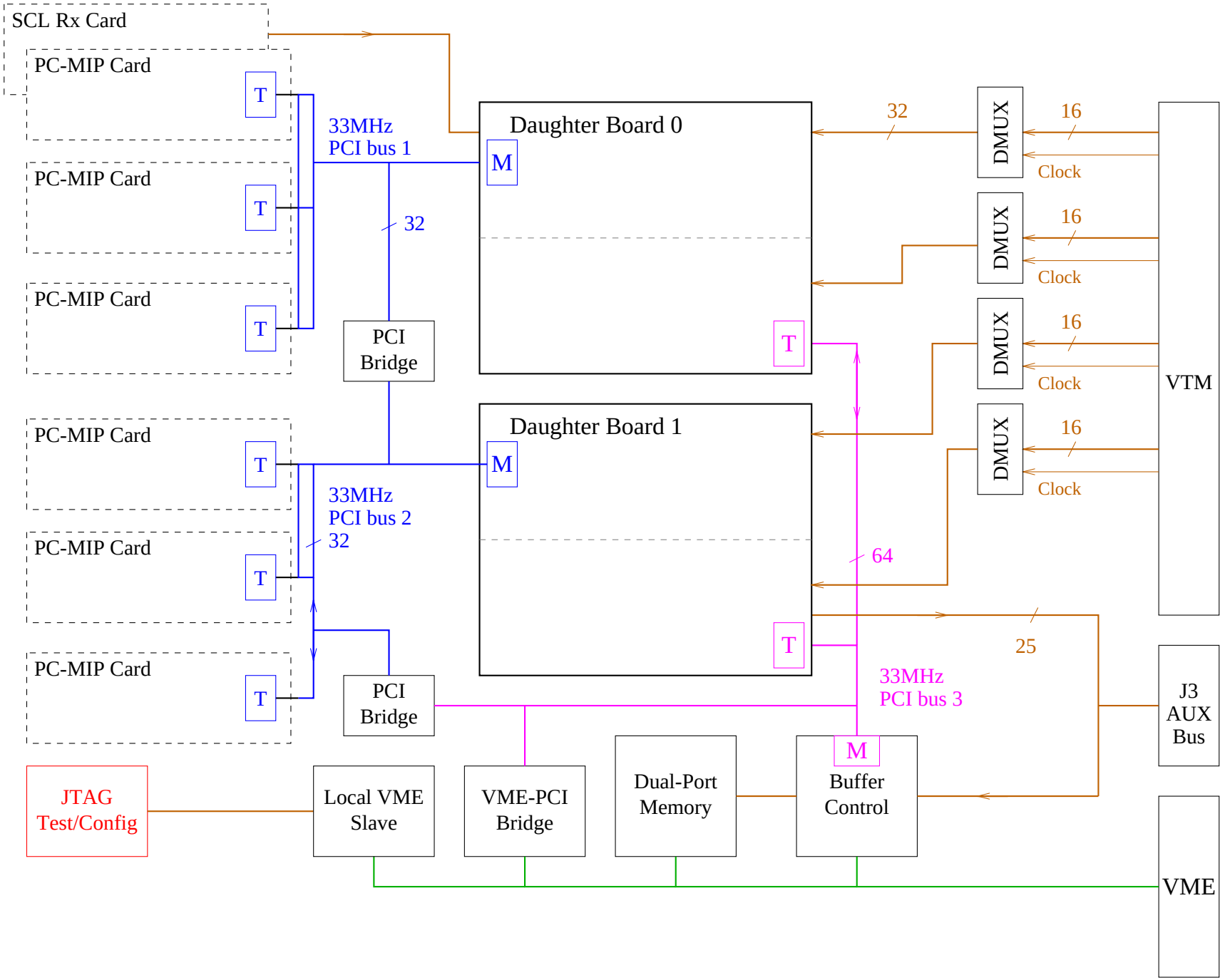

LVDS Point-to-Point Link Receiver
PC-MIP card with 32 bit 33MHz PCI

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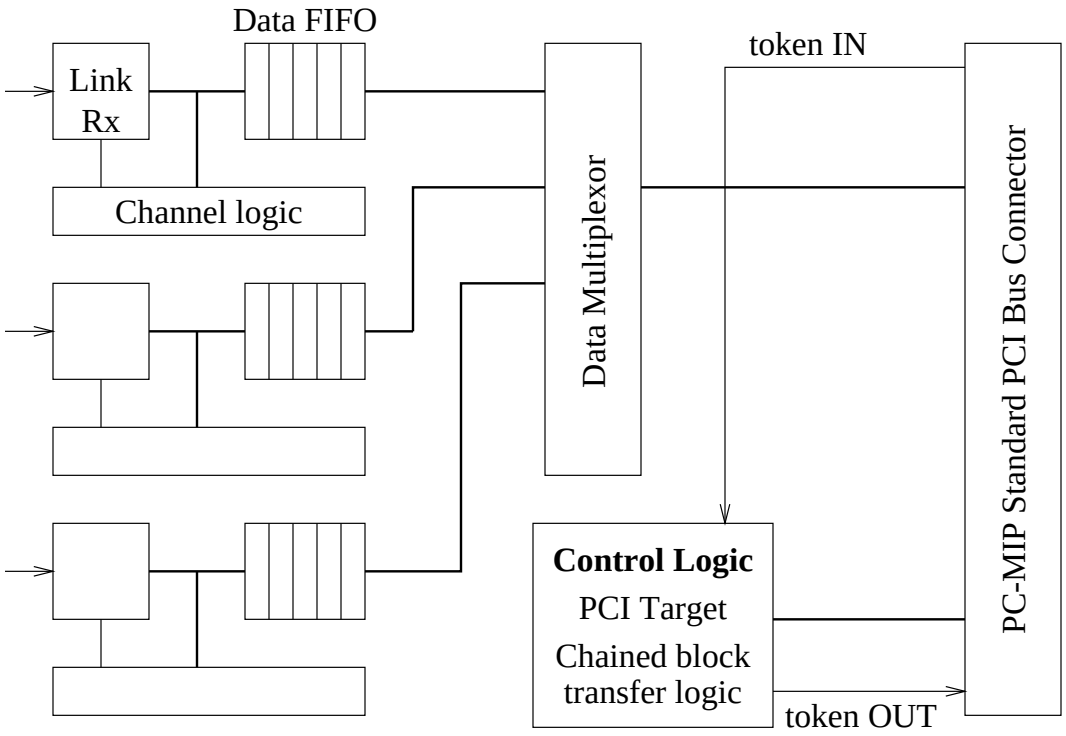

Fiber Road Card (FRC)

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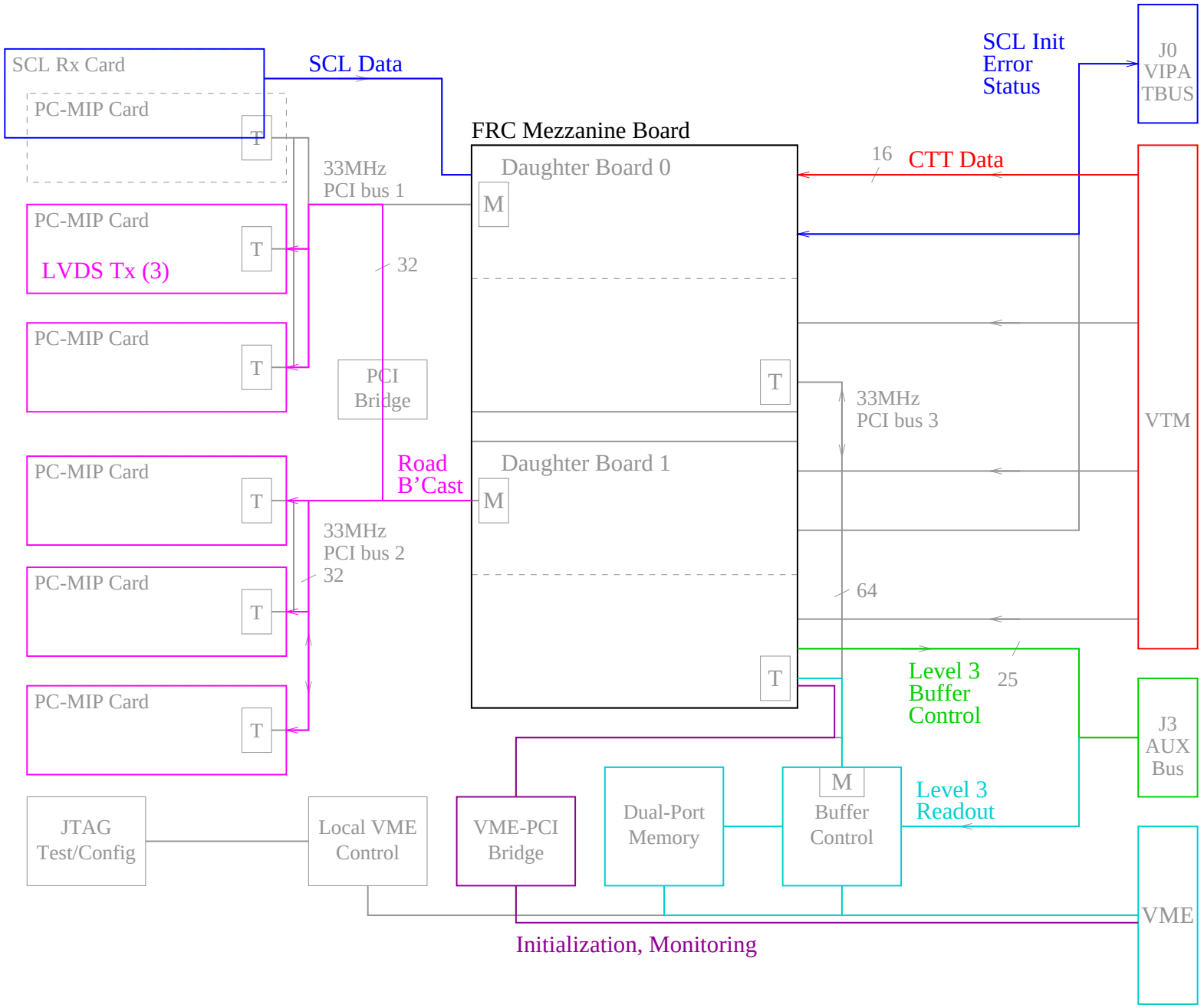

Silicon Track Card (STC)

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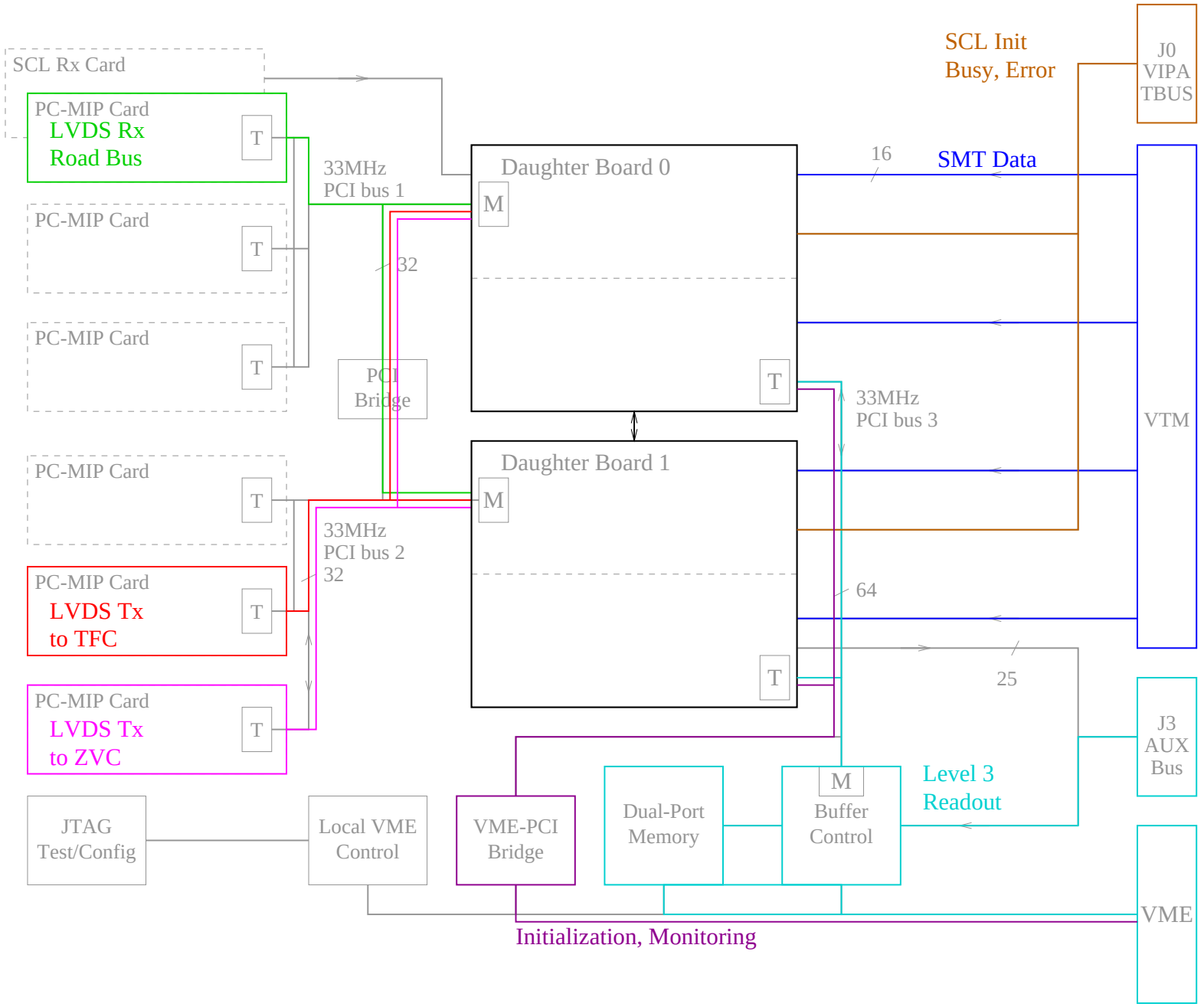

Track Fit Card (TFC)

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