



ELSEVIER

Available online at www.sciencedirect.com

SCIENCE @ DIRECT®

Nuclear Instruments and Methods in Physics Research A 535 (2004) 421–423

NUCLEAR
INSTRUMENTS
& METHODS
IN PHYSICS
RESEARCH
Section A

www.elsevier.com/locate/nima

Design and test of innovative CMOS pixel detectors

D. Passeri^{a,c}, P. Placidi^{a,c}, M. Petasecca^{a,c}, G. Matrella^{b,c}, A. Marras^{b,c,*},
P. Ciampolini^{b,c}, G.M. Bilei^c

^a*Dip. di Ing. Elettronica e dell'Informazione, Univ. di Perugia, Perugia, Italy*

^b*Dip. di Ing. dell'Informazione, Univ. di Parma, Parma, Italy*

^c*I.N.F.N., sezione di Perugia, Perugia, Italy*

Available online 17 August 2004

Abstract

In this work, design, implementation and test phases of a radiation sensor based on active pixel architectures are discussed. Fully standard CMOS technology has been exploited, allowing for easier integration of signal-processing circuitry. Alternative circuit schemes have been considered; a novel architecture, called WIPS, is introduced, aimed at a more efficient sparse-access mode of the sensor array. A first prototype of the chip has been fabricated, in a 0.18 μm CMOS technology. An automatic testing procedure has been devised, including design and fabrication of a suitable test board and of an optical bench. Preliminary results of the measurements are given, validating the overall approach and the operating principle of the WIPS architecture.

© 2004 Elsevier B.V. All rights reserved.

PACS: 85.40.e; 29.40.Wk

Keywords: Silicon; Radiation; Pixel; Sensors

1. Introduction

The adoption of standard VLSI CMOS technology has been proposed for charged-particle detection [1,2] in order to achieve higher resolution and lower manufacturing cost: the active pixel

sensor (APS) scheme was proposed to compensate for technology-related drawbacks (such as low charge collection efficiency). In this work, we discuss some issues related to the design and characterization of a CMOS active pixel sensor chip (RAPS01), developed in the framework of the radiation active pixel sensors (RAPS) INFN project. The project aims at the development of radiation sensors in a commercial, fully standard CMOS technology, conjugating fair signal-to-noise ratio and excellent on-chip signal processing.

*Corresponding author. Dip. di Ing. dell'Informazione, Parco Arca delle Scienze 181/A, Parma 43100, Italy. Tel.: +39-521-905-811; fax: +39-521-905-822.

E-mail address: amarras@nemo.unipr.it (A. Marras).

2. Technology analysis and system architecture

In order to satisfy behavioural specifics required to particle detectors, physical evaluation of several device fabrication technologies was carried out. In particular, charge collection performance and interference with neighbouring circuitry was estimated. Eventually, a $0.18\ \mu\text{m}$ United Microelectronics Corporation (UMC) technology was chosen [3] among several candidates. Such a technology features no intrinsic epitaxial layer; nevertheless, its lightly doped ($N = 10^{15}\ \text{cm}^{-3}$) substrate still allows for a satisfactory charge-collection efficiency (CCE), whereas it limits charge sharing among adjacent pixels and thus allows for very small pixel pitches. Because of the low supply voltage value ($1.8\ \text{V}$), total bulk depletion is far from being reached: device simulation shows that roughly 600 electrons are collected for a single minimum ionising particle (MIP) impact. Assuming a constant generation rate of 80 electron–holes pairs generated per μm , this value means that only electrons generated in the first $7\text{--}8\ \mu\text{m}$ of silicon depth are actually collected. This makes critical the balance among photodiode and parasitic capacitances, which calls for careful sizing of devices. Again, device simulation allows detailed analysis and has been used to optimize the photodiode area, with respect to charge collection, parasitic capacitance, dark current and minimum resolution concerns. Classical APS scheme is sketched in Fig. 1(left): it is based on a photodiode, which is periodically reverse-biased by a RESET pulse applied to a pull-up transistor. The impinging radiation generates charge that is collected at this junction, and lowers the voltage at the photodiode cathode (PhD

node). A source follower stage (M_{SF}) keeps the photodiode isolated from the output line which, in turn, is controlled by a *READ* enable. Main noise sources for this architectures (namely, thermal noise at the photodiode and charge-integration noise due to dark current) were estimate to give a global contribution not in excess of $1.4\ \text{mV}$. This, in turn, should guarantee a SNR in the order of several tens. The main advantage of this architecture is that, since it requires only a few devices, it lends itself to the design of compact pixels ($3.3 \times 3.3\ \mu\text{m}^2$, in the actual layout implementation shown in Fig. 2(left)) with an high fill factor. Several APS structures were designed and implemented in the test-chip RAPS01, in order to evaluate the influence of some options (guard rings, p-block layer, etc.). Random access to each pixel has been foreseen for testing purposes, by implementing dedicated row and column decoders. Pixel data are exported to the output pins in both analog and digital formats. Taking advantage from the capability of integrating high-quality, CMOS read-out circuitry, a more elaborate read-out scheme, oriented to an efficient sparse-access mode, has been devised and implemented. Such a novel scheme has been called weak inversion pixel sensor (WIPS). The basic WIPS scheme is shown in Fig. 1(right), and relies on a dynamic mechanism: first, columns and rows are precharged at different voltages: for instance, column is precharged HIGH and row is precharged LOW value. Then, the RESET pulse brings the photodiode in the inverse regime, and the M_{W} FET is switched off, just below the onset of the conduction region (thus in the weak inversion regime). In this case, a

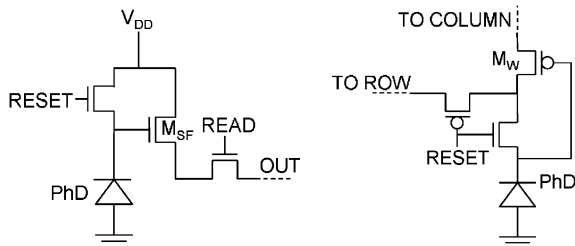


Fig. 1. left: APS pixel circuit; right: WIPS pixel circuit.

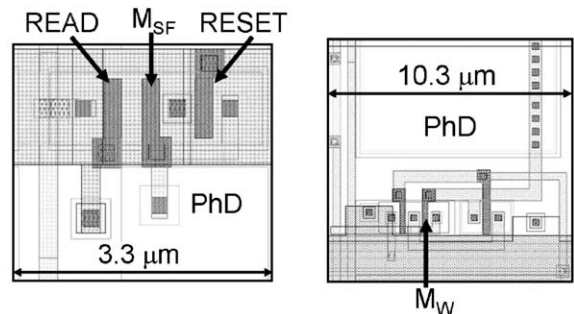


Fig. 2. left: APS pixel layout; right: WIPS pixel layout.

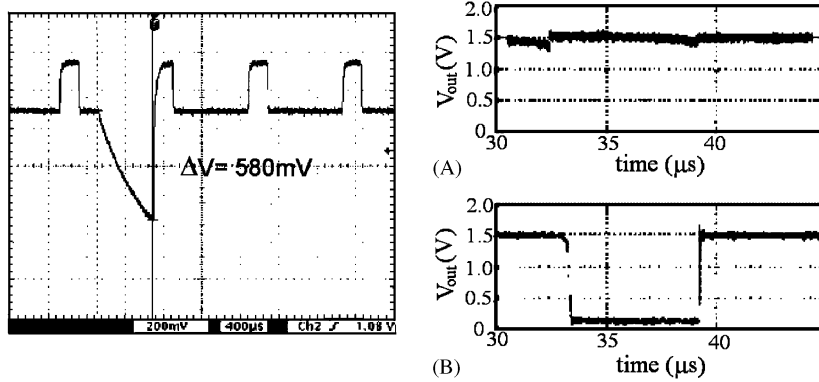


Fig. 3. left: APS α -particle response; right: WIPS laser response.

small voltage shift at the photodiode cathode turns M_W on, so that column and row charges are shared, resulting in a voltage lowering at the column line and a voltage increase at the row-line. Thus, the read-out scheme allows for asynchronous, simultaneous detection of both the coordinates of the hit pixel. The operating mode devised above allows for a “sparse”, more efficient, access mode to the detector matrix: assuming a pixel array counting m rows and n columns, the conventional scheme would require to scan each pixel in the array thus requiring a time proportional to $(n \times m)$ to get the whole frame. By independently scanning column and row outputs, the WIPS scheme requires a read-out time proportional to $(n + m)$. The presence of a pMOS device could in principle be a problem, as the n-well junction actually may act as a parasitic charge drain, competing with the photodiode: a suitable area ratio between the photodiode and the pMOS footprints has been used in order to make this drawback tolerable; this, however, makes WIPS pixels fairly larger ($10.3 \times 10.3 \mu\text{m}^2$) than APS ones, as shown in Fig. 2(right).

3. Test

The first chip prototype includes 11 APS arrays and 8 WIPS arrays (differing in some processing-layer options and in design parameters such as pixel pitch, guard rings, etc.). Several simpler test

structures are integrated as well. To accomplish independent tests of each structure, without requiring an excessive number of I/O pins, two different versions of the bonding schemes have been applied, each allowing to access a subset of devices. Due to the variety of architectures and operating modes, a fairly articulated sequence of test signals is to be generated and delivered to the chip for testing purposes. A dedicated test board has thus been realized and an optical test-bench has been set up for measurements under laser irradiation. Preliminary test results are quite encouraging: response of both APS and WIPS pixels are satisfactory. The APS response to an α -particle hit is shown in Fig. 3(left): a radiation-triggered voltage drop is clearly visible on the analog output. Fig. 3(right) shows the WIPS digital responses to dark condition (A) and laser pulse (B). A more comprehensive set of data is being acquired and will be available for presentation in the next future: suggestions coming from RAPS01 test results will be useful for the realization of a second chip (RAPS02), which is currently been designed.

References

- [1] D. Husson, et al., Nucl. Instr. and Math. A 461 (2001) 511.
- [2] R. Turchetta, et al., Nucl. Instr. and Math. A 458 (2001) 677.
- [3] D. Passeri, et al., Nucl. Instr. and Math. A 511 (2003) 92.