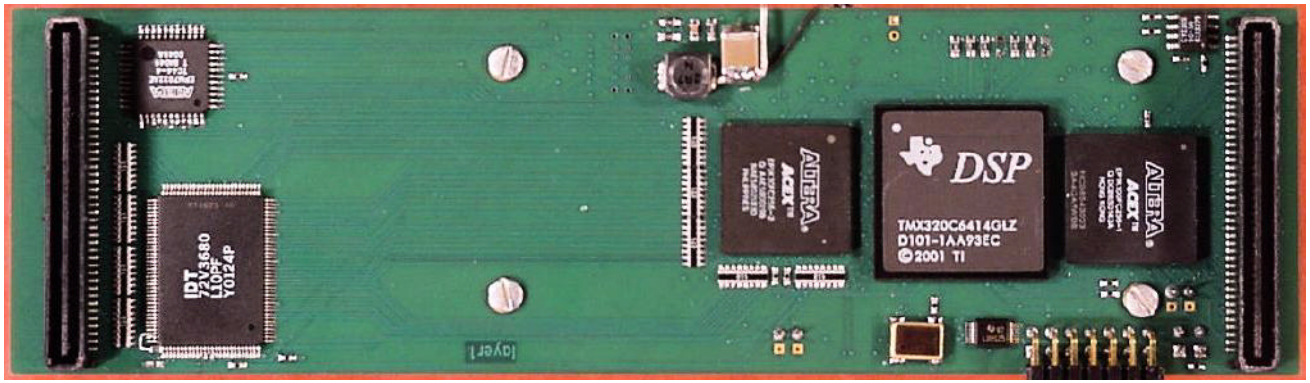
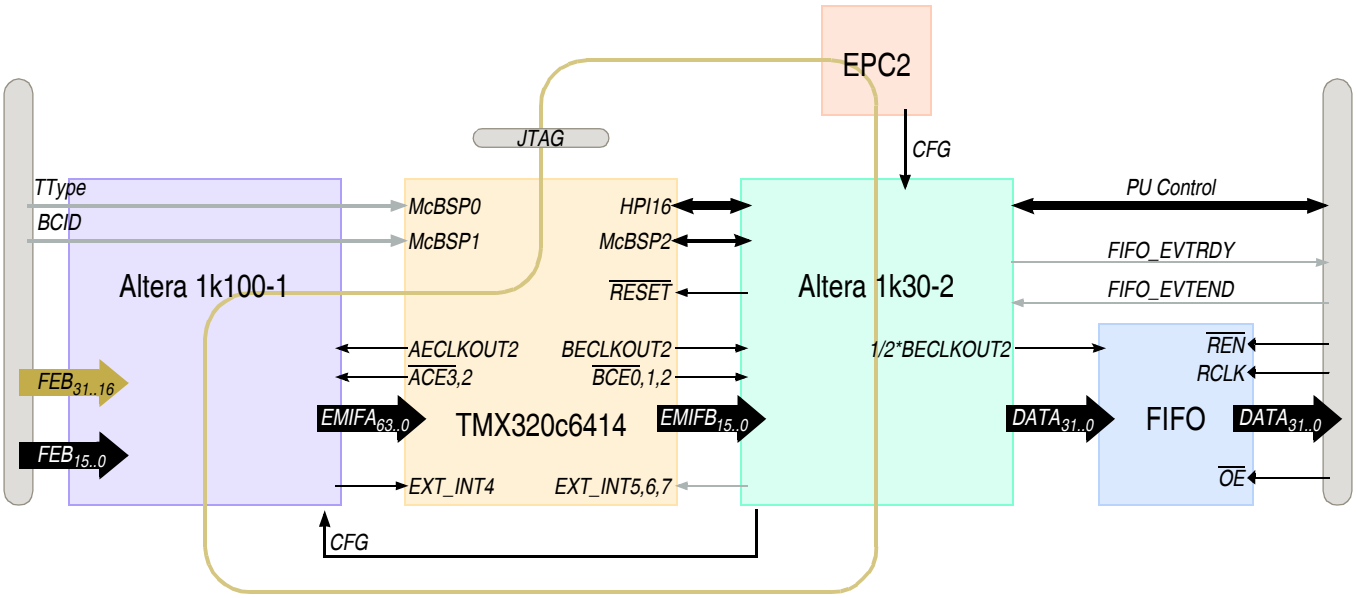
Status of the DSP6414 Processing Unit



The 6414 PU in the ROD Demo format has been designed during November 2001 jointly by Nevis and LAPP.

- The PCB was submitted for fabrication early December, and one fully-assembled board has been received back at Nevis early January.
- The DSP configuration jumpers (pull-up or pull-down resistors) were set for 480 MHz CPU frequency and 80 MHz EMIFA/B synchronous memory clocks (CPU/6).
- A second "dummy" 6414 PCB was equipped (by hand, at Nevis) with the power distribution system only (switching regulator, MOS switch, all 0.1 μF bypass capacitors), to allow for stand-alone measurements *(more →)*
- The fully-assembled PU was powered on for the first time on Jan 18.
- By Jan 24, successful tests of the Input FPGA, Output FPGA, DSP, FIFO led to decision to assemble a 2nd board for delivery to LAPP this week.



Output FPGA - VME interface tests - HPI boot

- The DSP JTAG port showed up to be non functional, rendering impossible the programming of any of the three Altera FPGAs on the board.
- The DSP had to be removed from the JTAG chain by making use of the 0 Ω resistors (jumpers) foreseen "just in case".
- The Output FPGA was configured successfully, and the DSP booted via its 16-bit host interface.

DSP data to Output FPGA and external FIFO

- Tested the DSP → Output FPGA serial port (McBSP2)
- Tested the DSP EMIFB (synchronous FIFO write, latency 0, to the Output FIFO) up to 80 MHz.
  (In the future this interface will be tested up to 120 MHz.)
- Output FPGA converts EMIFB data 16 bits @ BECLKOUT2 to 32 bits @ half the speed for writing to the event FIFO.

EPC2

- Programmed the on-board EPC2 device with a stable version of the Output FPGA code. Now the Output FPGA is configured from EPC2 at power-up.

Input FPGA - FEB data - DSP EMIF A

- Programmed the Input FPGA (FEB data serial-to-parallel conversion, data rearrangement, error checking) via JTAG and/or VME (through the Output FPGA).
- Tested the Input FPGA → DSP EMIFA (synchronous FIFO read, latency 3) 64 bits @ 80MHz. (In the future this interface will be tested at 100 MHz, with a 600 MHz DSP.)
- Note : the FEB input data to the Input FPGA comes from Atlas FEB via the optical link, followed by G-link deserializer (double frame mode) and a 16-bit to 32-bit demux (FPGA on the Nevis VME test board).

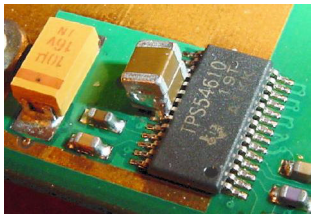
Summary of DSP DMA tests

- Tested **QDMA** (quick DMA, submitted via software) from **EMIFA to SRAM** (32-bit or 64-bit element size) and from **SRAM to EMIFB** (32-bit element size).
- Tested input DMA synchronization on EXT_INT4 (starts automatically, without intervention of the CPU core) from EMIFA to SRAM.

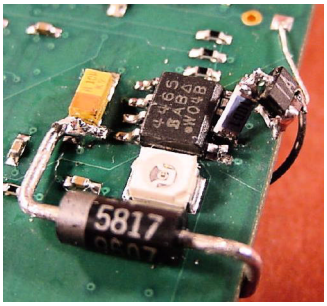
Second board has been built, tested, and will be delivered to LAPP.

Power Supply - Summary

- The 64x DSPs use a 0.12 µm CMOS process, with separate core (1.2 or 1.4 V) and I/O (3.3 V) power supply voltages.
- Our experience with the 6202/6203 DSPs has shown that proper power supply sequencing can be a tricky issue!
- The power consumption of the 64x is still listed as "TBD" in the data sheet.
- Therefore, we assumed a worst-case 2 A @ 1.2 V and we decided to use a **switching regulator** for the DSP core voltage power supply.
- The switcher has a "power good" output which enables the DSP I/O voltage via a MOS switch.
- Initial tests done in January showed a clean 1.2 V rail, but very noisy 3.3 V primary (due to the switching regulator). Additional 20 µF capacitance had to be added directly on the input pins of the switcher.



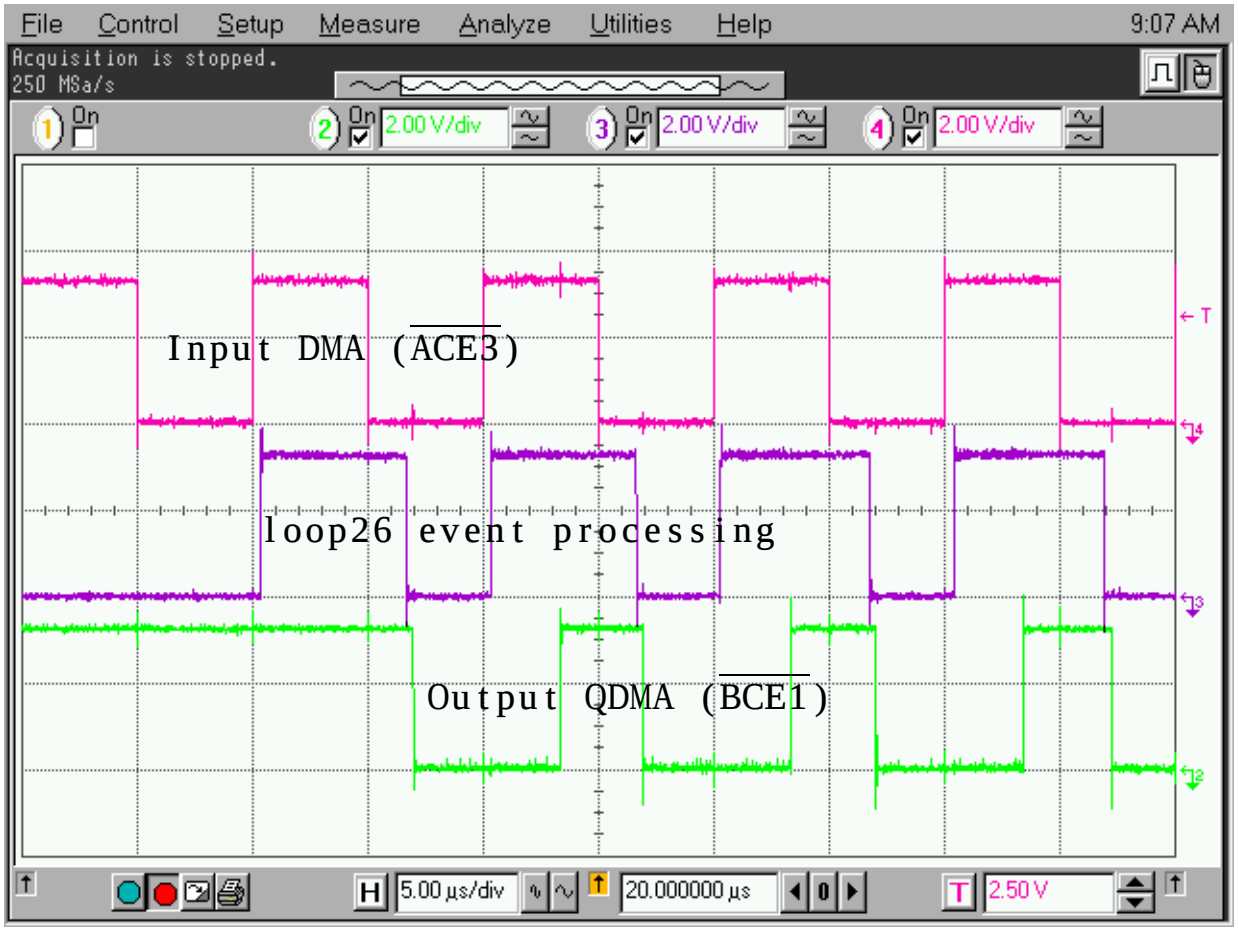
- Meanwhile, an *updated Silicon Errata* for the 6414 DSP became available on TI web site. New, tighter power sequencing requirements were introduced. Failure to comply means risk to damage the device!
- As a result, the entire power distribution has been revisited and finally the "dummy" PCB was "retro-fitted" with a new 3.3 V discrete switch and Schottky diode. After a new set of measurements (power-on and power-off ramps), we decided to implement the changes on the fully-assembled 6414 board.



A First Look ...

- Input DMA and output DMA do indeed overlap, with no visible interference.

- Running the **loop26** optimal filtering code (developed for the 6202/6203) takes 6.5 μs for 128 channels at 480 MHz
  i.e. 49 CPU cycles/pair of channels,
  very close to the simulator prediction (52 cycles)

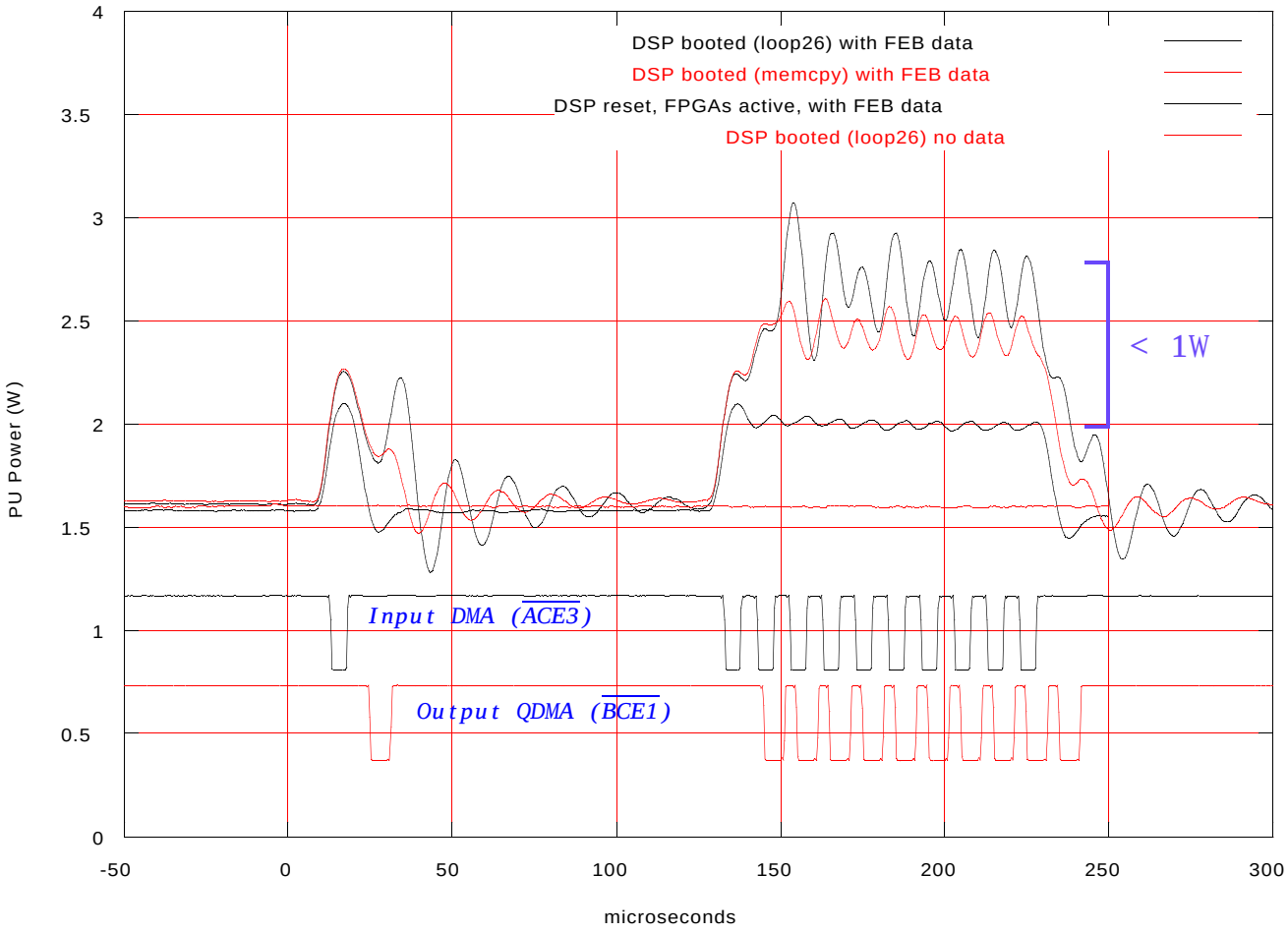


PU Power consumption

Measurement conditions:

- 480 MHz CPU clock, 1.2 V DSP core voltage
- 80 MHz EMIFA (to Input FPGA) and EMIFB (to Output FPGA) memory clocks
  Except when DSP is under RESET: 20 MHz EMIF clocks.
- Input DMA, output DMA, loop26 event processing (128 channels)
- 100 kHz instantaneous L1A trigger rate

Total PU power ~ 3 W, DSP core ~ 1 W



Next steps

⇒Boundary scan testing *(JTAG)* will be done at LAPP

⇒Handling of the TTC information still to be done (serial ports servicing by DMA etc.)

⇒Output event (fragment/burst) synchronization needs to be studied. Contrary to the 6203 DSP, this device does not have "DMA Complete" output pins, nor does it support level-triggered (as opposed to edge-triggered) DMA synchronization!

⇒Evaluation of the optimal filtering code written specifically for the 64x !
Input event handling (Input FPGA) to fit the needs of the OF code being investigated.

This new PU should allow, during the next months, to evaluate the 6414 TI DSP for use in the LArg ROD system.

If this DSP, or the 6203C (also 0.12 μm CMOS) is chosen, then the **power supply scheme (sequencing) needs to be revisited!** We should consider the possibly, that the DSP core voltage be supplied by the motherboard.

The DSP choice is due for July 2002.